

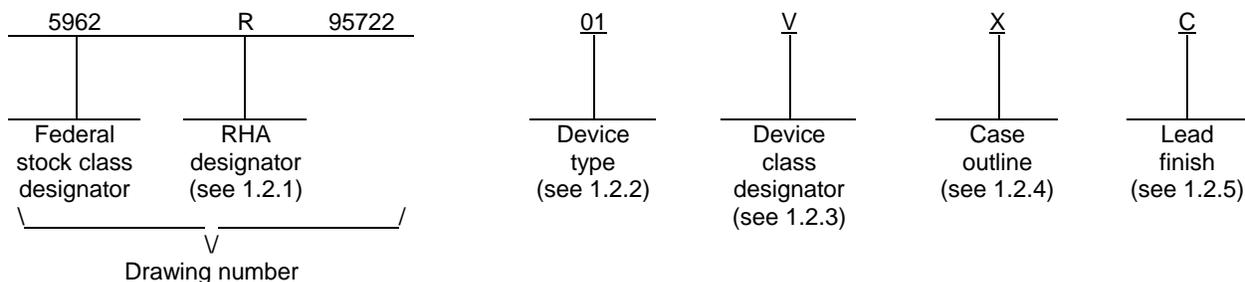
REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R096-96.	96-04-05	Monica L. Poelking
B	Correct title to accurately describe device function. Update boilerplate to current MIL-PRF-38535 requirements and to include radiation hardness assurance requirements. – LTG	07-05-25	Thomas M. Hess

REV																					
SHEET																					
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28							
REV STATUS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B	
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	
PMIC N/A	PREPARED BY Thomas M. Hess						DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil MICROCIRCUIT, DIGITAL, CMOS, RADIATION HARDENED 16-BIT MICROPROCESSOR, MONOLITHIC SILICON														
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas M. Hess																				
	APPROVED BY Monica L. Poelking																				
	DRAWING APPROVAL DATE 96-01-28																				
	REVISION LEVEL B																				
						SIZE A	CAGE CODE 67268	5962-95722													
						SHEET 1 OF 28															

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	80C86RH	Radiation hardened 16-bit microprocessor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
X	See figure 1	42	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage (V _{DD})	+7.0 V dc
Input or output voltage range	V _{SS} -0.3 V dc to V _{DD} +0.3 V dc
Storage temperature range (T _{STG}).....	-65°C to +150°C
Junction temperature (T _J).....	+175°C
Thermal resistance, junction-to-case (θ _{JC})	
Case Q	8.6°C/W
Case X.....	9.7°C/W
Thermal resistance, junction-to-ambient (θ _{JA})	
Case Q	40°C/W
Case X.....	72.1°C/W
Maximum package power dissipation at T _A = +125°C (P _D) 2/	
Case Q	1.25 W
Case X.....	0.69 W
Maximum lead temperature (soldering, 10 seconds).....	+300°C

1.4 Recommended operating conditions.

Operating supply voltage range (V _{DD})	4.75 V dc to +5.25 V dc
Operating temperature range (T _A).....	-35°C to +125°C
Input low voltage range (V _{IL})	0 V dc to +0.8 V dc
Input high voltage range (V _{IH}).....	3.5 V dc to V _{DD}
Clock input low voltage range (V _{ILC})	0 V dc to +0.8 V dc
CLK and MS/MX input high voltage range (V _{ILH})	V _{DD} - 0.8 V dc to V _{DD}

1.5 Radiation features.

Maximum total dose available (Dose rate = 50 – 300 rads(Si)/sec)	> 100K Rads(Si)
Transient upset	> 10 ⁸ Rads(Si)/sec 3/
Single event upset (SEU)	6 MeV/(mg/cm ²) 3/
Single event latchup (SEL).....	75 MeV/(mg/cm ²) 3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at a rate of 25.0 mW/°C for case Q and 13.9 mW/°C for case X.
- 3/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

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2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <http://www.astm.org> or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

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3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} -35°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage (TTL)	V _{OH1}	V _{DD} = 4.75 V, I _{OH} = -2.5 mA V _{IN} = 0 V or V _{DD}	1, 2, 3	All	3.0		V
High level output voltage (CMOS)	V _{OH2}	V _{DD} = 4.75 V, I _{OH} = -100 μA V _{IN} = 0 V or V _{DD}	1, 2, 3	All	V _{DD} -0.4		V
Low level output voltage	V _{OL}	V _{DD} = 4.75 V, I _{OL} = +2.5 mA V _{IN} = 0 V or V _{DD}	1, 2, 3	All		0.4	V
Input leakage current, low	I _{IL}	V _{DD} = 5.25 V, V _{IN} = GND or V _{DD} DIP pins: 17-19, 21-23, 33 ^{2/}	1, 2, 3	All	-1.0	+1.0	μA
Input leakage current, high	I _{IH}				-1.0	+1.0	
Output leakage current, low	I _{OZL}	V _{DD} = 5.25 V, V _{OUT} = 0 V or V _{DD} DIP pins: 2-16, 26-29, 32, 34-39 ^{2/}	1, 2, 3	All	-10	+10	μA
Output leakage current, high	I _{OZH}				-10	+10	
Input current bus hold, high	I _{BHH}	V _{DD} = 4.75 V and 5.25 V V _{IN} = 3.0 V Pins: 2-16, 26-32, 34-39 ^{2/ 3/}	1, 2, 3	All	-600	-40	μA
Input current bus hold, low	I _{BHL}	V _{DD} = 4.75 V and 5.25 V V _{IN} = 0.8 V Pins: 2-16, 34-39 ^{2/ 4/}	1, 2, 3	All	40	600	μA
Standby power supply current	I _{DDSB}	I _O = 0 mA, V _{IN} = V _{DD} or V _{SS} V _{DD} = 5.25 V ^{5/}	1, 2, 3	All		500	μA
Operating power supply current	I _{DDOP}	I _O = 0 mA, V _{IN} = V _{DD} or V _{SS} V _{DD} = 5.25 V, f = 1 MHz	1, 2, 3	All		12	mA/ MHz
Functional tests		See 4.4.1b, V _{IN} = V _{DD} or V _{SS} V _{DD} = 4.75 V and 5.25 V, f = 1 MHz	7, 8	All			
Noise immunity functional tests		See 4.4.1b V _{DD} = 4.75 V and 5.25 V V _{IN} = 0.8 V or 3.5 V ^{6/}	7, 8	All			
Input capacitance	C _{IN}	See 4.4.1c, f = 1 MHz, V _{DD} = open All measurements are referenced device GND.	4	All		15	pF
Output capacitance	C _{OUT}		4	All		15	pF
I/O capacitance	C _{I/O}		4	All		20	pF
CLK cycle period	t _{CLCL}	V _{DD} = 4.75 V and 5.25 V ^{7/}	9, 10, 11	All	200		ns
CLK low time	t _{CLCH}	V _{DD} = 4.75 V ^{7/}	9, 10, 11	All	118		ns
CLK high time	t _{CHCL}	V _{DD} = 4.75 V and 5.25 V ^{7/}	9, 10, 11	All	69		ns
Data in setup time	t _{DVCL}	V _{DD} = 4.75 V ^{7/}	9, 10, 11	All	30		ns
Data in hold time	t _{CLDX1}	V _{DD} = 4.75 V ^{7/}	9, 10, 11	All	10		ns
Ready setup time into device	t _{RYHCH}	V _{DD} = 4.75 V ^{7/}	9, 10, 11	All	113		ns
Ready hold time into device	t _{CHRYX}	V _{DD} = 4.75 V ^{7/}	9, 10, 11	All	30		ns
Ready inactive to CLK	t _{RYLCL}	V _{DD} = 4.75 V ^{7/ 8/}	9, 10, 11	All	-8		ns
Hold setup time	t _{HVCH}	V _{DD} = 4.75 V ^{7/}	9, 10, 11	All	35		ns
INTR, NMI, TEST setup time	t _{INVCH}	V _{DD} = 4.75 V ^{7/}	9, 10, 11	All	30		ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/} -35°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
MINIMUM MODE TIMING RESPONSE							
Address valid delay	t _{CLAV}	V _{DD} = 4.75 V C _L = 100 pF	9, 10, 11	All	10	110	ns
ALE width	t _{LHLL}		9, 10, 11	All	t _{CLCH} -20		ns
ALE active delay	t _{CLLH}		9, 10, 11	All		80	ns
ALE inactive delay	t _{CHLL}		9, 10, 11	All		85	ns
Address hold time to ALE inactive	t _{LLAX}		9, 10, 11	All	t _{CLCH} -10		ns
Control active delay 1	t _{CVCTV}		9, 10, 11	All	10	110	ns
Control active delay 2	t _{CHCTV}		9, 10, 11	All	10	110	ns
Control inactive delay	t _{CVCTX}		9, 10, 11	All	10	110	ns
RD active delay	t _{CLRL}		9, 10, 11	All	10	165	ns
RD inactive delay	t _{CLRH}		9, 10, 11	All	10	50	ns
RD inactive to next address active	t _{RHAV}		9, 10, 11	All	t _{CLCH} -15		ns
HLDA valid delay	t _{CLHAV}		9, 10, 11	All	10	160	ns
RD width	t _{RLRH}		9, 10, 11	All	2t _{CLCL} -75		ns
WR width	t _{WLWH}		9, 10, 11	All	2t _{CLCH} -60		ns
Address valid to ALE low	t _{AVLL}		9, 10, 11	All	t _{CLCH} -60		ns
Output rise time	t _{OLOH}	From 0.8 V to 2.0 V V _{DD} = 4.75 V, C _L = 100 pF	9, 10, 11	All		20	ns
Output fall time	t _{OHOL}	From 2.0 V to 0.8 V V _{DD} = 4.75 V, C _L = 100 pF	9, 10, 11	All		20	ns

TIMING REQUIREMENT

CLK cycle period	t _{CLCL}	V _{DD} = 5.25 V V _{DD} = 4.75 V	9, 10, 11	All	200		ns
CLK low time	t _{CLCH}	V _{DD} = 4.75 V	9, 10, 11	All	118		ns
CLK high time	t _{CHCL}	V _{DD} = 5.25 V V _{DD} = 4.75 V	9, 10, 11	All	69		ns
Data in setup time	t _{DVCL}	V _{DD} = 4.75 V	9, 10, 11	All	30		ns
Data in hold time	t _{CLDX1}	V _{DD} = 4.75 V	9, 10, 11	All	10		ns
RDY setup time into device	t _{RYHCH}	V _{DD} = 4.75 V	9, 10, 11	All	113		ns
RDY hold time into device	t _{CHRYX}	V _{DD} = 4.75 V	9, 10, 11	All	30		ns
Ready inactive to CLK	t _{RYLCL}	V _{DD} = 4.75 V ^{8/}	9, 10, 11	All	-8		ns
INTR, NMI, test setup time	t _{INVCH}	V _{DD} = 4.75 V	9, 10, 11	All	30		ns
RQ/GT setup time	t _{GVCH}	V _{DD} = 4.75 V	9, 10, 11	All	20		ns
RQ hold time into device	t _{CHGX}	V _{DD} = 4.75 V ^{9/}	9, 10, 11	All	40	t _{CHCL} +10	ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/} -35°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	

TIMING REQUIREMENT – Continued.

CLK rise time	t _{CH1CH2}	Min and max mode from 1.0 V to 3.5 V ^{10/} V _{DD} = 4.75 V and 5.25 V	9, 10, 11	All		15	ns
CLK fall time	t _{CL2CL1}	Min and max mode from 3.5 V to 1.0 V ^{10/} V _{DD} = 4.75 V and 5.25 V	9, 10, 11	All		15	ns
Input rise time	t _{LIH}	Min and max mode from 0.8 V to 2.0 V ^{10/} V _{DD} = 4.75 V and 5.25 V	9, 10, 11	All		25	ns
Input fall time	t _{HIH}	Min and max mode from 2.0 V to 0.8 V ^{10/} V _{DD} = 4.75 V and 5.25 V	9, 10, 11	All		25	ns

MAXIMUM MODE TIMING RESPONSE

Address float delay	t _{CLAZ}	V _{DD} = 4.75 V and 5.25 V C _L = 100 pF Min and max mode ^{10/ 11/}	9, 10, 11	All	t _{CLAX}	80	ns
Status float delay	t _{CHSZ}	V _{DD} = 4.75 V and 5.25 V C _L = 100 pF Max mode only ^{10/ 11/}	9, 10, 11	All		80	ns
Data hold time after \overline{WR}	t _{WHDX}	V _{DD} = 4.75 V and 5.25 V C _L = 100 pF Minimum mode ^{10/}	9, 10, 11	All	t _{CLCL-30}		ns
Data hold time	t _{CLDX2}	V _{DD} = 4.75 V and 5.25 V C _L = 100 pF Min and max mode ^{10/}	9, 10, 11	All	10		ns
Address hold time	t _{CLAX}	V _{DD} = 4.75 V and 5.25 V C _L = 100 pF Min and max mode ^{10/}	9, 10, 11	All	10		ns
Data valid delay	t _{CLDV}	V _{DD} = 4.75 V and 5.25 V C _L = 100 pF Min and max mode ^{10/}	9, 11, 11	All	10	110	ns
Address float to read active	t _{AZRL}	V _{DD} = 4.75 V and 5.25 V C _L = 100 pF Min and max mode ^{10/ 11/}	9, 10, 11	All	0		ns

MINIMUM COMPLEXITY SYSTEM TIMING

Ready active to status passive	t _{RYHSH}	V _{DD} = 4.75 V ^{8/ 12/}	9, 10, 11	All		110	ns
Status active delay	t _{CHSV}	V _{DD} = 4.75 V	9, 10, 11	All	10	110	ns
Status inactive delay	t _{CLSH}	V _{DD} = 4.75 V ^{12/}	9, 10, 11	All	10	130	ns
Address valid delay	t _{CLAV}	V _{DD} = 4.75 V	9, 10, 11	All	10	110	ns
\overline{RD} active delay	t _{CLRL}	V _{DD} = 4.75 V	9, 10, 11	All	10	165	ns
\overline{RD} inactive delay	t _{CLRH}	V _{DD} = 4.75 V	9, 10, 11	All	10	150	ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/} -35°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
MINIMUM COMPLEXITY SYSTEM TIMING – Continued.							
\overline{RD} inactive to next address	t _{RHAV}	V _{DD} = 4.75 V	9, 10, 11	All	t _{CLCL} -45		ns
\overline{GT} active delay	t _{CLGL}	V _{DD} = 4.75 V	9, 10, 11	All	0	85	ns
\overline{GT} inactive delay	t _{CLGH}	V _{DD} = 4.75 V	9, 10, 11	All	0	85	ns
\overline{RD} width	t _{RLRH}	V _{DD} = 4.75 V	9, 10, 11	All	2t _{CLCL} -75		ns
Output rise time	t _{OLOH}	From 0.8 V to 2.0 V V _{DD} = 4.75 V	9, 10, 11	All		20	ns
Output fall time	t _{OHOL}	From 2.0 V to 0.8 V V _{DD} = 4.75 V	9, 10, 11	All		20	ns

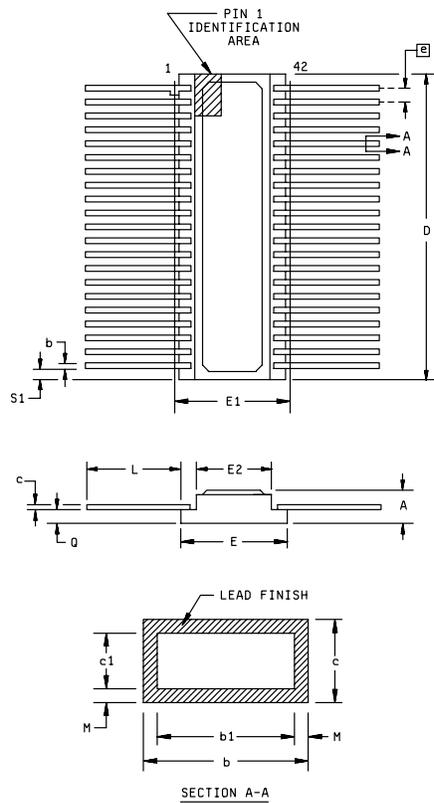
- ^{1/} RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, these devices are only tested at the 'R' level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
- ^{2/} Pin numbers are for 40 pin dip. Use equivalent functions for 42 pin flat package.
- ^{3/} I_{BHH} should be measured after raising V_{IN} to V_{DD} and then lowering to valid input high level of 3.0 V on the following pins; 2-16, 26-32, 34-39.
- ^{4/} I_{BHL} should be measured after raising V_{IN} to GND and then raising to valid input low level of 0.3 V on the following pins: 2-16, 34-39.
- ^{5/} I_{DDSB} tested during clock high time after HALT instruction execution.
- ^{6/} CLK and MN/ \overline{MX} input high = V_{DD} - 0.8 V.
- ^{7/} Setup requirement for asynchronous signal to guarantee recognition at next clock.
- ^{8/} Applies only to T2 state (8 ns into T3).
- ^{9/} The device actively pulls the RQ/ \overline{GT} pin to a logic one on the following clock low time.
- ^{10/} The parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
- ^{11/} Output drivers disabled. Bus hold circuitry still active.
- ^{12/} Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

TABLE IB. SEP test limits. ^{1/} ^{2/}

Device type	T _A = Temperature ±10°C ^{3/}	V _{DD} = 4.75 V SEU Bias	Bias for latch-up test V _{DD} = 5.25 V SEL Bias LET = ^{3/}
		Effective LET no upsets [MeV/(mg/cm ²)]	
All	+25°C	≥ 6	≥ 75

- ^{1/} For SEP test conditions, see 4.4.4.2 herein.
- ^{2/} Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
- ^{3/} Worst case temperature for latch-up test is T_A = +125°C.
Test temperature for SEU test is T_A = +25°C.

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Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	---	2.54	---	0.100
b	0.43	0.64	0.017	0.025
b1	0.43	0.58	0.017	0.023
c	0.18	0.33	0.007	0.013
c1	0.18	0.25	0.007	0.010
D	26.54	27.31	1.045	1.075
E	16.00	16.51	0.630	0.650
E1	---	17.27	---	0.680
E2	13.46	13.97	0.530	0.550
e	1.27 BSC		0.050 BSC	
L	8.13	8.89	0.320	0.350
Q	1.14	1.65	0.045	0.065
S1	0	---	0	---
M	---	0.04	---	0.0015
N	42		42	

FIGURE 1. Case outlines.

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Device type	01		
Case outline	Q		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	21	RESET
2	AD14	22	READY
3	AD13	23	$\overline{\text{TEST}}$
4	AD12	24	QS1 ($\overline{\text{INTA}}$)
5	AD11	25	QS0 (ALE)
6	AD10	26	$\overline{\text{S0}}$ ($\overline{\text{DEN}}$)
7	AD9	27	$\overline{\text{S1}}$ ($\overline{\text{DT/R}}$)
8	AD8	28	$\overline{\text{S2}}$ ($\overline{\text{M/IO}}$)
9	AD7	29	$\overline{\text{LOCK}}$ ($\overline{\text{WR}}$)
10	AD6	30	$\overline{\text{RQ/GT1}}$ (HLDA)
11	AD5	31	$\overline{\text{RQ/GT0}}$ (HOLD)
12	AD4	32	$\overline{\text{RD}}$
13	AD3	33	MN/ $\overline{\text{MX}}$
14	AD2	34	$\overline{\text{BHE/S7}}$
15	AD1	35	A19/S6
16	AD0	36	A18/S5
17	NMI	37	A17/S4
18	INTR	38	AD16/S3
19	CLK	39	AD15
20	GND	40	V _{DD}

FIGURE 2. Terminal connections.

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Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	22	RESET
2	AD14	23	READY
3	AD13	24	$\overline{\text{TEST}}$
4	AD12	25	QS1($\overline{\text{INTA}}$)
5	AD11	26	QS0 (ALE)
6	AD10	27	$\overline{\text{S0}}$ ($\overline{\text{DEN}}$)
7	AD9	28	$\overline{\text{S1}}$ ($\overline{\text{DT/R}}$)
8	AD8	29	$\overline{\text{S2}}$ ($\overline{\text{M/IO}}$)
9	AD7	30	$\overline{\text{LOCK}}$ ($\overline{\text{WR}}$)
10	AD6	31	$\overline{\text{RQ/GT1}}$ (HLDA)
11	AD5	32	$\overline{\text{RQ/GT0}}$ (HOLD)
12	AD4	33	$\overline{\text{RD}}$
13	AD3	34	MN/ $\overline{\text{MX}}$
14	AD2	35	$\overline{\text{BHE/S7}}$
15	AD1	36	A19/S6
16	AD0	37	A18/S5
17	NC	38	A17/S4
18	NMI	39	AD16/S3
19	INTR	40	NC
20	CLK	41	AD15
21	GND	42	V _{DD}

NC = No connection

FIGURE 2. Terminal connections – Continued.

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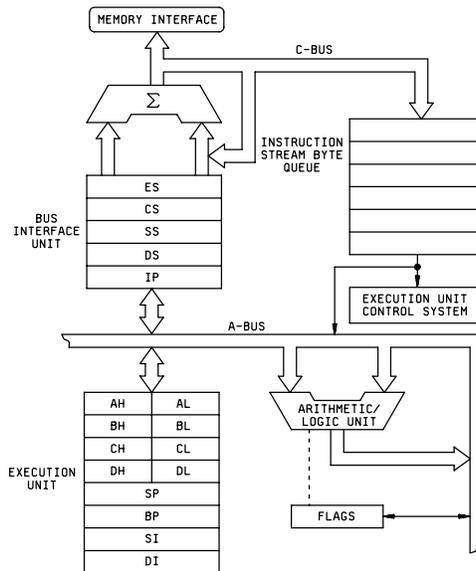
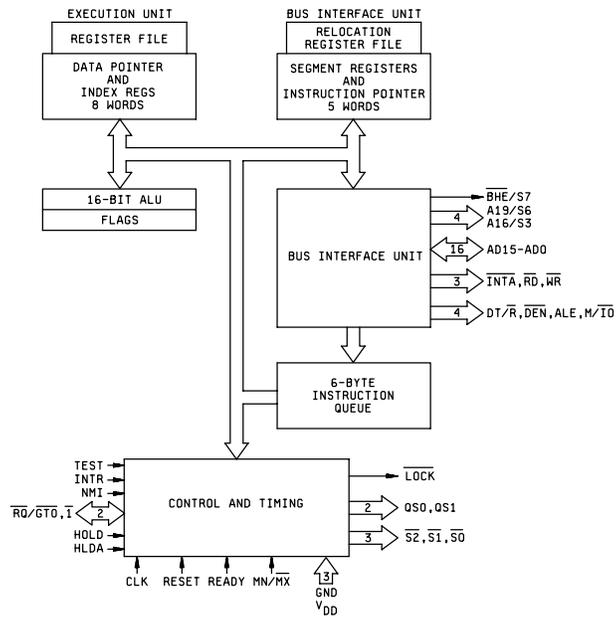
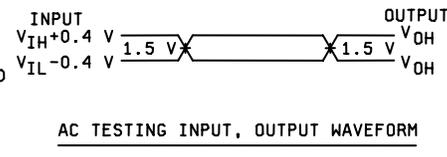
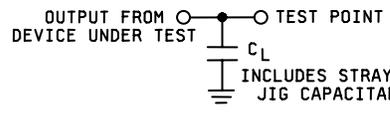
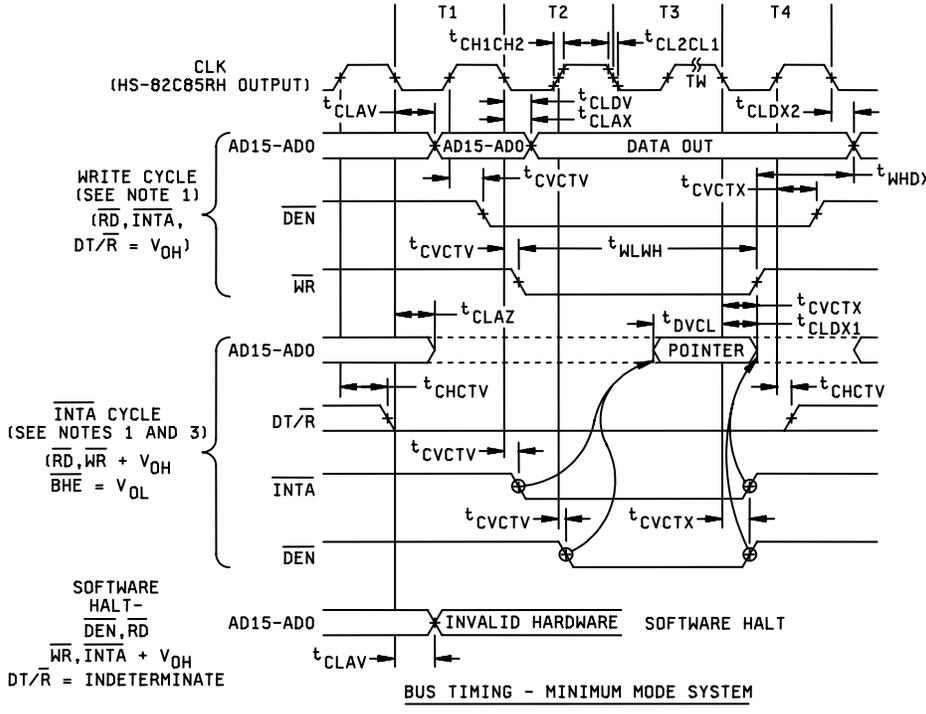


FIGURE 3. Block diagram.

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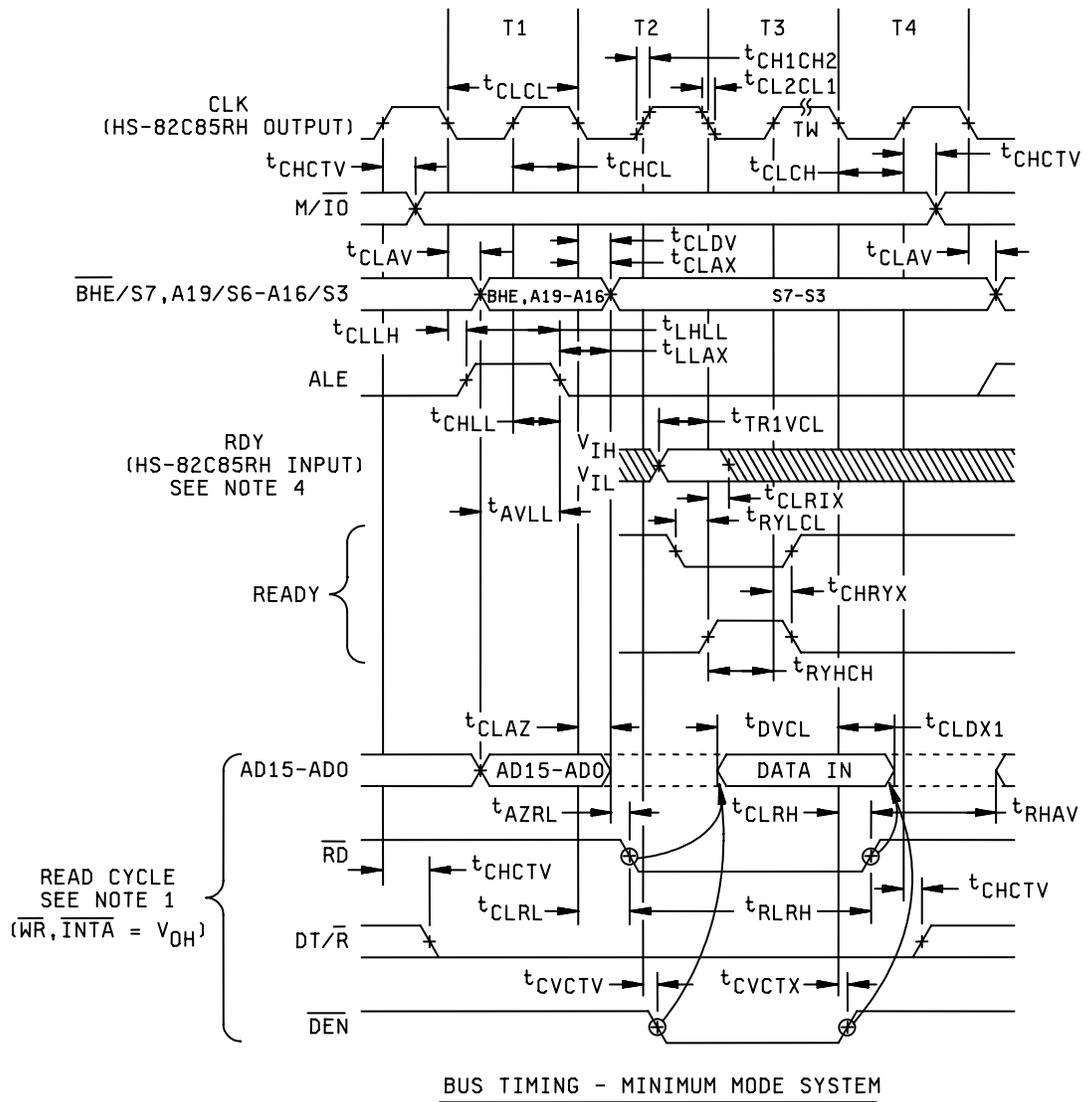


NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T2, T3, and TW to determine if TW machine states are to be inserted.
3. Two \overline{INTA} cycles run back-to-back. The device local ADDR/DATA bus is inactive during both \overline{INTA} cycles. Control signals are shown for the second \overline{INTA} cycle.
4. All timing measurements are made at 1.5 V unless otherwise noted.
5. All inputs signals (other than CLK) must be switched between $V_{IL(MAX)} - 0.4 V$ and $V_{IH(MIN)} + 0.4 V$. CLK must switch between 0.4 V and $V_{DD} - 0.4 V$. t_r and t_f must be less than or equal to 15 ns. CLK, t_r and t_f must be less than or equal to 10 ns.

FIGURE 4. Timing waveforms and test circuit.

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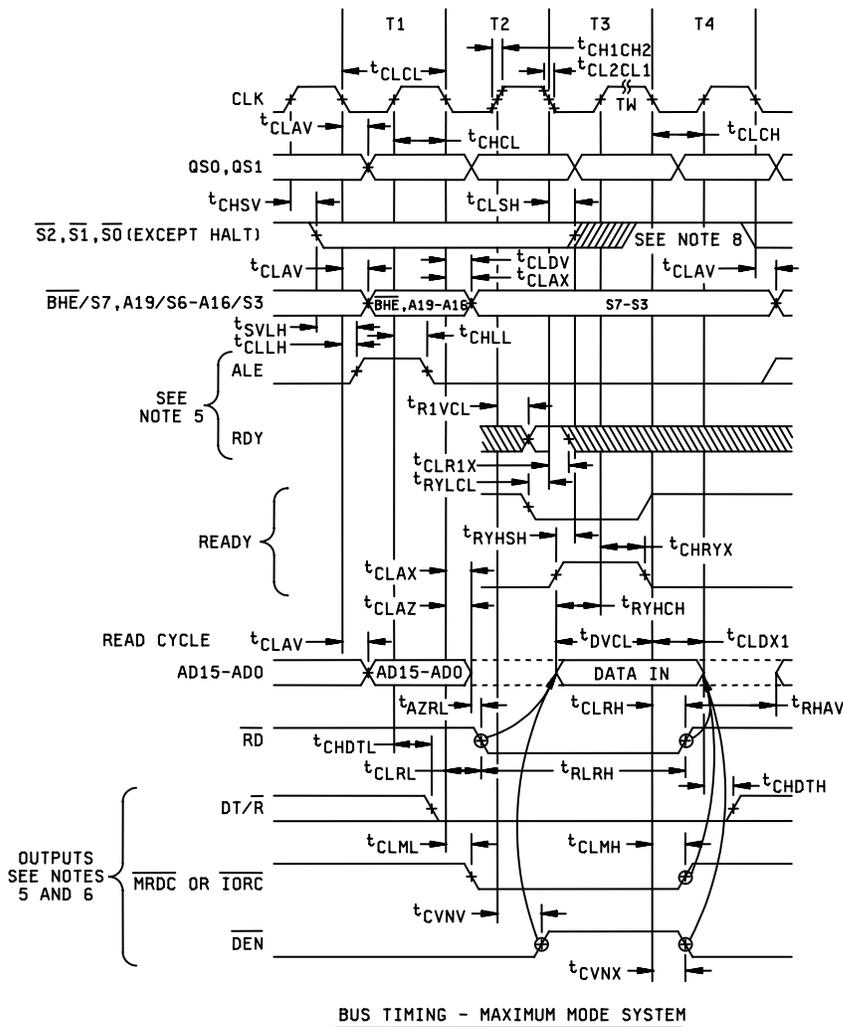
BUS TIMING - MINIMUM MODE SYSTEM

NOTES:

1. Unless otherwise specified, all signals switch between V_{OH} and V_{OL} .
2. RDY is sampled near the end of T2, T3, and TW to determine if TW machines states are to be inserted.
3. Two INTA cycles run back-to-back. The device local ADDR/DATA bus is inactive during both INTA cycles. Control signals are shown for the second INTA cycle.
4. Signals at HS-82C85RH are shown for reference only.
5. Unless otherwise specified, all timing measurements are made at 1.5 V.

FIGURE 4. Timing waveforms and test circuit - Continued.

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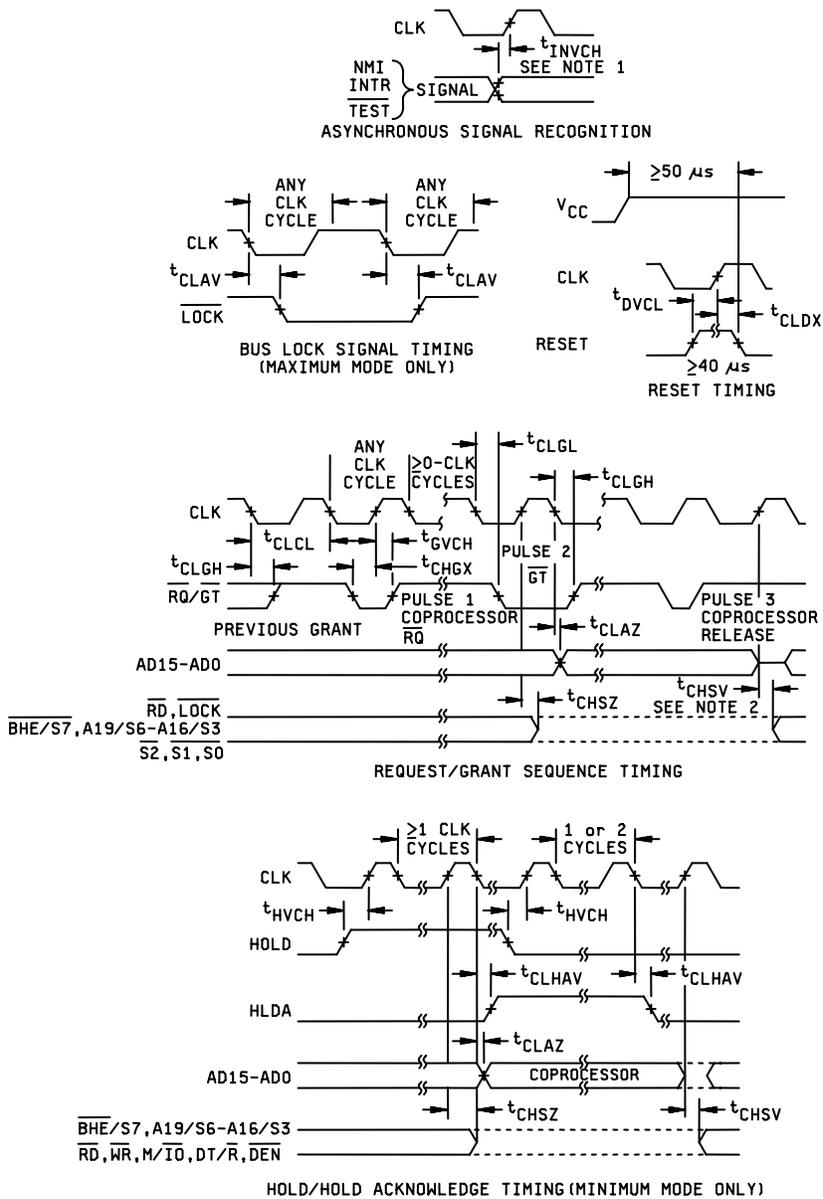


NOTES:

1. Unless otherwise specified, all signals switch between V_{OH} and V_{OL} .
2. RDY is sampled near the end of T2, T3, and TW to determine if TW machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back-to-back. The device local ADDR/DATA bus is inactive during both INTA cycles. Control for pointer address is shown for the second INTA cycle.
5. Signals at 82C85 and 82C88 are shown for reference only.
6. The issuance of the device command and control signals (\overline{MRDC} , \overline{MWTC} , \overline{AMWC} , \overline{IORC} , \overline{IOWC} , \overline{AIOWC} , \overline{INTA} and \overline{DEN}) lags the active high of 82C88 CEN.
7. Unless otherwise specified, all timing measurements are made at 1.5 V.
8. Status inactive in state just prior to T4.

FIGURE 4. Timing waveforms and test circuit - Continued.

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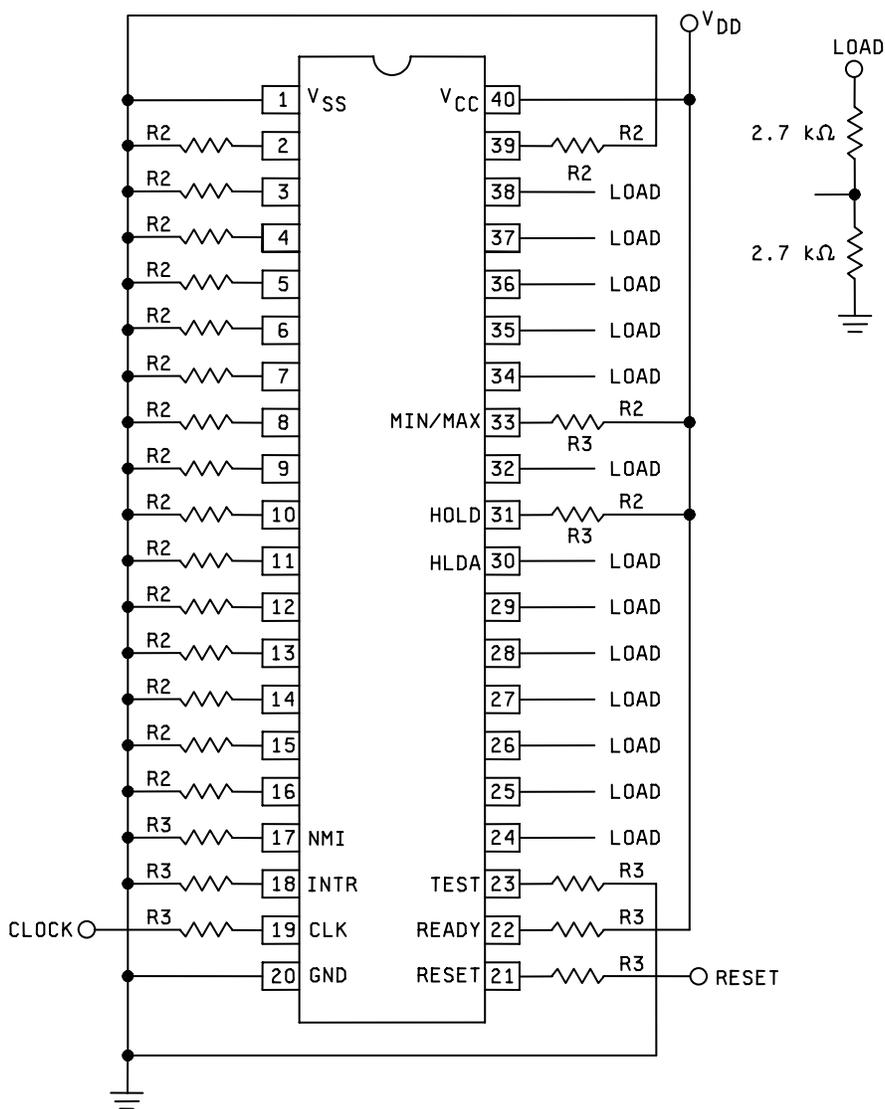


NOTES:

1. Setup requirements for asynchronous signals only to guarantee recognition at next CLK.
2. The coprocessor may not drive the busses outside the region shown without risking contention.

FIGURE 4. Timing waveforms and test circuit - Continued.

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NOTES:

1. $V_{DD} = 5.0 V \pm 0.5 V$.
2. $R2 = 3.3 k\Omega$. $R3 = 47 k\Omega$.
3. Pins tied to GND: 1-18, 20, 23, 39.
Pins tied to V_{DD} : 22, 31, 33, 40.
Pins with loads: 24-29, 30, 32, 34-38.
Pins brought out 19 (clock), 21 (reset).
4. Clock and reset should be brought out separately so they can be toggled before irradiation.

FIGURE 5. Radiation exposure circuit.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. Subgroup 4 (C_{IN} , C_{OUT} , and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/</u> <u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	<u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroups 1 and 7.

2/ PDA applies to subgroups 1, 7, and delta's.

3/ Delta limits as specified in table IIB herein shall be required where specified and the delta values shall be completed with reference to the zero hour.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter	Symbol	Delta limits
Standby power supply current	I_{DDSB}	$\pm 100 \mu A$
Output leakage current	I_{OZL}, I_{OZH}	$\pm 2 \mu A$
Input leakage current	I_{IH}, I_{IL}	$\pm 200 nA$
Low level output voltage	V_{OL}	$\pm 80 mV$
TTL high level output voltage	V_{OH1}	$\pm 600 mV$
CMOS high level output voltage	V_{OH2}	$\pm 150 mV$

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ C$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at $25^\circ\text{C} \pm 5^\circ\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 micron in silicon.
- e. The test temperature shall be $+25^\circ\text{C}$ for the upset measurements and the maximum rated operating temperature $\pm 10^\circ\text{C}$ for the latch-up measurements.
- f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.
- g. For SEP test limits, see table IB herein.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331 and as follows:

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>
AD15-AD0	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/I/O address (T1) and data (T2, T3, TW, T4) bus. A0 is analogous to BHE for the lower byte of the data bus, pins D7-D0. It is LOW during T1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight bit oriented devices tied to the lower half would normally use AD0 to condition chip select functions (see BHE). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A19/S6 A18/S5 A17/S4 A16/S3	O	ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations these lines are low. During memory and I/O operations, status information is available on these lines during T2, T3, TW, T4 • S6 is always zero. The status of the interrupt enable FLAG bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded.

This information indicates which segment register is presently being used for data accessing.

These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence".

S4	S3	Characteristics
0	0	Extra data
0	1	Stack
1	0	Code or none
1	1	Data

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6.5 Abbreviations, symbols, and definitions – Continued.

Pin symbol	Type	Description															
$\overline{\text{BHE/S7}}$	O	<p>BUS HIGH ENABLE/STATUS: During T1 the bus high enable signal ($\overline{\text{BHE}}$) should be used to enable data onto the most significant half of the data bus, pins D15-D8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{\text{BHE}}$ to condition chip select functions. $\overline{\text{BHE}}$ is LOW during T1 for read, write, and interrupt acknowledge cycles when a bytes is to be transferred on the high portion of the bus. The S7 status information is available during T2, T3, and T4. The signal is active LOW, and is held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence"; it is LOW during T1 for the first interrupt acknowledge cycle.</p> <table border="1"> <thead> <tr> <th>$\overline{\text{BHE}}$</th> <th>A0</th> <th>Characteristics</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Whole word</td> </tr> <tr> <td>0</td> <td>1</td> <td>Upper byte from/to odd address</td> </tr> <tr> <td>1</td> <td>0</td> <td>Lower byte from/to odd address</td> </tr> <tr> <td>1</td> <td>1</td> <td>None</td> </tr> </tbody> </table>	$\overline{\text{BHE}}$	A0	Characteristics	0	0	Whole word	0	1	Upper byte from/to odd address	1	0	Lower byte from/to odd address	1	1	None
$\overline{\text{BHE}}$	A0	Characteristics															
0	0	Whole word															
0	1	Upper byte from/to odd address															
1	0	Lower byte from/to odd address															
1	1	None															
$\overline{\text{RD}}$	O	<p>READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the M/I/O or $\overline{\text{S2}}$ pin. This signal is used to read devices which reside on the device local bus. $\overline{\text{RD}}$ is active LOW during T2, T3, and TW of any read cycle, and is guaranteed to remain HIGH in T2 until the device local bus has floated.</p> <p>This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence".</p>															
READY	I	<p>READY: Is the acknowledgment from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C85 clock generator to form READY. This signal is active HIGH. The device READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.</p>															
INTR	I	<p>INTERRUPT REQUEST: Is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. If so, an interrupt service routine is called via an interrupt vector lookup table located in system memory. INTR is internally synchronized and it can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.</p>															
$\overline{\text{TEST}}$	I	<p>TEST: Input is examined by the "Wait" instruction. If the $\overline{\text{TEST}}$ input is LOW execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.</p>															
NMI	I	<p>NON-MASKABLE INTERRUPT: Is an edge triggered input which causes a type 2 interrupt. An interrupt service routine is called via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.</p>															
RESET	I	<p>RESET: Causes the processor to immediately terminate its present activity. The signal must change from LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.</p>															

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6.5 Abbreviations, symbols, and definitions – Continued.

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>
CLK	I	CLOCK: Provides the basic timing for the processor and bus controller. It is asymmetric with a 33 percent duty cycle to provide optimized internal timing.
V _{DD}		V _{DD} : +5 V power supply pin. A 0.1 μF capacitor between pin 20 and pin 40 is recommended for decoupling.
GND		GND: Ground. Note: Both must be connected. A 0.1 μF capacitor between pin 1 and pin 20 is recommended for decoupling.
MN/MX	I	MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin descriptions are for the 80C86RH in Min mode (i.e. MN/MX = V_{DD}). Only the pin functions which are unique to the minimum mode are described below.

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u> - Continued.
M/I \bar{O}	O	STATUS LINE: Logically equivalent to $\bar{S}2$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/I \bar{O} becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (M = HIGH, I/O = LOW). M/I \bar{O} is held to a high impedance logic zero during local bus "hold acknowledge".
$\bar{W}R$	O	WRITE: Indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/I \bar{O} signal. $\bar{W}R$ is active for T2, T3, and TW of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\bar{I}N\bar{T}A$	O	INTERRUPT ACKNOWLEDGE: Is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and TW of each interrupt acknowledge cycle. Note that INTA is never floated.
ALE	O	ADDRESS LATCH ENABLE: Is provided by the processor to latch the address into the 82C82 address latch. It is a HIGH pulse active during clock LOW of T1 of any bus cycle. Note that ALE is never floated.
DT/ \bar{R}	O	DATA TRANSMIT/RECEIVE: Is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/ \bar{R} is equivalent to $\bar{S}1$ in maximum mode, and its timing is the same as for M/I \bar{O} (T = HIGH, R = LOW). DT/ \bar{R} is held to a high impedance logic one during local bus "hold acknowledge".
$\bar{D}EN$	O	DATA ENABLE: Provided as an output enable for a bus transceiver in a minimum system which uses the transceiver. $\bar{D}EN$ is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle it is active from the middle of T2 until the middle of T4, while for a write cycle it is active from the beginning of T2 until the middle of T4 • $\bar{D}EN$ is held to a high impedance logic one during local bus "hold acknowledge".

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6.5 Abbreviations, symbols, and definitions – Continued.

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>
HOLD HLDA	I O	HOLD: Indicates that another master is requesting a local bus "hold". To be a acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T4 or T1 clock cycle. Simultaneously with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time. The following pin functions are for the device system in maximum mode (i.e. MN/MX = GND). Only the pin functions which are unique to maximum mode are described below.

$\overline{S_0}, \overline{S_1}, \overline{S_2}$	O	STATUS: Is active during T4, T1, and T2 and is returned to the passive state (1, 1, 1) during T3 or during TW when READY is HIGH. This status is used by the 82C88 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}, \overline{S_1}$, or $\overline{S_0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a 8 μ s cycle. These status lines are encoded.
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These signals are held at a high impedance logic one state during "grant sequence".

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Characteristics
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

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6.5 Abbreviations, symbols, and definitions – Continued.

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>
$\overline{RQ/GT0}$ $RQ/GT1$	I/O	<p>REQUEST/GRANT: Pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bi-directional with $\overline{RQ/GT0}$ having higher priority than $RQ/GT1$. $\overline{RQ/GT}$ has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ/GT}$ sequence timing).</p> <ol style="list-style-type: none"> 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the device (pulse 1). 2. During a T4 or T1 clock cycle, a pulse 1 CLK wide from the device to the requesting master (pulse 2) indicates that the device has allowed the bus to float and that it will enter the "grant sequence" state at next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse 1 CLK wide from the requesting master indicates to the device (pulse3) that the "hold" request is about to end and that the device can reclaim the local bus at the next CLK. The CPU then enters T4 (or T1 if no bus cycles pending). <p>Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low.</p> <p>If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met:</p> <ol style="list-style-type: none"> 1. Request occurs on or before T2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. <p>If the local bus is idle when the request is made the two possible events will follow:</p> <ol style="list-style-type: none"> 1. Local bus will be released during the next cycle. 2. A memory cycle will start within three clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
\overline{LOCK}	O	<p>LOCK: Output indicates that other system bus masters are not to gain control of the system bus while LOCK is active LOW. The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a HIGH impedance logic one state during "grant sequence". In MAX mode, LOCK is automatically generated during T2 of the first INTA cycle and removed during T2 of the second INTA cycle.</p>

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6.5 Abbreviations, symbols, and definitions – Continued.

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>															
QS1, QS0	O	<p>QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed.</p> <p>QS1 and QS2 provide status to allow external tracking of the internal device instruction queue. Note that QS1, QS0 never become high impedance.</p> <table border="1"> <thead> <tr> <th>QS1</th> <th>QS0</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>No operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>First byte of Op code from queue</td> </tr> <tr> <td>1</td> <td>0</td> <td>Empty the queue</td> </tr> <tr> <td>1</td> <td>1</td> <td>Subsequent byte from queue</td> </tr> </tbody> </table>	QS1	QS0		0	0	No operation	0	1	First byte of Op code from queue	1	0	Empty the queue	1	1	Subsequent byte from queue
QS1	QS0																
0	0	No operation															
0	1	First byte of Op code from queue															
1	0	Empty the queue															
1	1	Subsequent byte from queue															

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When specified in the purchase order or contact, a copy of the following additional data shall be supplied.

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Number of upsets (SEP).
- d. Number of transients (SEP).
- e. Occurrence of latch-up (SEP).

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DATE: 07-05-25

Approved sources of supply for SMD 5962-95722 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9572201QQC	34371	HS1-80C86RH-8
5962R9572201VQC	34371	HS1-80C86RH-Q
5962R9572201QXC	34371	HS9-80C86RH-8
5962R9572201VXC	34371	HS9-80C86RH-Q

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

Vendor name
and address

34371

Intersil Corporation
1650 Robert J. Conlan Blvd
Palm Bay, FL 32905

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.