

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R127-98.	98-07-08	Monica L. Poelking
B	Update boilerplate to current MIL-PRF-38535 requirements and to include radiation hardness assurance requirements. - LTG	07-04-17	Thomas M. Hess
C	Update radiation features in section 1.5 and SEP test table IB. Remove class M requirements throughout. Update boilerplate paragraphs to current MIL-PRF-38535 requirements. - MAA	15-07-15	Thomas M. Hess



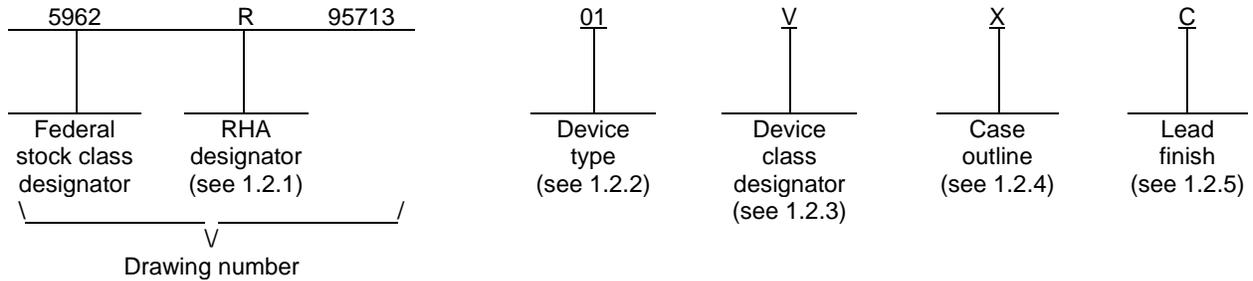
REV																				
SHEET																				
REV	C																			
SHEET	15																			
REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	PREPARED BY Thomas M. Hess	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil/</p> <p>MICROCIRCUIT, DIGITAL, RADIATION HARDENED CMOS PROGRAMMABLE INTERVAL TIMER, MONOLITHIC SILICON</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Thomas M. Hess																		
	APPROVED BY Monica L. Poelking																		
	DRAWING APPROVAL DATE 96-01-16																		
	REVISION LEVEL C	SIZE A	CAGE CODE 67268	5962-95713															
SHEET 1 OF 15																			

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	82C54RH	Radiation hardened CMOS programmable interval timer

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
X	CDFP4-F24	24	Ceramic flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

Supply voltage (V _{DD})	+7.0 V dc
Input or output voltage range	V _{SS} -0.3 V dc to V _{DD} +0.3 V dc
Storage temperature range (T _{STG}).....	-65°C to +150°C
Junction temperature (T _J).....	+175°C
Thermal resistance, junction-to-case (θ _{JC})	
Case J	+6°C/W
Case X.....	+4°C/W
Thermal resistance, junction-to-ambient (θ _{JA})	
Case J	+40°C/W
Case X.....	+60°C/W
Maximum package power dissipation at T _A = +125°C (P _D) 2/	
Case J	+1.25 W
Case X.....	+0.83 W
Maximum lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Operating supply voltage range (V _{DD})	4.5 V dc to +5.5 V dc
Operating temperature range (T _A).....	-55°C to +125°C
Input low voltage range (V _{IL})	0 V dc to +0.8 V dc
Input high voltage range (V _{IH})	V _{DD} -1.5 V dc to V _{DD}

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	100 krads(Si)
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.2)	≤ 60 MeV/(mg/cm ²) 3/
No SEU occurs at effective LET (see 4.4.4.2).....	≤ 22 MeV/(mg/cm ²) 3/

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at a rate of 25.0 mW/°C for case J and 16.7 mW/°C for case X.
- 3/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at <http://www.astm.org> or from: ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as specified on figure 3.

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3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein .

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TTL output current, high	I _{OH1}	V _{DD} = 4.5 V, V _O = 3.0 V V _{IN} = 0 V or 4.5 V	1, 2, 3	All	-2.5		mA
CMOS output current, high	I _{OH2}	V _{DD} = 4.5 V, V _O = 4.1 V V _{IN} = 0 V or 4.5 V	1, 2, 3	All	-100		μA
Output current, low	I _{OL}	V _{DD} = 4.5 V, V _O = 0.4 V V _{IN} = 0 V or 4.5 V	1, 2, 3	All	2.5		mA
Input leakage current, high	I _{IH}	V _{DD} = 5.5 V, V _{IN} = 0 V or 5.5 V Pins: 9, 11, 14-16, 18-23	1, 2, 3	All	-1.0	1.0	μA
Input leakage current, low	I _{IL}				-1.0	1.0	
Output leakage current, high	I _{OZH}	V _{DD} = 5.25 V, V _{IN} = 0 V or 5.5 V Pins: 1-8	1, 2, 3	All	-10	10	μA
Output leakage current, low	I _{OZL}				-10	10	
Standby power supply current	I _{DDSB}	V _{DD} = 5.5 V, V _{IN} = GND or V _{DD} I _O = 0 mA, Counters programmed	1, 2, 3	All		20.0	μA
Operating power supply current	I _{DDOP}	V _{DD} = 5.5 V, V _{IN} = GND or V _{DD} I _O = 0 mA CLK0 = CLK1 = CLK2 = 5 MHz	1, 2, 3	All		12.0	mA
Input capacitance	C _{IN}	See 4.4.1c V _{DD} = open, f = 1 MHz Measurement referenced to GND	4	All		15	pF
Output capacitance	C _{OUT}	See 4.4.1c V _{DD} = open, f = 1 MHz Measurement referenced to GND	4	All		15	pF
I/O capacitance	C _{I/O}	See 4.4.1c V _{DD} = open, f = 1 MHz Measurement referenced to GND	4	All		20	pF
Functional tests		See 4.4.1b V _{DD} = 4.5 V and 5.5 V V _{IN} = GND or V _{DD} , f = 1 MHz	7, 8	All			
Noise immunity functional tests		See 4.4.1b V _{DD} = 5.5 V V _{IN} = GND or V _{DD} - 1.5 V and V _{DD} = 4.5 V V _{IN} = 0.8 V or V _{DD}	7, 8	All			
Address stable before \overline{RD}	t _{AVRL}	V _{DD} = 4.5 V and 5.5 V	9, 10, 11	All	75		ns
\overline{CS} stable before \overline{RD}	t _{SLRL}		9, 10, 11	All	0		ns
Address hold time after \overline{RD}	t _{RHAX}		9, 10, 11	All	0		ns
\overline{RD} pulse width	t _{RLRH}		9, 10, 11	All	240		ns
Data delay from \overline{RD}	t _{RLDV}		9, 10, 11	All		200	ns
Command recovery time	t _{RHRL}		9, 10, 11	All	320		ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
WRITE CYCLE							
Address stable before \overline{WR}	t _{AVWL}	V _{DD} = 4.5 V and 5.5 V	9, 10, 11	All	0		ns
\overline{CS} stable before \overline{WR}	t _{SLWL}		9, 10, 11	All	0		ns
Address hold time after \overline{WR}	t _{WHAX}		9, 10, 11	All	0		ns
\overline{WR} pulse width	t _{WLWH}		9, 10, 11	All	240		ns
Data setup time before \overline{WR}	t _{DVWH}		9, 10, 11	All	225		ns
Data hold time after \overline{WR}	t _{WHDX}		9, 10, 11	All	35		ns
Command recovery time	t _{WHWL}		9, 10, 11	All	320		ns

CLOCK AND GATE

Clock period	t _{CLCL}	V _{DD} = 4.5 V and 5.5 V	9, 10, 11	All	200		ns
High pulse width	t _{CHCL}		9, 10, 11	All	100		ns
Low pulse width	t _{CLCH}		9, 10, 11	All	100		ns
Gate width high	t _{GHGL}		9, 10, 11	All	80		ns
Gate width low	t _{GLGH}		9, 10, 11	All	80		ns
Gate setup time to CLK	t _{GVCH}		9, 10, 11	All	80		ns
Gate hold time after CLK	t _{CHGX}		9, 10, 11	All	80		ns
Output delay from CLK	t _{CLOV}		9, 10, 11	All		240	ns
Output delay from gate	t _{GLOV}		9, 10, 11	All		200	ns
Data delay from address read	t _{AVAV}		9, 10, 11	All		275	ns
Output delay from \overline{WR} high	t _{WHOV}		9, 10, 11	All		260	ns

TIMING REQUIREMENTS

\overline{RD} to data float ^{2/}	t _{RHDZ}	V _{DD} = 4.5 V and 5.5 V	9, 10, 11	All	8	145	ns
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TIMING RESPONSES

Clock rise time ^{2/}	t _{CH1CH2}	V _{DD} = 4.5 V and 5.5 V 1.0 V to 3.5 V	9, 10, 11	All		25	ns
Clock fall time ^{2/}	t _{CL1CL2}	V _{DD} = 4.5 V and 5.5 V 3.5 V to 1.0 V	9, 10, 11	All		25	ns

^{1/} RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, these devices are only tested at the 'R' level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

^{2/} These parameters are controlled via design or process and are not directly tested. These parameters are characterized upon initial design and upon changes which may affect parameters.

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TABLE IB. SEP test limits. 1/ 2/

Device type	T _A = Temperature ±10°C	Bias V _{DD} = 4.5 V	Bias V _{DD} = 5.5 V for SEL test
		No SEU occur at effective LET	No SEL occurred at effective LET
All	3/	LET ≤ 22 MeV/(mg/cm ²)	LET ≤ 60 MeV/(mg/cm ²)

- 1/ Devices that contain cross-coupled resistance must be tested at the maximum T_A. For SEP test conditions, see 4.4.4.2 herein.
- 2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
- 3/ Worst case temperature for latch-up test is T_A = +125°C±10°C and for SEU test is T_A = +25°C±10°C.

Device type	01
Case outlines	J and X
Terminal number	Terminal symbol
1	D7
2	D6
3	D5
4	D4
5	D3
6	D2
7	D1
8	D0
9	CLK 0
10	OUT 0
11	GATE 0
12	GND
13	OUT 1
14	GATE 1
15	CLK 1
16	GATE 2
17	OUT 2
18	CLK 2
19	A0
20	A1
21	<u>CS</u>
22	<u>RD</u>
23	WR
24	V _{DD}

FIGURE 1. Terminal connections.

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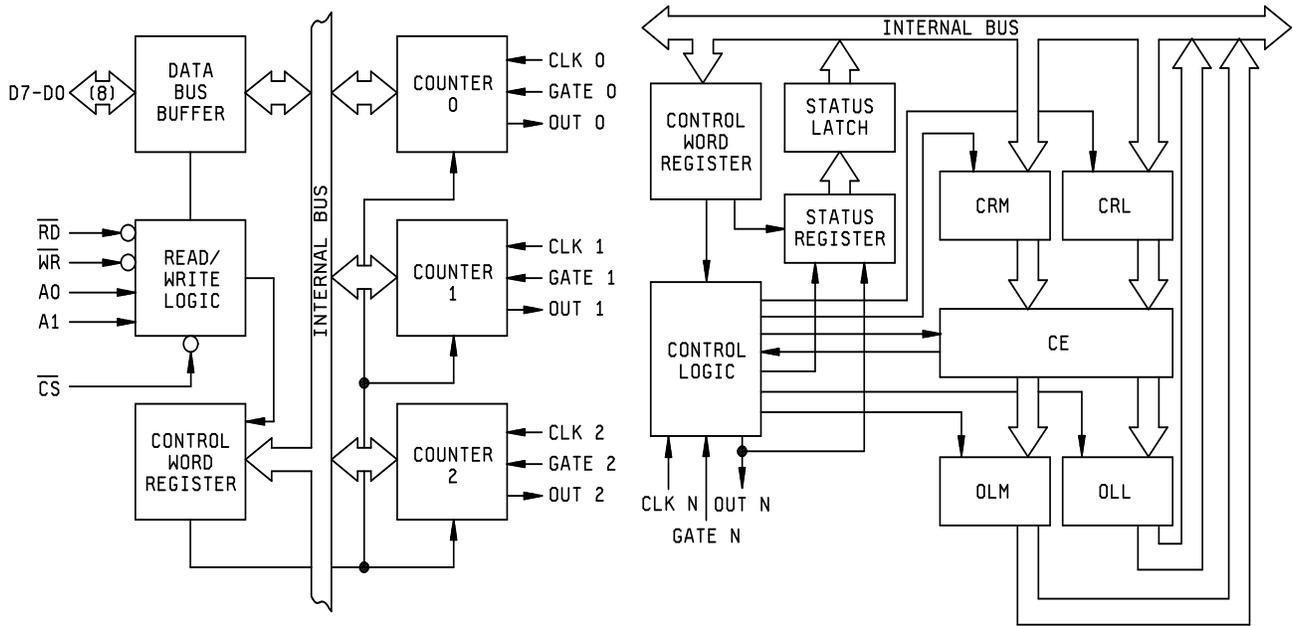


FIGURE 2. Block diagram.

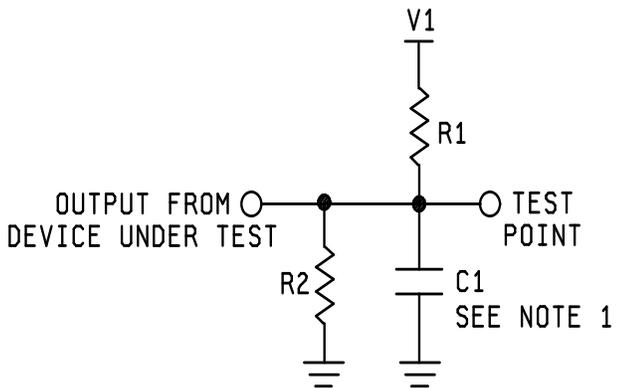
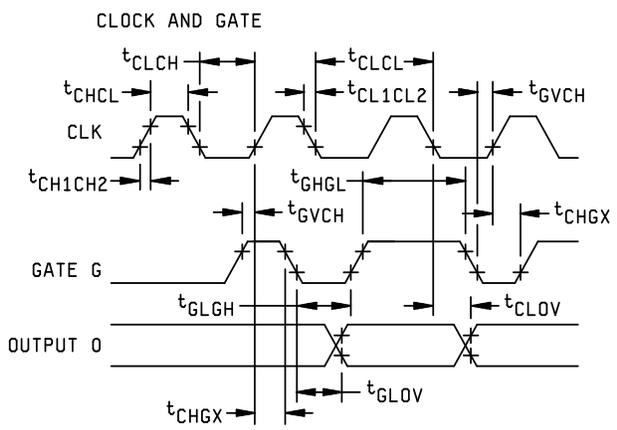
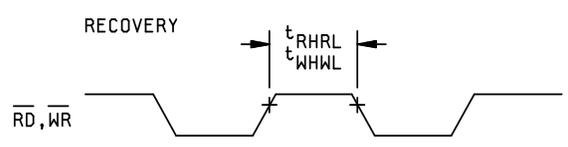
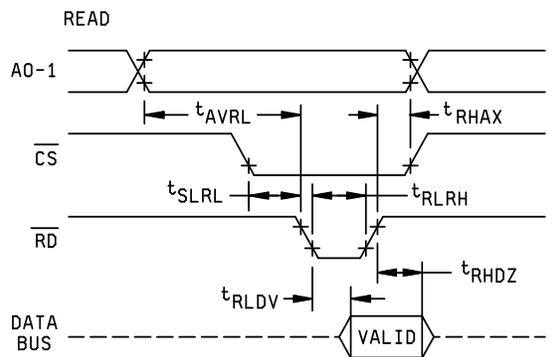
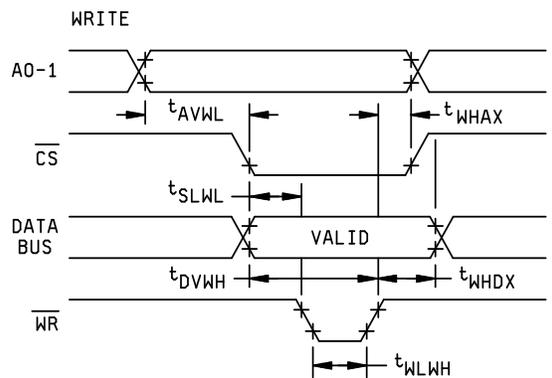
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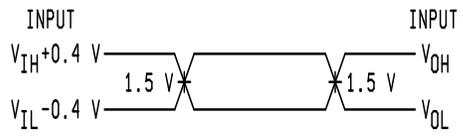
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C1 = 150 pF
 R1 = 510Ω
 V1 = 1.7 V
 R2 = open



All input signals must switch between $V_{IL} - 0.4 V$ and $V_{IH} + 0.4 V$. Input rise and fall times are driven at 1 ns/V.

NOTE:
 1. Includes stray jig capacitance.

FIGURE 3. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. Subgroup 4 (C_{IN} , C_{OUT} , and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/</u> <u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	<u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroups 1 and 7.

2/ PDA applies to subgroups 1, 7 and delta's.

3/ Delta limits as specified in table IIB herein shall be required where specified and the delta values shall be completed with reference to the zero hour.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameters	Symbols	Delta limits
Standby power supply current	I_{DDSB}	$\pm 2 \mu A$
Output leakage current	I_{OZL}, I_{OZH}	$\pm 2 \mu A$
Input leakage current	I_{IH}, I_{IL}	$\pm 200 \text{ nA}$
Output low current	I_{OL}	$\pm 500 \mu A$ or $\pm 10\%$ of initial reading, whichever is greater
TTL output high current	$I_{OH \text{ TTL}}$	$\pm 500 \mu A$ or $\pm 10\%$ of initial reading, whichever is greater
CMOS output high current	$I_{OH \text{ CMOS}}$	$\pm 20 \mu A$ or $\pm 10\%$ of initial reading, whichever is greater

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 micron in silicon.
- e. The test temperature shall be $+25^{\circ}\text{C}$ for the upset measurements and the maximum rated operating temperature $\pm 10^{\circ}\text{C}$ for the latch-up measurements.
- f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.
- g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>															
D7-D0	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.															
CLK 0	I	CLOCK 0: Clock input of counter 0.															
OUT 0	O	OUT 0: Output of counter 0.															
GATE 0	I	GATE 0: Gate input of counter 0.															
GND		GROUND: Power supply connection.															
OUT 1	O	OUT 1: Output of counter 1.															
GATE 1	I	GATE 1: Gate input of counter 1.															
CLK 1	I	CLOCK 1: Clock input of counter 1.															
GATE 2	I	GATE 2: Gate input of counter 2.															
OUT 2	O	OUT 2: Output of counter 2.															
CLK 2	I	CLOCK 2: Clock input of counter 2.															
A0, A1	I	ADDRESS: Select inputs for one of the three counters or control word register for read/write operations. Normally connected to the system address bus.															
		<table border="1"> <thead> <tr> <th><u>A1</u></th> <th><u>A0</u></th> <th><u>Selects</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Counter 0</td> </tr> <tr> <td>0</td> <td>1</td> <td>Counter 1</td> </tr> <tr> <td>1</td> <td>0</td> <td>Counter 2</td> </tr> <tr> <td>1</td> <td>1</td> <td>Control word register</td> </tr> </tbody> </table>	<u>A1</u>	<u>A0</u>	<u>Selects</u>	0	0	Counter 0	0	1	Counter 1	1	0	Counter 2	1	1	Control word register
<u>A1</u>	<u>A0</u>	<u>Selects</u>															
0	0	Counter 0															
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6.5 Abbreviations, symbols, and definitions – Continued.

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>
\overline{CS}	I	CHIP <u>SELECT</u> : A low on this input enables the device to respond to \overline{RD} and \overline{WR} signals. \overline{RD} and \overline{WR} are ignored otherwise.
\overline{RD}	I	READ: This input is low during CPU read operations.
\overline{WR}	I	WRITE: This input is low during CPU write operations.
V_{DD}		V_{DD} : The +5 V power supply pin. A 0.1 μ F capacitor between pins 12 and 24 is recommended for decoupling.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA test conditions (SEP).
- b. Number of upsets (SEU).
- c. Number of transients (SET).
- d. Occurrence of latch-up (SEL).

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-07-15

Approved sources of supply for SMD 5962-95713 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R9571301QJC	34371	HS1-82C54RH-8
5962R9571301QXC	34371	HS9-82C54RH-8
5962R9571301VJC	34371	HS1-82C54RH-Q
5962R9571301VXC	34371	HS9-82C54RH-Q

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

Vendor name and address

34371

Intersil Corporation
1650 Robert Conlan Blvd
Palm Bay, FL 32905

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.