REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add paragraph 3.1.1 and appendix A for microcircuit die. In accordance with N.O.R. 5962-R034-97.	96-11-07	R. MONNIN
B	Update boilerplate and add device class T device. Redrawn. - ro	98-12-02	R. MONNIN
C	Make changes to I_{INL}, I_{IN}, $-V_{IC}$, V_{HYST} tests and footnote 5 as specified under table I. - ro	00-04-14	R. MONNIN
D	Add vendor CAGE F8859. Changed placement of footnote 3/ in paragraph 1.5. Updated footnote 2/ in table I to accommodate RHA designator "P". Update boilerplate to reflect current requirements. -rrp	02-11-27	R. MONNIN
E	Add junction temperature to 1.3. Update drawing to reflect current requirements. –rrp	07-01-23	J. RODENBECK
F	Make change to the "DC diode input current enable pin" limit as specified under 1.3. Add Neutron testing under paragraph 4.4.4. - ro	07-04-12	R. HEBER
G	Add device type 02. Delete table III and device class M references. Make change to the physical die size under figure A-1. - ro	13-01-31	C. SAFFLE
H	Add case outline Y. Add note under figure 1. - ro	13-05-02	C. SAFFLE

REV																				
SHEET																				
REV	H	H	H	H	H	H	H	H	H											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
MICHAEL FRYE

DRAWING APPROVAL DATE
96-06-19

REVISION LEVEL
H

MICROCIRCUIT, LINEAR, RADIATION HARDENED, QUAD DIFFERENTIAL LINE RECEIVER, MONOLITHIC SILICON

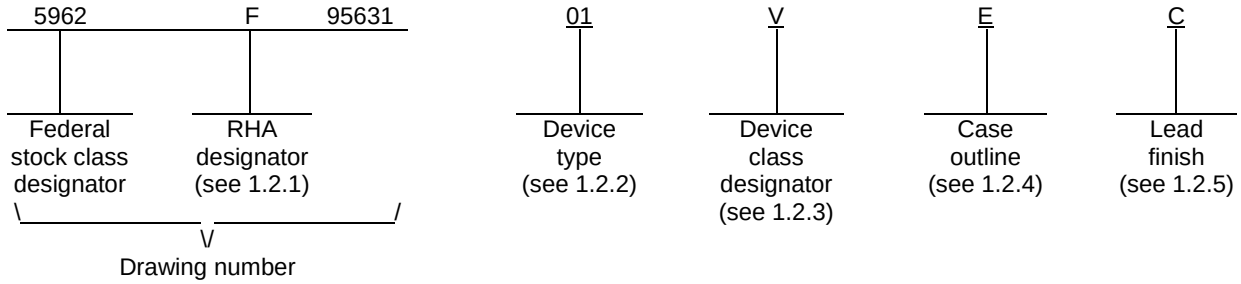
SIZE	CAGE CODE	
A	**67268**	**5962-95631**

SHEET 1 OF 23

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	26CT32RH	Radiation hardened quad differential line receiver
02	26CT32EH	Radiation hardened quad differential line receiver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	CDIP2-T16	16	Dual-in-line
X	CDFP4-F16	16	Flat pack
Y	CDFP4-F16	16	Flat pack with grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD})	-0.5 V to +7.0 V
Differential input voltage (V_{IND})	±12 V
Common mode voltage range (CMVR)	±12 V
Enable pins input voltage	-0.5 V to V_{DD} +0.5 V
DC drain current (any one output)	±25 mA
DC diode input current enable pin	±20 mA
Maximum package dissipation (P_D) (T_A = -55°C to +125°C):	
Case E	0.625 W
Cases X and Y	0.485 W
Maximum device power dissipation (P_D) (T_A = +125°C)	0.319 W 2/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case E	80°C/W
Cases X and Y	103°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+4.5 V to +5.5 V
Common mode voltage range (CMVR)	±7.0 V
Low input voltage (V_{IL})	0 V to 0.8 V, maximum
High input voltage (V_{IH})	V_{DD} to V_{DD}/2 V, minimum
Input rise and fall time	500 ns, maximum

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Maximum device power dissipation is defined as V_{DD} x I_{CC} and must withstand the added P_D due to output current test (I_O) at T_A = +125°C.

1.5 Radiation features

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):
Device type 01:
Device classes V or Q ..... 300 krads(Si) 3/
Device class T ..... 100 krads(Si) 3/
Device type 02 ..... 300 krads(Si) 4/
Maximum total dose available (dose rate ≤ 0.01 rad(Si)/s):
Device type 02..... 50 krads(Si) 4/
Single event phenomena (SEP):

No SEL occurs at effective LET (see 4.4.4.6) ..... ≤ 100 MeV/mg/cm^2 5/

Neutron irradiation ..... = 1 x 10^{14} neutrons/cm^2 5/

Dose rate induced upset ..... ≥ 5 x 10^8 rads(Si)/sec 5/

Dose rate survivability ..... = 5 x 10^{11} rads(Si)/sec 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

_____

3/ Device type 01 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si) for classes V or Q and 100 krads(Si) for device class T.
4/ Device type 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si), and condition D to a maximum total dose of 50 krads(Si).
5/ Guaranteed by process or design, not tested.

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output 3/ voltage	V_{OH}	V_{DD} = 4.5 V, 4/ V_{DIFF} = 1.0 V, I_O = -6 mA	1,2,3	01, 02	4.1		V
Low level output 3/ voltage	V_{OL}	V_{DD} = 4.5 V, 4/ V_{DIFF} = -1.0 V, I_O = 6 mA	1,2,3	01, ,02		0.4	V
Differential input voltage	V_{TH}	$V_{DD} = V_{IH}$ = 4.5 V, V_{CM} = -7.0 V to +7.0 V	1,2,3	01, 02	-400	+400	mV
Enabled high level input voltage	V_{IH}	V_{DD} = 4.5 V, 5.5 V 5/	1,2,3	01, 02	V_{DD} / 2.0		V
Enabled low level input voltage	V_{IL}	V_{DD} = 4.5 V, 5.5 V 5/	1,2,3	01, 02		0.8	V
Input current high (differential inputs)	I_{INH}	V_{DD} = 5.5 V, +V = 10 V, -V = 0 V, +V = 0 V, -V = 10 V	1,2,3	01, 02		1.8	mA
Input current low (differential inputs)	I_{INL}	V_{DD} = 5.5 V, +V = -10 V, V = 0 V, +V = 0 V, -V = -10 V	1,2,3	01, 02	-2.7		mA
Input leakage enable pins	I_{IN}	V_{DD} = 5.5 V, V_{IN} = 0 V, 5.5 V	1,2,3	01, 02	-1.0	+1.0	µA
Three-state output leakage current	I_{OZ}	V_{DD} = 5.5 V, $V_O = V_{DD}$ or GND	1,2,3	01, 02	-5.0	+5.0	µA
Standby supply current	I_{DDSB}	V_{DD} = 5.5 V, V_{DIFF} = 1.0 V, outputs = open	1,2,3	01, 02		25	mA
Enable clamp voltage	$-V_{IC}$	At -1 mA	1,2,3	01, 02	-1.5		V
	$+V_{IC}$	At 1 mA				1.5	
Input hysteresis	V_{HYST}	V_{DD} = 4.5 V, V_{IH} = 4.5 V, V_{IL} = 0 V	1,2,3	01, 02	20 6/	100	mV
Input resistance	RIN	V_{DD} = 5.5 V, V_{IH} = 5.5 V, V_{IL} = 0 V, input under test $V_{IN} = \pm 7$ V	1,2,3	01, 02	4	20	kΩ

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Fail safe voltage	F_{SAFE}	V_{OUT} = logic "1", 6/ + and - inputs are open	1,2,3	01, 02	4.1		V
Input capacitance	C_{IN}	V_{DD} = open, f = 1 MHz, T_A = +25°C, see 4.4.1d	4	01, 02		12	pF
Output capacitance	C_{OUT}	V_{DD} = open, f = 1 MHz, T_A = +25°C, see 4.4.1d	4	01, 02		12	pF
Functional testing		See 4.4.1b	7,8	01, 02			
Propagation delay time 7/	t_{PLH}, t_{PHL}	V_{DD} = 4.5 V, V_{DIFF} = 2.5 V	9,10,11	01, 02	6	40	ns
Propagation delay time 7/	t_{PZH}, t_{PZL}	V_{DD} = 4.5 V, V_{DIFF} = 2.5 V	9,10,11	01, 02	3	18	ns
Propagation delay time 7/	t_{PLZ}, t_{PHZ}	V_{DD} = 4.5 V, V_{DIFF} = 2.5 V	9,10,11	01, 02	6	29	ns
Propagation delay time 7/	t_{THL}, t_{TLH}	V_{DD} = 4.5 V, V_{DIFF} = 2.5 V	9,10,11	01	2	12	ns

1/ RHA device type 01 (device classes Q and V) supplied to this drawing will meet all levels M, D, P, L, R and F of irradiation, and device type 01 (device class T) will meet all levels M, D, P,L, R of irradiation. However, device type 01 (devices class Q and V) is only tested at the "F" or "P" levels depending on the manufacturer, and device type 01 (class T) is only tested at the "R" level in accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein).

RHA device type 02 supplied to this drawing will meet all levels M, D, P, L, R, and F of irradiation for condition A and levels M, D, P, and L for condition D. However, device type 02 is only tested at the "F" level in accordance with MIL-STD-883, method 1019, condition A and tested at the "L" level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).

Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ All voltages referenced to device ground.

3/ Force and measure functions may be interchanged.

4/ V_{IL} = 0.8 V and $V_{IN} = V_{DD}/2$.

5/ This parameter tested as inputs for the V_{OL} and V_{OH} tests.

6/ If not tested, shall be guaranteed to the limits specified in table I herein.

7/ See figures 3 and 4.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	SEP	Temperature (T_A)	V_S	Effective linear energy transfer (LET)
01	No SEL	+125°C	5.5 V	$\leq$ 100 MeV/mg/cm^2
02	No SEL	+125°C	5.5 V	$\leq$ 100 MeV/mg/cm^2

1/ For single event phenomena (SEP) test conditions, see 4.4.4.6 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but, not production tested unless specified by the customer through the purchase order or contract.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

Device types	01, 02
Case outlines	E, X and Y SEE NOTE
Terminal number	Terminal symbol
1	$\overline{\text{AIN}}$
2	AIN
3	AOUT
4	ENABLE
5	COUT
6	CIN
7	$\overline{\text{CIN}}$
8	GND
9	$\overline{\text{DIN}}$
10	DIN
11	DOUT
12	$\overline{\text{ENABLE}}$
13	BOUT
14	BIN
15	$\overline{\text{BIN}}$
16	V_{DD}

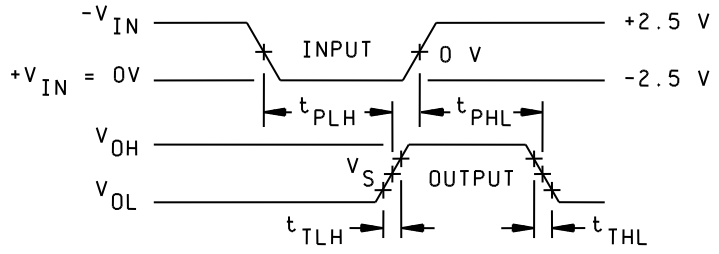
Note: For case outline Y only, the lid is grounded.

FIGURE 1. Terminal connections.

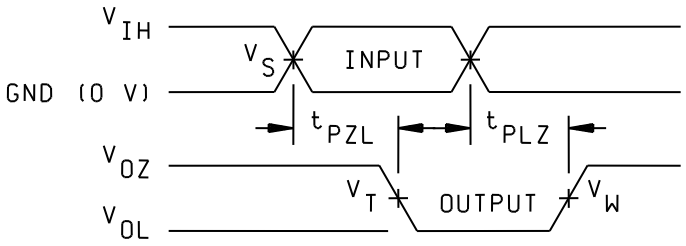
Device power	INPUTS			OUTPUT
ON / OFF	ENABLE	$\overline{\text{ENABLE}}$	INPUT	OUTPUT
ON	0	1	X	HI-Z
ON	1	X	$V_{ID} \geq V_{TH}$ (max)	1
ON	1	X	$V_{ID} \leq V_{TH}$ (min)	0
ON	X	0	$V_{ID} \geq V_{TH}$ (max)	1
ON	X	0	$V_{ID} \leq V_{TH}$ (min)	0
ON	1	X	Open	1
ON	X	0	Open	1

FIGURE 2. Truth table.

Propagation delay



Three-state

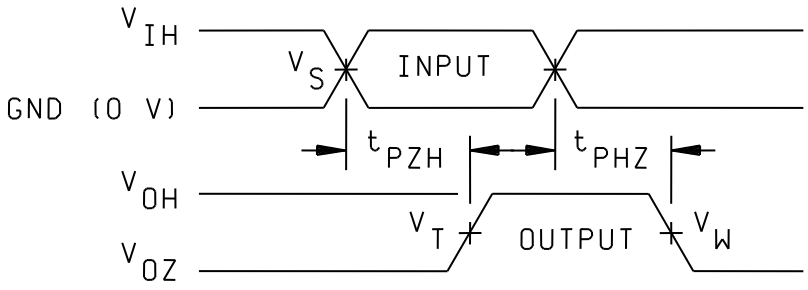


Three state low voltage levels

Parameter	Limits	Units
V_{DD}	4.50	V
V_{IH}	3.00	V
V_S	1.30	V
V_T	50	%
V_W	V_{OL} + 0.5	V
GND	0	V

FIGURE 3. Timing diagrams.

Three-state high

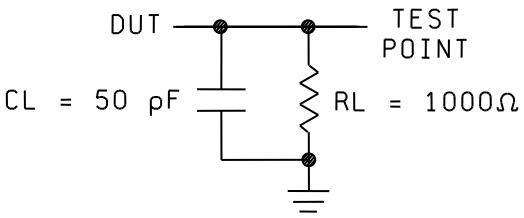


Three-state high voltage levels

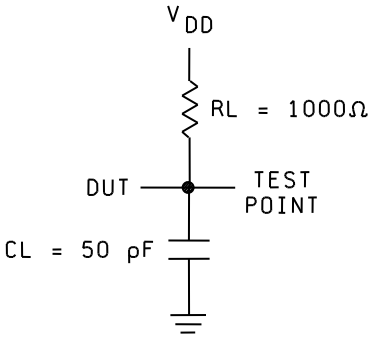
Parameters	Limits	Units
V_{DD}	4.50	V
V_{IH}	3.00	V
V_S	1.30	V
V_T	50	%
V_W	V_{OH} - 0.5	V
GND	0	V

FIGURE 3. Timing diagrams – Continued.

Propagation delay



Three-state low



Three-state high

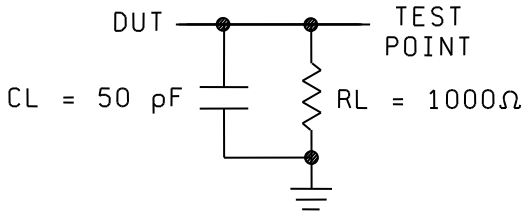


FIGURE 4. Load circuits.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,7,8, 1/ 9,10,11	1,2,3, 1/ 2/ 7,8,9,10,11	As specified in QM plan
Group A test requirements (see 4.4)	1,2,3,4, 3/ 7,8,9,10,11	1,2,3,4, 3/ 7,8,9,10,11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8, 9,10,11	1,2,3, 2/ 7,8,9,10,11	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	As specified in QM plan

1/ PDA applies to subgroup 1. For class V to subgroups 1, 7, 9, and Δ.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).
3/ Subgroup 4, if not tested, shall be guaranteed to the limits specified in table I.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/ 2/

Parameters	Symbol	Delta limits
Standby supply current	I_{DDSB}	±4 mA
Three state output leakage current	I_{OZ}	±1.0 μA
Low level output voltage	V_{OL}	±60 mV
High level output voltage	V_{OH}	±150 mV
Input leakage current	I_{IL}, I_{IH}	±150 nA

1/ Deltas are performed at room temperature.
2/ 240 hour burn-in and 1,000 hour operating group C life test.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

d. Subgroup 4 (C_{IN} and C_{OUT}) should be measured only for initial qualification and after any process or design changes which may affect input or output capacitance.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.2 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4. 2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device type 01 and 02. In addition, for device type 02 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.2.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.3 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein (see 1.5). All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25°C ± 5°C after an exposure of 2×10^{14} neutrons/cm^2 (minimum).

4.4.4.4 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.5 Dose rate upset testing. Dose rate upset testing shall be performed on a technology process, in accordance with test method 1023 of MIL-STD-883 and herein (see 1.5 herein).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the device. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q, T, and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.6 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature $\pm$10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

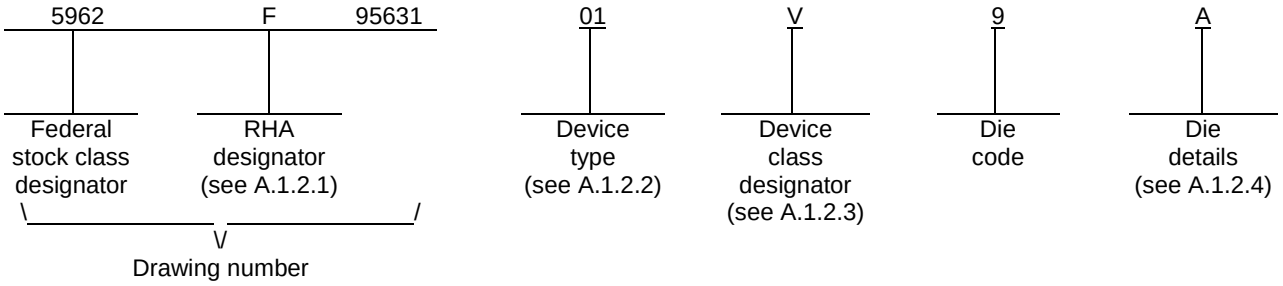
a. RHA upset levels.
b. Test conditions (SEP).
c. Number of upsets (SEU).
d. Number of transients (SET).
e. Occurrence of latchup (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-95631

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	26CT32RH	Radiation hardened quad differential line receiver
02	26CT32EH	Radiation hardened quad differential line receiver

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, 4.4.4.2.1, 4.4.4.3, 4.4.4.4, 4.4.4.5, and 4.4.4.6 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

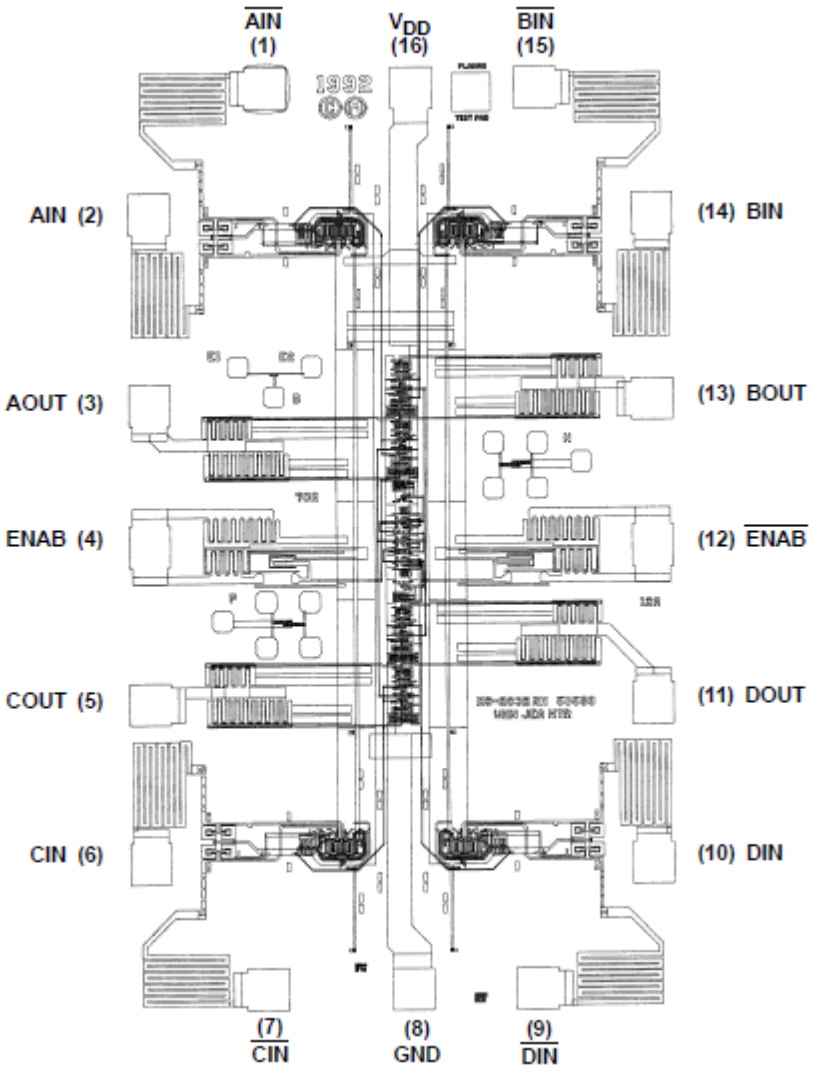
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines E, X, and Y (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.
Die size: 1970 microns x 3120 microns.
Die thickness: 21 ± 1 mils.

Interface materials.
Top metallization: Si Al Cu 10.0 kÅ ± 1 kÅ
Backside metallization: None: chemical etch

Glassivation.
Type: PSG
Thickness: 8 kÅ ± 1 kÅ

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: substrate internally tied to V_{DD}
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-05-02

Approved sources of supply for SMD 5962-95631 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962P9563101QXA	3/	26CT32K02Q
5962P9563101VXA	3/	26CT32K02V
5962P9563101QXC	3/	26CT32K01Q
5962P9563101VXC	3/	26CT32K01V
5962P9563101QEA	3/	26CT32D09Q
5962P9563101VEA	3/	26CT32D09V
5962P9563101QEC	3/	26CT32D08Q
5962P9563101VEC	3/	26CT32D08V
5962F9563101QEC	34371	HS1-26CT32RH-8
5962F9563101QXC	34371	HS9-26CT32RH-8
5962R9563101TEC	34371	HS1-26CT32RH-T
5962R9563101TXC	34371	HS9-26CT32RH-T
5962F9563101VEC	34371	HS1-26CT32RH-Q
5962F9563101VXC	34371	HS9-26CT32RH-Q
5962F9563101VYC	34371	HS9G-26CT32RH-Q
5962F9563101V9A	34371	HS0-26CT32RH-Q
5962F9563102VEC	34371	HS1-26CT32EH-Q
5962F9563102VXC	34371	HS9-26CT32EH-Q
5962F9563102V9A	34371	HS0-26CT32EH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035-6803