

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Redraw. Update drawing to current requirements. – drw	09-12-11	Charles F. Saffle

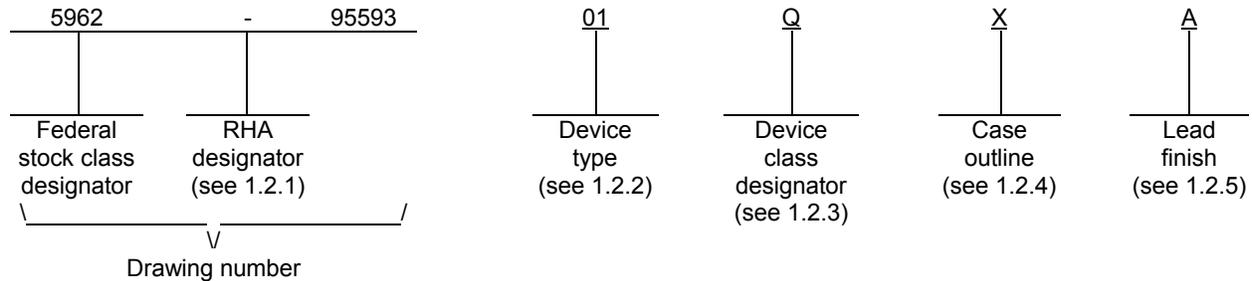
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REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	PREPARED BY Sandra Rooney	<p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil</p>																			
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY Sandra Rooney																				
	APPROVED BY Michael A. Frye																				
	DRAWING APPROVAL DATE 95-03-21																				
	REVISION LEVEL A																				
AMSC N/A	SIZE A	CAGE CODE 67268	5962-95593																		
		SHEET		1 OF 14																	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	ADC12062	12-bit, 1 MHz, 75 mW, A/D converter with input multiplexer and sample/hold

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	44	Quad flatpack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 2

1.3 Absolute maximum ratings. 1/, 2/

Supply voltage ($V_{CC} = DV_{CC} = AV_{CC}$).....	-0.3 V to +6 V
Voltage at any input or output	-0.3 V to $V_{CC} + 0.3$ V
Input current at any pin 3/	25 mA
Package input current 3/	50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Power dissipation (P_D) 4/	875 mW
Lead temperature (soldering, 10 seconds).....	+300°C
Junction temperature (T_J).....	+150°C
Thermal resistance, junction-to-case (θ_{JC}).....	7.5°C/W
Thermal resistance, junction-to-ambient (θ_{JA}).....	48°C/W

1.4 Recommended operating conditions.

Supply voltage range ($DV_{CC} = AV_{CC}$)	+4.5 V to +5.5 V
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ All voltages are measured with respect to GND (GND = AGND = DGND), unless otherwise specified.
- 3/ When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V_{CC}$) the absolute value of current at that pin should be limited to 25 mA or less. The 50 mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
- 4/ The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J max, θ_{JA} and the ambient temperature T_A . The maximum allowable power dissipation at any temperature is $P_D = (T_J \text{ max} - T_A)/\theta_{JA}$ or the number given in the absolute maximum ratings, whichever is lower. In most cases the maximum derated power dissipation will be reached only during fault conditions.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 3

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 4

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CONVERTER CHARACTERISTICS							
Resolution	RES		1, 2, 3	01		12	Bits
Differential linearity error	DLE		1	01	-0.8	+0.8	LSB
			2, 3		-0.95	+0.95	
Integral linearity error	ILE	<u>2/</u>	1	01	-1.0	+1.0	LSB
			2, 3		-1.5	+1.5	
Offset error	OE		1	01	-1.25	+1.25	LSB
			2, 3		-2.0	+2.0	
Full scale error	FSE		1	01	-1.0	+1.0	LSB
			2, 3		-1.5	+1.5	
Power supply sensitivity	PSRR	DV _{CC} = AV _{CC} = 5 V ±10%	1, 2, 3	01	-1.0	+1.0	LSB
Reference resistance	R _{REF}		1, 2, 3	01	500	1000	Ω
V _{REF+} (sense) input voltage	V _{REF+}		1, 2, 3	01		AV _{CC}	V
V _{REF-} (sense) input voltage	V _{REF-}		1, 2, 3	01	AGND		V
Input voltage range	V _{IN}	To V _{IN1} , V _{IN2} , or ADC IN	1, 2, 3	01	AGND – 0.05 V	AV _{CC} + 0.05 V	V
ADC IN input leakage	I _{INL}	AGND to AV _{CC} – 0.3 V	1, 2, 3	01		3	μA
MUX on-channel leakage	I _{ONL}	AGND to AV _{CC} – 0.3 V	1, 2, 3	01		3	μA
MUX off-channel leakage	I _{OFFL}	AGND to AV _{CC} – 0.3 V	1, 2, 3	01		3	μA

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 5

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DYNAMIC CHARACTERISTICS <u>3/</u>							
Signal-to-noise plus distortion ratio	SINAD	<u>4/</u>	4, 5, 6	01	68.0		dB
Signal-to-noise ratio	SNR	<u>4/</u> , <u>5/</u>	4, 5, 6	01	69.5		dB
Total harmonic distortion	THD	<u>4/</u> , <u>6/</u>	4	01		-74	dBc
			5, 6			-70	
Effective number of bits	ENOB	<u>4/</u> , <u>7/</u>	4, 5, 6	01	11		Bits
DC CHARACTERISTICS							
Logical 1 input voltage	V _{IN1}	DV _{CC} = AV _{CC} = +5.5 V	1, 2, 3	01	2.0		V
Logical 0 input voltage	V _{IN0}	DV _{CC} = AV _{CC} = +4.5 V	1, 2, 3	01		0.8	V
Logical 1 input current	I _{IN1}		1, 2, 3	01		1.0	μA
Logical 0 input current	I _{IN0}		1, 2, 3	01		1.0	μA
Logical 1 output voltage	V _{OUT1}	DV _{CC} = AV _{CC} = +4.5 V, I _{OUT} = -360 μA	1, 2, 3	01	2.4		V
					4.25		
Logical 0 output voltage	V _{OUT0}	DV _{CC} = AV _{CC} = +4.5 V, I _{OUT} = 1.6 mA	1, 2, 3	01		0.4	V
TRI-STATE 0 output leakage current	I _{OUT}	Pins DB0-DB11	1, 2, 3	01		3	μA
DV _{CC} supply current	DI _{CC}		1, 2, 3	01		3	mA
AV _{CC} supply current	AI _{CC}		1, 2, 3	01		12	mA

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 6

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC CHARACTERISTICS							
Maximum sampling rate (1/t _{THROUGHPUT})	f _S		9, 10, 11	01	1		MHz
Conversion time (S/H low to EOC high)	t _{CONV}		9, 10, 11	01	600	980	ns
S/H pulse width	t _{S/H}		9, 10, 11	01	5	550	ns
S/H low to EOC low	t _{EOC}		9, 10, 11	01	60	125	ns
Access time (RD low or OE high to data valid)	t _{ACC}	C _L = 100 pF	9, 10, 11	01		20	ns
TRI-STATE control (RD high or OE low databus TRI-STATE)	t _{1h} t _{0h}	R _L = 1 kΩ, C _L = 10 pF	9, 10, 11	01		40	ns
Delay from RD low to INT high	t _{INTH}	C _L = 100 pF	9, 10, 11	01		60	ns
Delay from EOC high to INT low	t _{INTL}	C _L = 100 pF	9, 10, 11	01		-10	ns
EOC high to new data valid	t _{UPDATE}		9, 10, 11	01		15	ns
Multiplexer address setup time (MUX address valid to EOC low)	t _{MS}		9, 10, 11	01	50		ns
Multiplexer address hold time (EOC low to MUX address invalid)	t _{MH}		9, 10, 11	01	50		ns
CS setup time (CS low to RD low, S/H low, or OE high)	t _{CSS}		9, 10, 11	01	20		ns
CS hold time (CS high after RD high, S/H high, or OE low)	t _{CSh}		9, 10, 11	01	20		ns

1/ DV_{CC} = AV_{CC} = +5 V, V_{REF+} (sense) = +4.096 V, V_{REF-} (sense) = AGND, and f_S = 1 MHz.

2/ Integral linearity error is the maximum deviation from a straight line between the measured offset and full scale endpoints.

3/ DV_{CC} = AV_{CC} = +5 V, V_{REF+} (sense) = +4.096 V, V_{REF-} (sense) = AGND, and f_S = 1 MHz, R_S = 25Ω, f_{IN} = 100 kHz, 0 dB from fullscale.

4/ Dynamic testing of the device is performed using the ADC IN input. The input multiplexer adds harmonic distortion at high frequencies.

5/ The signal-to-noise ratio is the ratio of the signal amplitude to the background noise level. Harmonics of the input signal are not included in its calculation.

6/ The contributions from the first nine harmonics are used in the calculation of the THD.

7/ Effective number of bits (ENOB) is calculated from the measured signal-to-noise ratio plus distortion ratio (SINAD) using the equation ENOB = (SINAD – 1.76)/6.02.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990

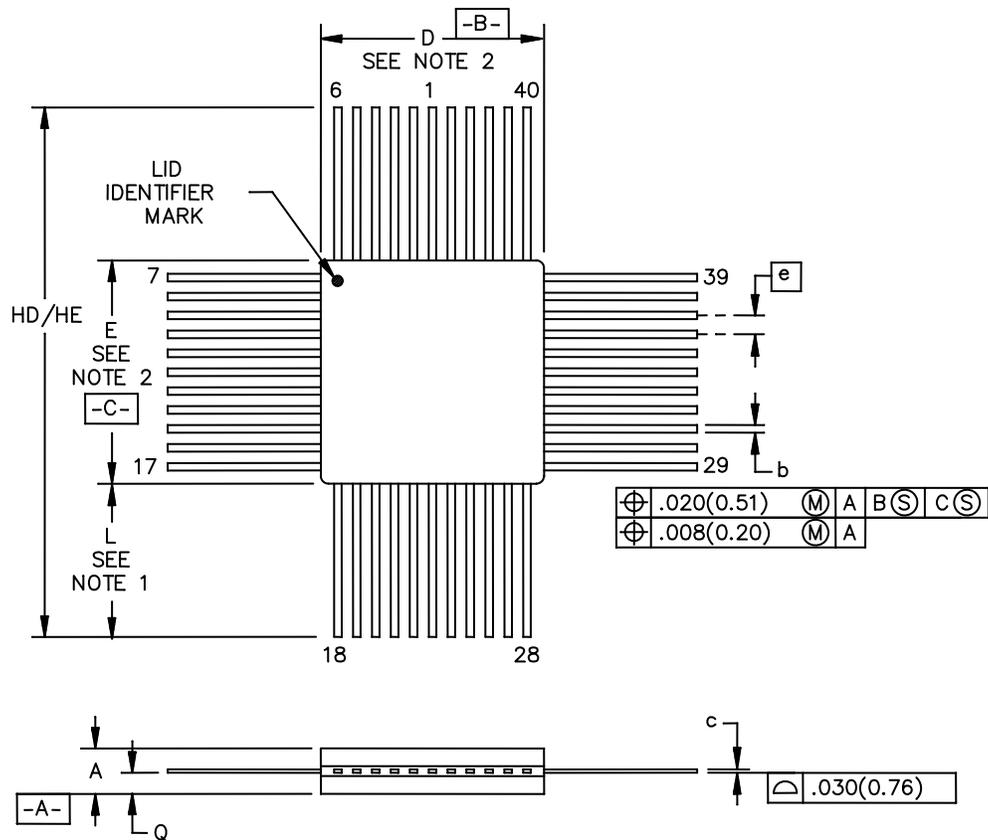
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REVISION LEVEL
A

5962-95593

SHEET

7



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.108	0.132	2.74	3.35
HD/HE	1.365	1.435	34.67	36.45
C	0.005	0.009	0.13	0.23
D/E	0.575	0.605	14.61	15.37
E	0.050 bsc		1.27 bsc	
L	0.395	0.415	10.03	10.54
Q	0.044	0.060	1.12	1.52
b	0.017	0.023	0.43	0.58

NOTES:

1. Leadframe to be solder dipped 200 microinches/5.08 micrometers minimum, measured at crest of the major flats.
2. Dimension includes the offset of base and lid.

FIGURE 1. Case outline.

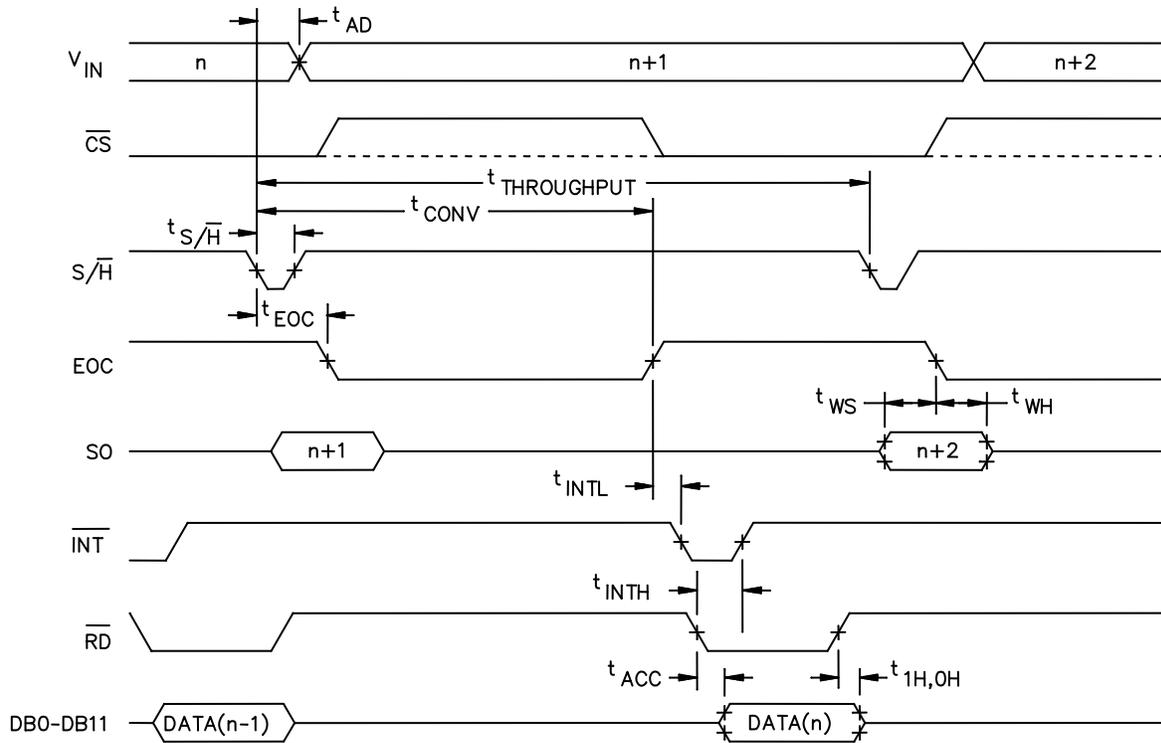
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 8

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AGND	23	$\overline{\text{CS}}$
2	V_{REF^-} (SENSE)	24	TEST
3	V_{REF^-} (FORCE)	25	DV_{CC}
4	$V_{\text{REF}}/16$	26	DGND1
5	V_{REF^+} (FORCE)	27	DGND2
6	V_{REF^+} (SENSE)	28	NC
7	$V_{\text{IN}1}$	29	$\overline{\text{INT}}$
8	NC	30	EOC
9	$V_{\text{IN}2}$	31	DB0
10	NC	32	DB1
11	MUX OUT	33	DB2
12	ADC IN	34	NC
13	AGND	35	DB3
14	AV_{CC}	36	DB4
15	DGND1	37	DB5
16	SO	38	DB6
17	$\overline{\text{PD}}$	39	DB7
18	DGND1	40	DB8
19	MODE	41	DB9
20	OE	42	DB10
21	$\overline{\text{RD}}$	43	DB11
22	$\overline{\text{S/H}}$	44	AV_{CC}

NC = no connection.

FIGURE 2. Terminal connections.

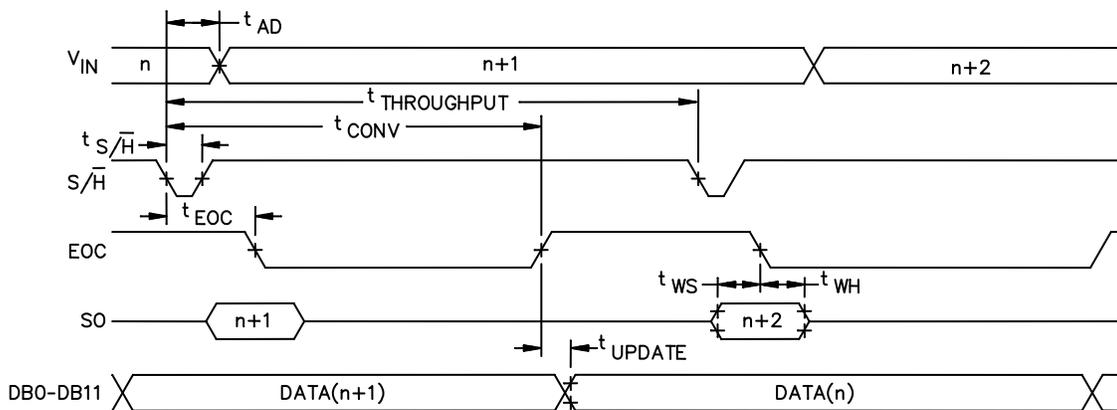
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 9



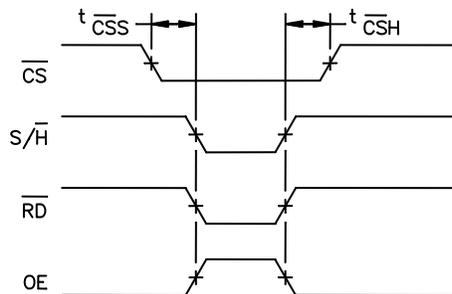
INTERRUPT INTERFACE TIMING(MODE = 1, OE = 1)

FIGURE 3. Timing diagrams.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 10



HIGH SPEED INTERFACE TIMING(MODE = 1, OE = 1, $\overline{CS} = 0$, $\overline{RD} = 0$)



\overline{CS} SETUP AND HOLD TIMING FOR S/\bar{H} , \overline{RD} , AND OE

FIGURE 3. Timing diagrams - continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 11

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 12

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>1/</u>	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>1/</u>	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>1/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	1	1	1

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 13

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95593
		REVISION LEVEL A	SHEET 14

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-12-11

Approved sources of supply for SMD 5962-95593 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9559301QXA	<u>3/</u>	ADC12062MW/883

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source. The last known supplier is listed below.

Vendor CAGE number

27014

Vendor name and address

National Semiconductor
 2900 Semiconductor Dr
 PO Box 58090
 Santa Clara, CA 95052-8090

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.