

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make changes to both $V_{OUT}$ limits under table I, Slew rate at unity gain test conditions column. Changes in accordance with N.O.R. 5962-R017-96.	96-01-10	M. A. FRYE
B	Add device type 02. Editorial and technical changes throughout.	96-02-06	M. A. FRYE
C	Make changes to $I_{IO}$ and $I_{IB}$ tests as specified under table I. - ro	00-09-20	R. MONNIN
D	Drawing updated to reflect current requirements. - gt	03-05-21	R. MONNIN
E	Delete references to device class M requirements. Updating document to current MIL-PRF-38535 requirements. - ro	14-05-27	C. SAFFLE

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REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E						
	SHEET	1	2	3	4	5	6	7	8	9	10	11								
PMIC N/A	PREPARED BY MARCIA B. KELLEHER		<b>DLA LAND AND MARITIME</b> <b>COLUMBUS, OHIO 43218-3990</b> <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a>																	
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	CHECKED BY RAJESH PITHADIA																			
	APPROVED BY MICHAEL A. FRYE																			
	DRAWING APPROVAL DATE 94-12-27																			
	REVISION LEVEL E																			
		SIZE A	CAGE CODE <b>67268</b>	<b>5962-95552</b>																
		SHEET 1 OF 11																		



1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V.

1.2.6 Device class N manufacturer PIN. For Device class N, plastic encapsulated microcircuits (PEMS) the following manufacturer PIN (see 3.5.1 herein) shall be marked:

Standard <sup>1/</sup> microcircuit drawing PIN	Manufacturer PIN
5962-9555201NXD	2272M

1.3 Absolute maximum ratings. <sup>2/</sup>

Supply voltage (+V <sub>DD</sub> ) .....	+8 V dc <sup>3/</sup>
Supply voltage (-V <sub>DD</sub> ) .....	-8 V dc
Differential input voltage (V <sub>ID</sub> ) .....	±16 V dc <sup>4/</sup>
Input voltage (V <sub>I</sub> ) .....	±8 V dc <sup>3/</sup>
Input current (I <sub>I</sub> ) .....	±5 mA
Output current (I <sub>O</sub> ) .....	±50 mA
Total current into +V <sub>DD</sub> .....	±50 mA
Total current out of -V <sub>DD</sub> .....	±50 mA
Duration of short-circuit (≤ 25°C) .....	Unlimited <sup>5/</sup>
Continuous total power dissipation (P <sub>D</sub> ) (≤ 25°C): <sup>6/</sup>	
Case H .....	675 mW
Case P .....	1050 mW
Case X .....	725 mW
Case 2 .....	1375 mW
Storage temperature range .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+260°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ):	
Cases H, P, and 2 .....	See MIL-STD-1835
Case X .....	See JEDEC Publication 95

1.4 Recommended operating conditions.

Supply voltage (±V <sub>DD</sub> ) .....	±2.2 V dc minimum to ±8 V dc maximum
Input voltage range (V <sub>I</sub> ) .....	-V <sub>DD</sub> minimum to +V <sub>DD</sub> - 1.5 V dc maximum
Common mode input voltage (V <sub>IC</sub> ) .....	-V <sub>DD</sub> minimum to +V <sub>DD</sub> - 1.5 V dc maximum
Operating free-air temperature (T <sub>A</sub> ) .....	-55°C minimum to +125°C maximum

- <sup>1/</sup> The SMD is provided for cross reference information, see 3.5.1 herein.
- <sup>2/</sup> Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- <sup>3/</sup> All voltage values except differential voltages are with respect to the midpoint between +V<sub>DD</sub> and -V<sub>DD</sub>.
- <sup>4/</sup> Differential voltages are at the non-inverting with respect to the inverting input. Excessive current will flow if input is brought below -V<sub>DD</sub> - 0.3 V.
- <sup>5/</sup> The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
- <sup>6/</sup> Above +25°C, derate at a factor of 5.8mW/°C for case X, 8.4mW/°C for case P, 5.4 mW/°C for case H and 11 mW/°C for case 2.

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation *or contract*.

### JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of this document are available online at [www.jedec.org/](http://www.jedec.org/) or from JEDEC – Solid State Technology Association, 3103 North 10<sup>th</sup> Street, Suite 240-S, Arlington, VA 22201).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions for device classes N, Q, and V shall be as specified in MIL-PRF-38535 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V <sub>IO</sub>	V <sub>DD</sub> / ±V <sub>DD</sub> = ±2.5 V, V <sub>IC</sub> = 0 V, V <sub>OUT</sub> = 0 V, R <sub>S</sub> = 50 Ω	1/	01		2500	μV
			2,3			3000	
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, V <sub>IC</sub> = 0 V, V <sub>OUT</sub> = 0 V, R <sub>S</sub> = 50 Ω	1			2500	
			2,3			3000	
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±2.5 V, V <sub>IC</sub> = 0 V, V <sub>OUT</sub> = 0 V, R <sub>S</sub> = 50 Ω	1			950	
			2,3			1500	
V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, V <sub>IC</sub> = 0 V, V <sub>OUT</sub> = 0 V, R <sub>S</sub> = 50 Ω	1		950				
	2,3		1500				
Input offset current	I <sub>IO</sub>	V <sub>DD</sub> / ±V <sub>DD</sub> = ±2.5 V, V <sub>IC</sub> = 0 V, V <sub>OUT</sub> = 0 V, R <sub>S</sub> = 50 Ω, T <sub>A</sub> = +125°C	2	All		800	pA
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, V <sub>IC</sub> = 0 V, V <sub>OUT</sub> = 0 V, R <sub>S</sub> = 50 Ω, T <sub>A</sub> = +125°C				800	
Input bias current	I <sub>IB</sub>	V <sub>DD</sub> / ±V <sub>DD</sub> = ±2.5 V, V <sub>IC</sub> = 0 V, V <sub>OUT</sub> = 0 V, R <sub>S</sub> = 50 Ω, T <sub>A</sub> = +125°C	2	All		800	pA
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, V <sub>IC</sub> = 0 V, V <sub>OUT</sub> = 0 V, R <sub>S</sub> = 50 Ω, T <sub>A</sub> = +125°C				800	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Common mode input voltage range	V <sub>ICR</sub>	V <sub>DD</sub> / ±V <sub>DD</sub> = 5 V, R <sub>S</sub> = 50 Ω,  V <sub>IO</sub>   ≤ 5 mV	1/	All	0 to 4		V
			1		0 to 3.5		
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, R <sub>S</sub> = 50 Ω,  V <sub>IO</sub>   ≤ 5 mV	1		-5 to 4		
			2,3		-5 to 3.5		
High level output voltage	V <sub>OH</sub>	V <sub>DD</sub> / ±V <sub>DD</sub> = 5 V, I <sub>OH</sub> = -200 μA	1,2,3	All	4.85		V
		V <sub>DD</sub> / ±V <sub>DD</sub> = 5 V, I <sub>OH</sub> = -1 mA			4.25		
Low level output voltage	V <sub>OL</sub>	V <sub>DD</sub> / ±V <sub>DD</sub> = 5 V, I <sub>OL</sub> = 500 μA, V <sub>IC</sub> = 2.5 V	1,2,3	All		0.15	V
		V <sub>DD</sub> / ±V <sub>DD</sub> = 5 V, I <sub>OL</sub> = 5 mA, V <sub>IC</sub> = 2.5 V				1.5	
Maximum positive peak output voltage	+V <sub>OM</sub>	V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, I <sub>O</sub> = -200 μA	1,2,3	All	4.85		V
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, I <sub>O</sub> = -1 mA			4.25		
Maximum negative peak output voltage	-V <sub>OM</sub>	V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, I <sub>O</sub> = 500 μA, V <sub>IC</sub> = 0 V	1,2,3	All	-4.85		V
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, I <sub>O</sub> = 5 mA, V <sub>IC</sub> = 0 V			-3.5		
Large signal differential voltage amplification	A <sub>VD</sub>	V <sub>DD</sub> / ±V <sub>DD</sub> = 5 V, V <sub>OUT</sub> = 1 V to 4 V, R <sub>L</sub> = 10 kΩ referenced to 2.5 V, V <sub>IC</sub> = 2.5 V	1,2,3	All	10		V/mV
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, V <sub>OUT</sub> = ±4 V, R <sub>L</sub> = 10 kΩ			20		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Common mode rejection ratio	CMRR	V <sub>DD</sub> / ±V <sub>DD</sub> = 5 V, V <sub>IC</sub> = 0 V to 2.7 V, V <sub>OUT</sub> = 2.5 V, R <sub>S</sub> = 50 Ω	1/ 1,2,3	All	70		dB
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, V <sub>IC</sub> = -5 V to 2.7 V, V <sub>OUT</sub> = 0 V, R <sub>S</sub> = 50 Ω			75		
Supply voltage rejection ratio (ΔV <sub>DD</sub> / ΔV <sub>IO</sub> )	kSVR	V <sub>DD</sub> / ±V <sub>DD</sub> = 4.4 V to 16 V, no load, V <sub>IC</sub> = V <sub>DD</sub> / 2	1,2,3	All	80		dB
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±2.2 V to ±8 V, no load, V <sub>IC</sub> = 0 V			80		
Supply current	I <sub>DD</sub>	V <sub>DD</sub> / ±V <sub>DD</sub> = 5 V, V <sub>OUT</sub> = 2.5 V, no load	1,2,3	All		3	mA
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, V <sub>OUT</sub> = 2.5 V, no load				3	
Slew rate at unity gain	SR	V <sub>DD</sub> / ±V <sub>DD</sub> = 5 V, V <sub>OUT</sub> = 1.25 V to 2.75 V, R <sub>L</sub> = 10 kΩ and C <sub>L</sub> = 100 pF referenced to 2.5 V	1	All	2.3		V/μs
			2,3		1.7		
		V <sub>DD</sub> / ±V <sub>DD</sub> = ±5 V, V <sub>OUT</sub> = ±1.0 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF	1		2.3		
			2,3		1.7		

1/ All subgroup 3 (-55°C) test limits are guaranteed but not tested.

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Device types	01 and 02		
Case outlines	H	X and P	2
Terminal number	Terminal symbol		
1	NC	COMP1 OUT	NC
2	COMP 1 OUT	COMP1 –IN	COMP1 OUT
3	COMP1 –IN	COMP1 +IN	NC
4	COMP +IN	-V <sub>DD</sub> / GND	NC
5	-V <sub>DD</sub> / GND	COMP2 +IN	COMP1 –IN
6	COMP2 +IN	COMP2 –IN	NC
7	COMP2 –IN	COMP2 OUT	COMP1 +IN
8	COMP2 OUT	+V <sub>DD</sub>	NC
9	+V <sub>DD</sub>	---	NC
10	NC	---	-V <sub>DD</sub> / GND
11	---	---	NC
12	---	---	COMP2 +IN
13	---	---	NC
14	---	---	NC
15	---	---	COMP2 –IN
16	---	---	NC
17	---	---	COMP2 OUT
18	---	---	NC
19	---	---	NC
20	---	---	+V <sub>DD</sub>

NC = No connection

FIGURE 1. Terminal connections.

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3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. A certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

#### 4. VERIFICATION

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

##### 4.2.1 Additional criteria.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified.

##### 4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1,2,3 <u>1/</u>	1,2,3 <u>1/</u>	1,2,3 <u>1/</u>
Group A test requirements (see 4.4)	1,2,3	1,2,3	1,2,3
Group C end-point electrical parameters (see 4.4)	---	1	1
Group D end-point electrical parameters (see 4.4)	---	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1 with the exception for input offset voltage ( $V_{IO}$ ) test.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. The devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ , after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply. Sources of supply for device classes N, Q, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-05-27

Approved sources of supply for SMD 5962-95552 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>	Manufacturer PIN
5962-9555201NXD	01295	TLC2272MDQ	2272M
5962-9555201QHA	01295	TLC2272MUB	---
5962-9555201QPA	01295	TLC2272MJGB	---
5962-9555201Q2A	01295	TLC2272MFKB	---
5962-9555202QHA	01295	TLC2272AMUB	---
5962-9555202QPA	01295	TLC2272AMJGB	---
5962-9555202Q2A	01295	TLC2272AMFKB	---

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

01295

Vendor name  
and address

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Ln.  
PO Box 660199  
Dallas, TX 75243  
Point of contact: U.S. Highway 75 South  
P.O. Box 84, M/S 853  
Sherman, TX 75090-9493

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