REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03 and 04. Technical and editorial changes throughout.	96-02-06	M. A. FRYE
B	Drawing updated to reflect current requirements. –ro	01-01-12	R. MONNIN
C	Make changes to I_{IO} and I_{IB} tests as specified in table I. -ro	01-01-31	R. MONNIN
D	Update drawing as part of 5 year review. -rrp	07-02-20	J. RODENBECK
E	Drawing updated to reflect current MIL-PRF-38535 requirements. Delete device class M references. - ro	14-01-28	C. SAFFLE

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			E	E	E	E	E	E	E	E	E	E	E	E		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
MICHAEL FRYE

DRAWING APPROVAL DATE
94-10-20

REVISION LEVEL
E

MICROCIRCUIT, LINEAR, RAIL-TO-RAIL, DUAL/QUAD OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

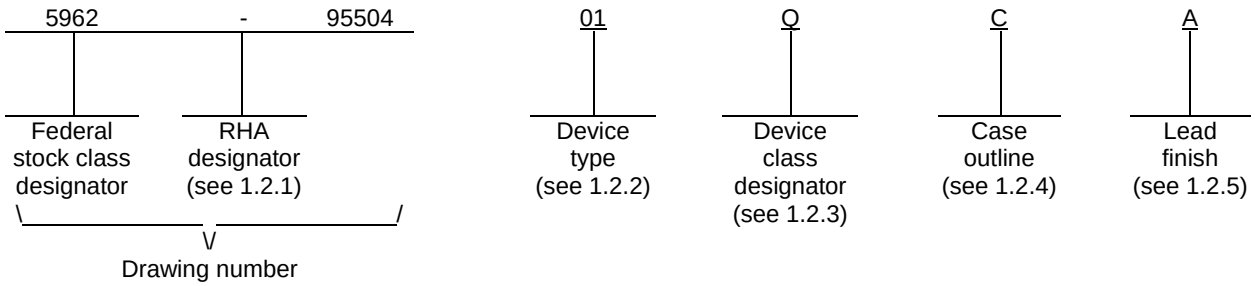
SIZE	CAGE CODE	
A	**67268**	**5962-95504**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TLV2262M	Rail-to-rail, dual, operational amplifier
02	TLV2264M	Rail-to-rail, quad, operational amplifier
03	TLV2262AM	Rail-to-rail, dual, operational amplifier with enhanced V_{IO}
04	TLV2264AM	Rail-to-rail, quad, operational amplifier with enhanced V_{IO}

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
H	GDFP1-F10 or CDFP2-F10	10	Flat pack
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.5 V dc to +8.0 V dc 2/
Differential input voltage (V_{ID})	$\pm V_{DD}$ 3/
Input voltage range (V_{IN})	$-V_{DD}$ – 0.3 V to $+V_{DD}$ 2/
Input current, each input (I_{IN})	+5.0 mA to –5.0 mA
Output current (I_{OUT})	+50.0 mA to –50.0 mA
Total current into $+V_{DD}$	+50.0 mA to –50.0 mA
Total current out of $–V_{DD}$	+50.0 mA to –50.0 mA
Duration of short-circuit current at or below +25°C	Unlimited 4/
Maximum power dissipation (P_D): 5/	
Case C and 2	1375 mW
Case D and H	700 mW
Case P	1050 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering 10 seconds)	+260°C
Maximum junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage ($\pm V_{DD}$)	2.7 V dc to 8.0 V dc
Input voltage range (V_{IN})	$-V_{DD}$ to $+V_{DD}$ – 1.3 V
Common-mode input voltage (V_{IC})	$-V_{DD}$ to $+V_{DD}$ – 1.3 V
Ambient operating temperature (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltage values, except differential voltages, are with respect to the midpoint between $+V_{DD}$ and $-V_{DD}$.

3/ Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if the input is brought below $-V_{DD}$ - 0.3 V.

4/ The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

5/ Above T_A = +25°C, derate by the following factors; cases C and 2 at 11.0 mW/°C, cases D and H at 5.5 mW/°C, and case P at 8.4 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Input offset voltage	V_{IO}	$V_{DD} = \pm 1.5$ V, $V_{IC} = 0$ V, $R_S = 50\ \Omega$, $V_{OUT} = 0$ V	1	01,02		2500	µV
				03,04		950	
			2,3	01,02		3000	
				03,04		1500	
		$V_{DD} = \pm 2.5$ V, $V_{IC} = 0$ V, $R_S = 50\ \Omega$, $V_{OUT} = 0$ V	1	01,02		2500	
				03,04		950	
			2,3	01,02		3000	
				03,04		1500	
Input offset current	I_{IO}	$V_{DD} = \pm 1.5$ V, $V_{IC} = 0$ V, $R_S = 50\ \Omega$, $V_{OUT} = 0$ V, $T_A = +125°C$	2	All		800	pA
		$V_{DD} = \pm 2.5$ V, $V_{IC} = 0$ V, $R_S = 50\ \Omega$, $V_{OUT} = 0$ V, $T_A = +125°C$				800	
Input bias current	I_{IB}	$V_{DD} = \pm 1.5$ V, $V_{IC} = 0$ V, $R_S = 50\ \Omega$, $V_{OUT} = 0$ V, $T_A = +125°C$	2	All		800	pA
		$V_{DD} = \pm 2.5$ V, $V_{IC} = 0$ V, $R_S = 50\ \Omega$, $V_{OUT} = 0$ V, $T_A = +125°C$				800	
Common-mode input voltage range	VICR	$V_{DD} = 3$ V, $\lvert V_{IO} \rvert \le 5$ mV, $R_S = 50\ \Omega$	1	All	0 to 2		V
			2,3		0 to 1.7		
		$V_{DD} = 5$ V, $\lvert V_{IO} \rvert \le 5$ mV, $R_S = 50\ \Omega$	1		0 to 4		
			2,3		0 to 3.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{DD} = 3 V, V_{IC} = 1.5 V,	1	All	2.85		V
		I_{OH} = -100 μA	2,3		2.82		
		V_{DD} = 3 V, V_{IC} = 1.5 V,	1		2.7		
		I_{OH} = -200 μA	2,3		2.6		
		V_{DD} = 5 V, V_{IC} = 2.5 V,	1		4.85		
		I_{OH} = -100 μA	2,3		4.82		
		V_{DD} = 5 V, V_{IC} = 2.5 V,	1		4.7		
		I_{OH} = -200 μA	2,3		4.5		
Low level output voltage	V_{OL}	V_{DD} = 3 V, V_{IC} = 1.5 V,	1	01,03		0.15	V
		I_{OL} = 500 μA	2,3			0.165	
			1,2,3	02,04		0.15	
		V_{DD} = 3 V, V_{IC} = 1.5 V,	1,2,3	All		0.3	
		I_{OL} = 1 mA					
		V_{DD} = 5 V, V_{IC} = 2.5 V,				0.15	
		I_{OL} = 500 μA					
		V_{DD} = 5 V, V_{IC} = 2.5 V,				0.3	
		I_{OL} = 1 mA					
Large-signal differential voltage amplification	AVD	V_{DD} = 3 V, V_{IC} = 1.5 V, 2/	1	All	60		V/mV
		V_{OUT} = 1 V to 2 V,	2,3		25		
		R_L = 50 kΩ					
		V_{DD} = 5 V, V_{IC} = 2.5 V, 2/	1		80		
		V_{OUT} = 1 V to 4 V,	2,3		50		
		R_L = 50 kΩ					

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Common-mode rejection ratio	CMRR	V_{DD} = 3 V, V_{OUT} = 1.5 V,	1	All	65		dB
		V_{IC} = 0 V to 1.7 V,	2,3		60		
		R_S = 50 Ω					
		V_{DD} = 5 V, V_{OUT} = 2.5 V,	1,2,3		70		
		V_{IC} = 0 V to 2.7 V,					
		R_S = 50 Ω					
Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	k_{SVR}	$\pm V_{DD}$ = 2.7 V to 8 V,	1,2,3	All	80		dB
		V_{IC} = V_{DD} / 2, no load					
		$\pm V_{DD}$ = 4.4 V to 8 V,			80		
		V_{IC} = V_{DD} / 2, no load					
Supply current (both channels)	I_{DD}	V_{DD} = 3 V, V_{OUT} = 1.5 V,	1,2,3	01,03		500	µA
		no load		02,04		1000	
		V_{DD} = 5 V, V_{OUT} = 2.5 V,		01,03		500	
		no load		02,04		1000	
Slew rate at unity gain	SR	V_{DD} = 3 V, R_L = 50 kΩ, 2/	4	All	0.35		V/µs
		V_{OUT} = 0.5 V to 1.7 V,	5,6		0.25		
		C_L = 100 pF					
		V_{DD} = 5 V, R_L = 50 kΩ, 2/	4		0.35		
		V_{OUT} = 0.5 V to 3.5 V,	5,6		0.25		
		C_L = 100 pF					

1/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

2/ Referenced to 1.5 V for V_{DD} = 3 V tests and 2.5 V for V_{DD} = 5 V tests.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

Device types	01,03			02,04	
Case outlines	H	P	2	C and D	2
Terminal number	Terminal symbol				
1	NC	OUTPUT 1	NC	OUTPUT 1	NC
2	OUTPUT 1	-INPUT 1	OUTPUT 1	-INPUT 1	OUTPUT 1
3	-INPUT 1	+INPUT 1	NC	+INPUT 1	-INPUT 1
4	+INPUT 1	$-V_{DD}$	NC	$+V_{DD}$	+INPUT 1
5	$-V_{DD}$	+INPUT 2	-INPUT 1	+INPUT 2	NC
6	+INPUT 2	-INPUT 2	NC	-INPUT 2	$+V_{DD}$
7	-INPUT 2	OUTPUT 2	+INPUT 1	OUTPUT 2	NC
8	OUTPUT 2	$+V_{DD}$	NC	OUTPUT 3	+INPUT 2
9	$+V_{DD}$	---	NC	-INPUT 3	-INPUT 2
10	NC	---	$-V_{DD}$	+INPUT 3	OUTPUT 2
11	---	---	NC	$-V_{DD}$	NC
12	---	---	+INPUT 2	+INPUT 4	OUTPUT 3
13	---	---	NC	-INPUT 4	-INPUT 3
14	---	---	NC	OUTPUT 4	+INPUT 3
15	---	---	-INPUT 2	---	NC
16	---	---	NC	---	$-V_{DD}$
17	---	---	OUTPUT 2	---	NC
18	---	---	NC	---	+INPUT 4
19	---	---	NC	---	-INPUT 4
20	---	---	$+V_{DD}$	---	OUTPUT 4

NC = No connection

FIGURE 1. Terminal connections.

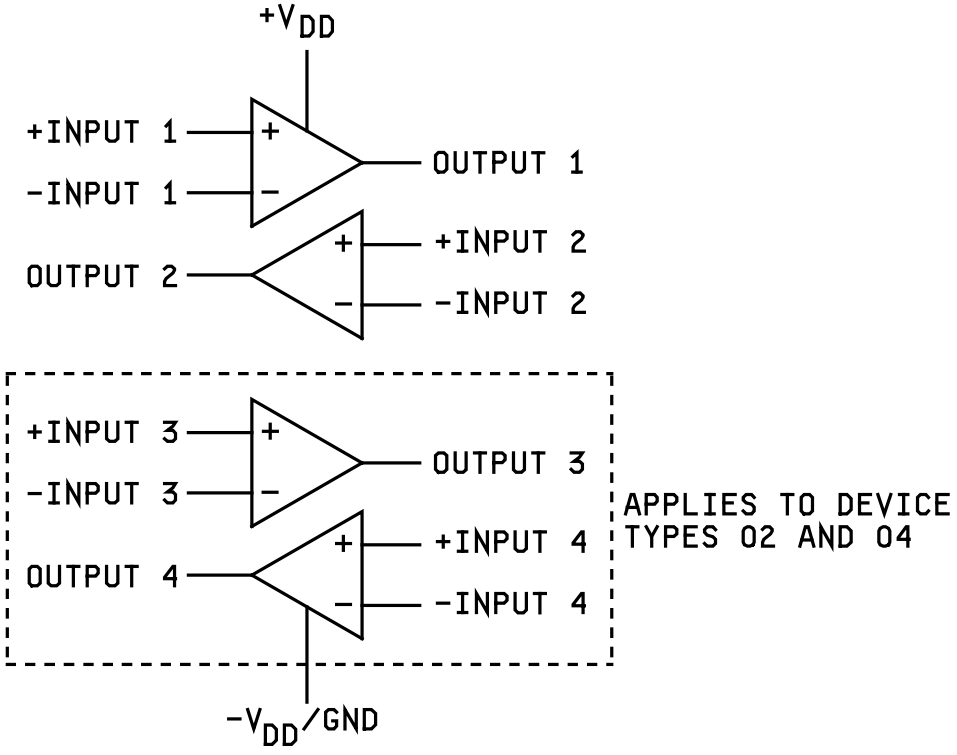


FIGURE 2. Logic diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	----	----
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/	1,2,3,4, 1/ 5,6
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1	1
Group D end-point electrical parameters (see 4.4)	1	1
Group E end-point electrical parameters (see 4.4)	---	---

1/ PDA applies to subgroup 1.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-01-28

Approved sources of supply for SMD 5962-95504 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9550401QHA	01295	TLV2262MUB
5962-9550401QPA	01295	TLV2262MJGB
5962-9550401Q2A	01295	TLV2262MFKB
5962-9550402QCA	01295	TLV2264MJB
5962-9550402QDA	01295	TLV2264MWB
5962-9550402Q2A	01295	TLV2264MFKB
5962-9550403QHA	01295	TLV2262AMUB
5962-9550403QPA	01295	TLV2262AMJGB
5962-9550403Q2A	01295	TLV2262AMFKB
5962-9550404QCA	01295	TLV2264AMJB
5962-9550404QDA	01295	TLV2264AMWB
5962-9550404Q2A	01295	TLV2264AMFKB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493