REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Added devices 07 and 08. Updated TABLE I. ksr	99-02-12	Raymond Monnin
E	Change the Y package designation, from CQCC2-F28A to CQCC2-J28 and added footnote. Updated boilerplate paragraphs. ksr	04-09-09	Raymond Monnin
F	Update drawing to current requirements. Editorial changes throughout. ksr.	09-11-30	Charles F. Saffle
G	Update drawing and RHA features in section 1.5 and SEP table IB to reflect current MIL-PRF-38535 requirements. Remove class M references. – llb	17-10-24	Charles F. Saffle
H	Update drawing to current MIL-PRF-38535 requirements. – cgh	24-08-01	James R. Eschmeyer

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets																					
REV																					
SHEET																					
REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Jeff Bowling

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
95-06-06

REVISION LEVEL
H

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ONE-TIME PROGRAMMABLE LOGIC ARRAY, (RAD-HARD), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-94754**

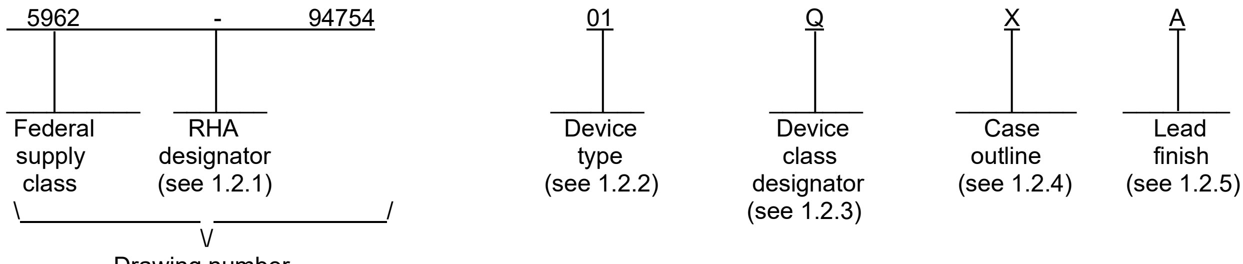
SHEET 1 OF 20

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	t_{PD}	Buffer type
01, 05	22VP10	22-input 10-output AND-OR-Logic array	25 ns	CMOS
02	22VP10	22-input 10-output AND-OR-Logic array	25 ns	TTL
03, 06	22VP10	22-input 10-output AND-OR-Logic array	20 ns	CMOS
04	22VP10	22-input 10-output AND-OR-Logic array	20 ns	TTL
07	22VP10	22-input 10-output AND-OR-Logic array	15.5 ns	CMOS
08	22VP10	22-input 10-output AND-OR-Logic array	15.5 ns	TTL

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP4-F24	24	Flat package
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line package
Y	CQCC2-J28	28	Unformed lead chip carrier package 1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Package style description indicates this package is shipped with unformed leads; optional per footnote 9 in MIL-STD-1835 for this package.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range .... -0.3 V dc to +7.0 V dc
Input voltage range .... -0.3 V dc to +7.0 V dc 4/
Output voltage applied .... -0.5 V dc to +7.0 V dc 4/
Output sink current .... 12 mA
Thermal resistance, junction-to-case (Θ_{JC}) .... See MIL-STD-1835
Maximum power dissipation (P_D) 5/ .... 1.6 W
Maximum junction temperature .... +175°C
Lead temperature (soldering, 10 seconds maximum) .... +300°C
Data retention .... 10 years (minimum)

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}) .... 4.5 V dc to 5.5 V dc 6/
High level input voltage (V_{IH}) TTL .... 2.2 V dc minimum
Low level input voltage (V_{IL}) TTL .... 0.8 V dc maximum
High level input voltage (V_{IH}) CMOS .... 0.7 x V_{DD}
Low level input voltage (V_{IL}) CMOS .... 0.3 x V_{DD}
Case operating temperature range (T_C) .... -55°C to + 125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50-300 Rad(Si)/s) .... 1M Rad(Si)
Single event phenomenon (SEP):
No SEL occurs at effective LET (see 4.4.4.4) .... ≤ 109 MeV-cm^2/mg
No SEU occurs at LET (see 4.4.4.4) .... ≤ 50 MeV-cm^2/mg

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltages referenced to V_{SS}.
4/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.
5/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
6/ See 3.10 herein for important operating requirements.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Irradiation test connections. The irradiation test connections shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.5 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.6 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.7 Programmed devices. The requirements for supplying programmed devices shall be as specified by an attached item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.6.1 Unprogrammed device deliver to the user. All testing shall be verified through group A testing as defined in 4.4.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration

3.6.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Data retention. A data retention stress test shall be completed as part of the vendor's reliability process. This test shall be done initially and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but will guarantee the number of years listed in section 1.3 herein. The vendors procedure shall be under document control and shall be made available upon request. Data retention capability shall be guaranteed over the full military temperature range.

3.10 Special operating requirement. Voltage supplied to V_{DD} pin(s) must be equal to 0V prior to the intended power-up sequence. Voltage on V_{DD} must rise from 0V to 1V at a rate of 0.1 V/s or faster, the V_{DD} rise must be continuously increasing with respect to time, through 3V, and monotonic thereafter. Following the reset, the clock input **must not** be driven from low to high until all applicable input and feedback setup times are met. Power-up voltage must meet as a minimum the V_{DD} described by the following, device dependent and temperature dependent equations.

Devices 01-04 and 08 V_{DD} = -0.0090 * (case temperature centigrade) + 4.61 V.
Devices 05, 06, and 07 V_{DD} = -0.0090 * (case temperature centigrade) + 4.41 V.

Note: The minimum V_{DD} requirements above is not applicable if the device application is purely combinatorial (i.e. no registered outputs).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	4.5 V ≤ V_{CC} ≤ 5.5 V V_{DD} = 4.5 V, I_{OH} = -12 ma TTL	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08	2.4		V
		4.5 V ≤ V_{CC} ≤ 5.5 V V_{DD} = 4.5 V, I_{OH} = -200 µA CMOS			V_{DD} – 0.05		
Low level output voltage	V_{OL}	4.5 V ≤ V_{CC} ≤ 5.5 V V_{DD} = 4.5 V, I_{OL} = 12 mA TTL	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08		0.4	V
		4.5 V ≤ V_{CC} ≤ 5.5 V V_{DD} = 4.5 V, I_{OL} = 200 µA CMOS				V_{SS} + 0.05	
High level input voltage (TTL)	V_{IH}	4.5 V ≤ V_{CC} ≤ 5.5 V	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08	2.2		V
Low level input voltage (TTL)	V_{IL}	4.5 V ≤ V_{CC} ≤ 5.5 V	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08		0.8	V
High level input voltage (CMOS)	V_{IH}	4.5 V ≤ V_{CC} ≤ 5.5 V	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08	.7 x V_{DD}		V
Low level input voltage (CMOS)	V_{IL}	4.5 V ≤ V_{CC} ≤ 5.5 V	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08		.3 x V_{DD}	V
High level input current	I_{IH}	4.5 V ≤ V_{CC} ≤ 5.5 V V_{IH} = V_{DD} CMOS	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08	-10	10	µA
		4.5 V ≤ V_{CC} ≤ 5.5 V V_{IH} = 2.4 V TTL			-10	10	
Low level input current	I_{IL}	4.5 V ≤ V_{CC} ≤ 5.5 V V_{IL} = 0.4 V TTL	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08	-10	10	µA
		4.5 V ≤ V_{CC} ≤ 5.5 V V_{IL} = GND CMOS			-10	10	
High impedance output leakage current 4/	I_{OZ}	4.5 V ≤ V_{CC} ≤ 5.5 V V_{DD} = 5.5 V, V_O = V_{DD} and V_{SS}	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08	-10	10	µA
Supply current 5/	I_{DD}	4.5 V ≤ V_{CC} ≤ 5.5 V V_{DD} = 5.5 V	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08		120	mA
Supply current (unprogrammed)	I_{DDQ}	4.5 V ≤ V_{CC} ≤ 5.5 V V_{DD} = 5.5 V	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08		25	mA
Output current short circuit 5/ 6/	I_{OS}	4.5 V ≤ V_{CC} ≤ 5.5 V V_{DD} = 5.5 V, V_O = V_{DD} V_{DD} = 5.5 V, V_O = 0 V	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08	-160	160	mA
Input capacitance	C_I 5/ 7/	4.5 V ≤ V_{CC} ≤ 5.5 V V_I = 0 V, V_{DD} = 5.0 V, T_A = +25°C, f = 1 Mhz See 4.4.1f	4	01, 02, 03, 04, 05, 06, 07, 08		15	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Bidirectional capacitance	$C_{I/O}$ 5/ 7/	$4.5 V \leq V_{CC} \leq 5.5 V$ $V_I = 0 V$, $V_{DD} = 5.0 V$, $T_A = +25°C$, f = 1 MHz See 4.4.1f	4	01, 02, 03, 04, 05, 06, 07, 08		15	pF
Functional testing		$4.5 V \leq V_{CC} \leq 5.5 V$ See 4.4.1c	7, 8A, 8B	01, 02, 03, 04, 05, 06, 07, 08			
Input to output propagation delay 5/ 8/ 9/	t_{PD}	$4.5 V \leq V_{CC} \leq 5.5 V$ See figure 4, circuit B and figure 5	9, 10, 11	01, 02, 05		25	ns
				03, 04, 06		20	
				07, 08		15.5	
Clock to output delay 5/ 9/	t_{CO}			01, 02, 03, 04, 05, 06, 07, 08		15	
Clock to combinatorial output delay via internal registered feedback 5/	t_{CO2}			01, 02, 05		28	
				03, 04, 06, 07, 08		24	
Registered clock to feedback input 5/	t_{CF}			01, 02, 03, 04, 05, 06, 07, 08		13	
Input to output enable delay 5/	t_{EA}	$4.5 V \leq V_{CC} \leq 5.5 V$ See figure 4, circuit A and figure 5		01, 02, 05		25	
				03, 04, 06, 07, 08		23	
Input to output disable 5/	t_{ER}			01, 02, 05		25	
				03, 04, 06, 07, 08		23	
Clock width, clock high time, clock 5/	t_{WH}, t_{WL}	$4.5 V \leq V_{CC} \leq 5.5 V$ See figure 4, circuit B and figure 5		01, 02, 05	14		
				03, 04, 06, 07, 08	12		
External clock period ($t_{CO} + t_S$) 5/	t_P			01, 02, 05	33		
				03, 04, 06, 07, 08	30		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input or feedback setup time 5/ 10/	t_S	$4.5 V \leq V_{CC} \leq 5.5 V$ See figure 4, circuit B and figure 5	9, 10, 11	01, 02, 05	18		ns
				03, 04, 06, 07, 08	15		
Input or feedback hold time 5/ 10/	t_H			01, 02, 03, 04, 05, 06, 07, 08	2		
Synchronous present recovery time 5/ 10/	t_{SPR}			01, 02, 05	25		
				03, 04, 06, 07, 08	20		
Power up resent time 5/ 10/	t_{PR}			01, 02, 03, 04, 05, 06, 07, 08	1		μs
External maximum frequency $1/(t_S + t_{CO})$ 5/ 10/	f_{MAX1}			01, 02, 05		30	MHz
				03, 04, 06, 07, 08		33	
Data path maximum frequency $1(t_{WH} + t_{WL})$ 5/ 10/	f_{MAX2}			01, 02, 05		36	
				03, 04, 06, 07, 08		42	
Internal feedback max frequency $1/(t_{CO} + t_{CF})$ 5/ 10/	f_{MAX3}			01, 02, 03, 04, 05, 06, 07, 08		32	
Asynchronous reset width 5/	t_{AW}			01, 02, 05	25		ns
				03, 04, 06, 07, 08	20		
Asynchronous reset recovery time 5/	t_{AR}			01, 02, 05	25		
				03, 04, 06, 07, 08	20		
Input to Asynchronous reset 5/	t_{AP}			01, 02, 05		25	
				03, 04, 06, 07, 08		0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Devices supplied to this drawing will meet levels M, D, P, L, R, F, G, and H of irradiation. However, this device is only tested at the 'H' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
2/ All voltages are referenced to ground.
3/ CMOS levels only tested on CMOS devices, TTL levels only tested on TTL devices.
4/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
5/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table IA.
6/ Only one output shorted at a time. Duration not to exceed one (1) second.
7/ All pins not being tested are to be open.
8/ Device types 07 and 08 tested at -55°C, +25°C, and +50°C. At 125°C, tested to 20 ns limit.
9/ Tested on programmed test ring only.
10/ Test applies only to registered outputs.

TABLE IB. SEP test limits. 1/ 2/

Device type	Bias V_{DD} = 4.5 V		Bias V_{CC} = 5.5 V for single event latch-up test No SEL occurs at effective LET 4/
	No upset occurs at LET 3/	Maximum device saturated cross section (LET = 120 MeV/(mg/cm^2))	
01, 02, 03, 04, 05, 06, 07, 08	LET ≤ 50 MeV/(mg/cm^2)	400 µm^2	LET_{eff} ≤ 109 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested for upsets at worse case temperature, T_A = +25° ± 10°C.
4/ Tested at worst case temperature, T_A = +125°C ± 10°C for latch-up.

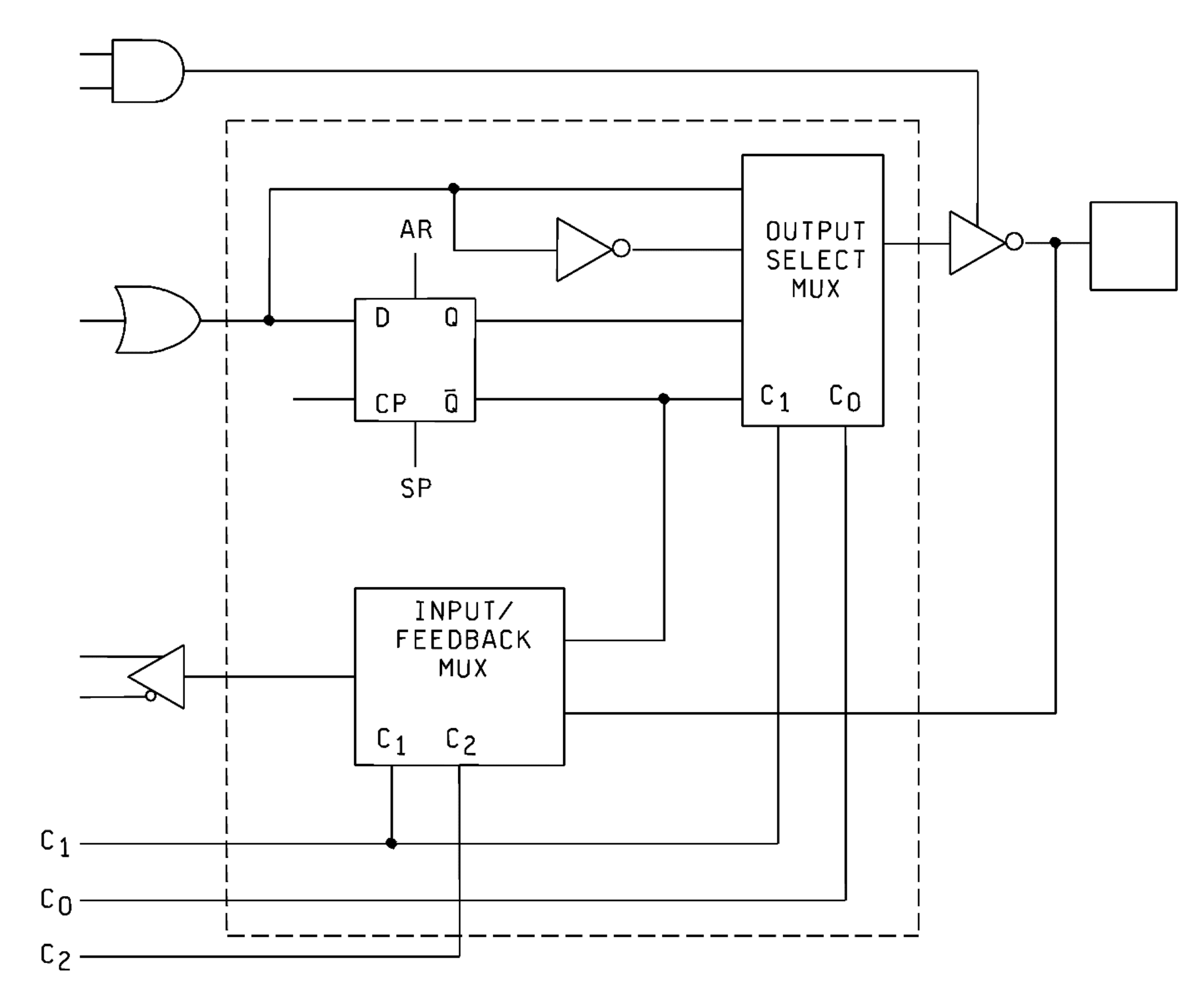
Device Types	01, 02, 03, 04, 05, 06, 07, 08	
Case Outlines	X and L	Y
Terminal Number	Terminal Symbol	
1	CK/I	V_{DD}
2	I	CK/I
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	V_{SS}
9	I	I
10	I	I
11	I	I
12	V_{SS}	I
13	I	I
14	I/O	V_{SS}
15	I/O	V_{SS}
16	I/O	I
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	V_{SS}
23	I/O	I/O
24	V_{DD}	I/O
25	- - -	I/O
26	- - -	I/O
27	- - -	I/O
28	- - -	V_{DD}

FIGURE 1. Case outline.

Truth table																						
Input pins													Output pins									
CK/I	I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1

NOTES:
1. X = Don't care
2. 1 - High

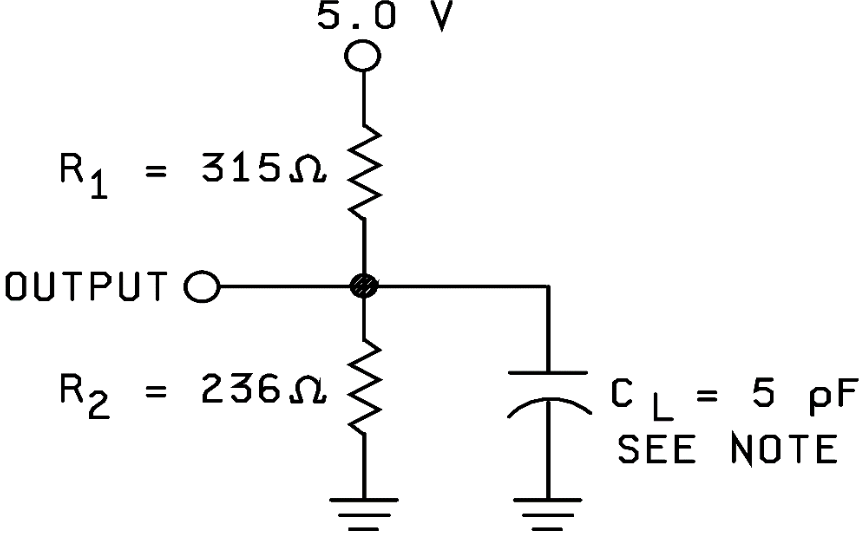
FIGURE 2. Truth table (unprogrammed).

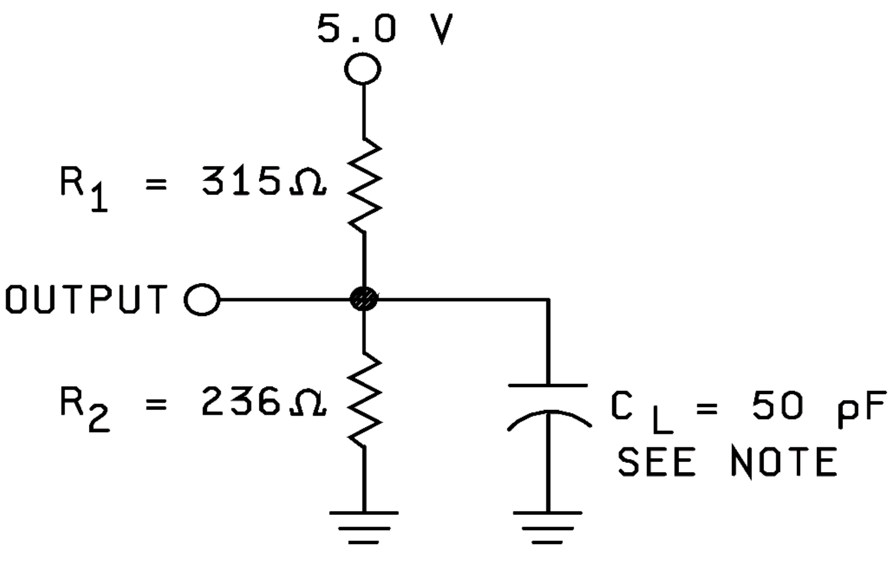


C_0	C_1	C_2	Output configuration
0	0	0	Registered feedback, reg, active low
1	0	0	Registered feedback, reg, active high
0	1	X	I/O feedback, combinatorial, active low
1	1	X	I/O feedback, combinatorial, active high
0	0	1	I/O feedback, registered, active low
1	0	1	I/O feedback, registered, active high

0 = Unblown fuse
1 = Blown fuse

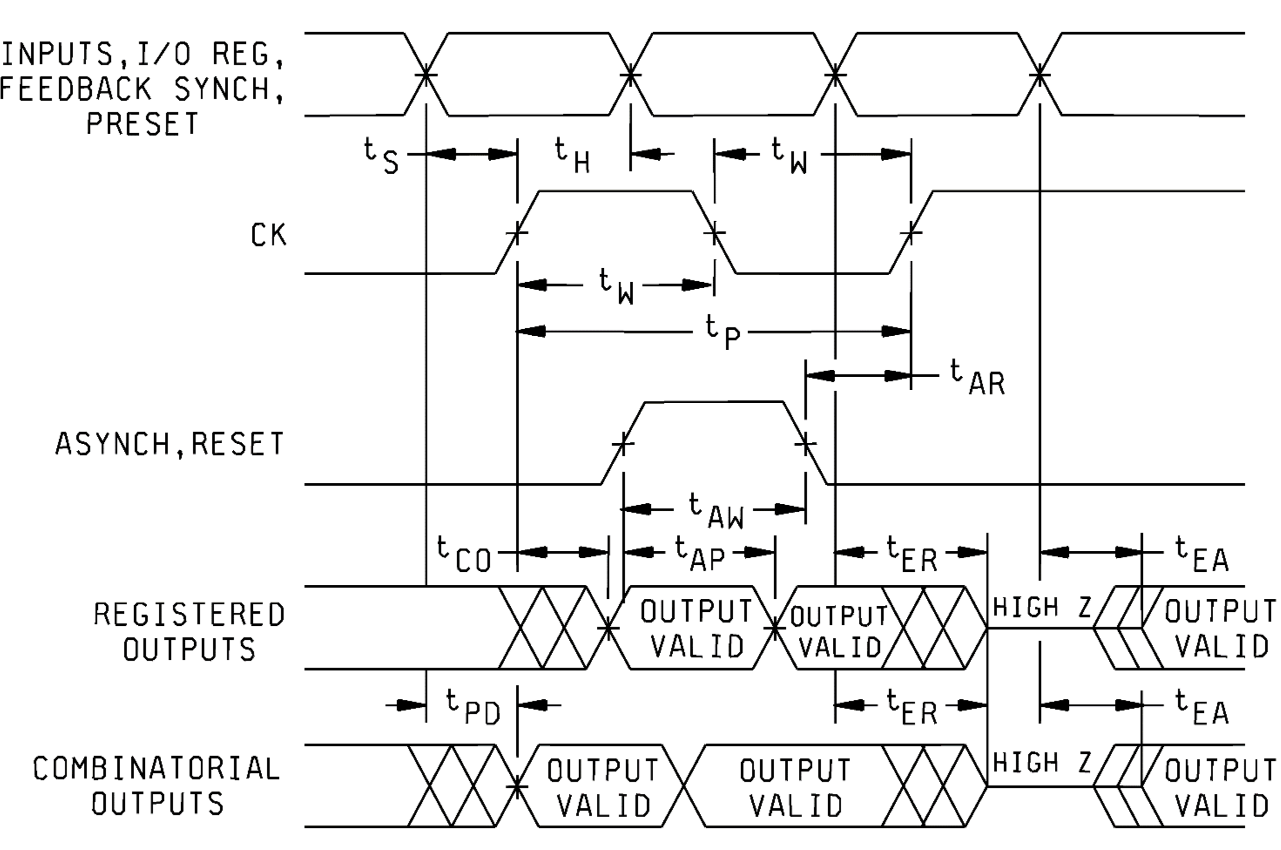
FIGURE 3. Logic diagram (unprogrammed).





NOTE: Including jig and scope (minimum value)

FIGURE 4. Output test circuit.



NOTE: Timing measurement reference is 1.5 V. Input ac driving levels are 0.0 V and 3.0 V unless otherwise specified. Input rise and fall times 3 ns maximum.

FIGURE 5. Switching waveform.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL STD 883 shall be omitted.

c. For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device.

d. Devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable: testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, 11, group A testing per MIL-STD-883, method 5005.

(1) A sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.6). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

(2) Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes, which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

f. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes, which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ± 5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9
2	Static burn-in (method 1015)	Not required	Required
3	Same as line 1		1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1		1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1f.
6/ Δ indicates delta limit (see TABLE IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{DDQ}	±20% of specified value in TABLE IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM Standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2 .

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = 4.5 V dc for the upset measurements and V_{DD} = 5.5 V dc for the latch-up measurements.

g. For SEP test limits, see table IB herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM **H** TO **L**	WILL CHANGE FROM **H** TO **L**
	CHANGE FROM **L** TO **H**	WILL CHANGE FROM **L** TO **H**
	DON’T CARE, ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-08-01

Approved sources of supply for SMD 5962-94754 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9475401Q3A	3/	22VP10C (GEN)
5962H9475401Q3C	3/	22VP10C (GEN)
5962H9475401QKA	3/	22VP10C (GEN)
5962H9475401QKC	3/	22VP10C (GEN)
5962H9475401QLA	65342	UT22VP10C-25PCA
5962H9475401QLC	65342	UT22VP10C-25PCC
5962H9475401QXA	65342	UT22VP10C-25UCA
5962H9475401QXC	65342	UT22VP10C-25UCC
5962H9475401QYA	65342	UT22VP10C-25WCA
5962H9475401QYC	65342	UT22VP10C-25WCC
5962H9475401V3A	3/	22VP10C (GEN)
5962H9475401V3C	3/	22VP10C (GEN)
5962H9475401VKA	3/	22VP10C (GEN)
5962H9475401VKC	3/	22VP10C (GEN)
5962H9475401VLA	65342	UT22VP10C-25PCA
5962H9475401VLC	65342	UT22VP10C-25PCC
5962H9475401VXA	65342	UT22VP10C-25UCA
5962H9475401VXC	65342	UT22VP10C-25UCC
5962H9475401VYA	65342	UT22VP10C-25WCA
5962H9475401VYC	65342	UT22VP10C-25WCC
5962H9475402Q3A	3/	22VP10T (GEN)
5962H9475402Q3C	3/	22VP10T (GEN)
5962H9475402QKA	3/	22VP10T (GEN)
5962H9475402QKC	3/	22VP10T (GEN)
5962H9475402QLA	65342	UT22VP10T-25PCA
5962H9475402QLC	65342	UT22VP10T-25PCC
5962H9475402QXA	65342	UT22VP10T-25UCA
5962H9475402QXC	65342	UT22VP10T-25UCC
5962H9475402QYA	65342	UT22VP10T-25WCA
5962H9475402QYC	65342	UT22VP10T-25WCC

See notes at end of table.

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9475402V3A	3/	22VP10T (GEN)
5962H9475402V3C	3/	22VP10T (GEN)
5962H9475402VKA	3/	22VP10T (GEN)
5962H9475402VKC	3/	22VP10T (GEN)
5962H9475402VLA	65342	UT22VP10T-25PCA
5962H9475402VLC	65342	UT22VP10T-25PCC
5962H9475402VXA	65342	UT22VP10T-25UCA
5962H9475402VXC	65342	UT22VP10T-25UCC
5962H9475402VYA	65342	UT22VP10T-25WCA
5962H9475402VYC	65342	UT22VP10T-25WCC
5962H9475403QLA	65342	UT22VP10C-20PCA
5962H9475403QLC	65342	UT22VP10C-20PCC
5962H9475403QXA	65342	UT22VP10C-20UCA
5962H9475403QXC	65342	UT22VP10C-20UCC
5962H9475403QYA	65342	UT22VP10C-20WCA
5962H9475403QYC	65342	UT22VP10C-20WCC
5962H9475403VLA	65342	UT22VP10C-20PCA
5962H9475403VLC	65342	UT22VP10C-20PCC
5962H9475403VXA	65342	UT22VP10C-20UCA
5962H9475403VXC	65342	UT22VP10C-20UCC
5962H9475403VYA	65342	UT22VP10C-20WCA
5962H9475403VYC	65342	UT22VP10C-20WCC
5962H9475404QLA	65342	UT22VP10T-20PCA
5962H9475404QLC	65342	UT22VP10T-20PCC
5962H9475404QXA	65342	UT22VP10T-20UCA
5962H9475404QXC	65342	UT22VP10T-20UCC
5962H9475404QYA	65342	UT22VP10T-20WCA
5962H9475404QYC	65342	UT22VP10T-20WCC
5962H9475404VLA	65342	UT22VP10T-20PCA
5962H9475404VLC	65342	UT22VP10T-20PCC

See notes at end of table.

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9475404VXA	65342	UT22VP10T-20UCA
5962H9475404VXC	65342	UT22VP10T-20UCC
5962H9475404VYA	65342	UT22VP10T-20WCA
5962H9475404VYC	65342	UT22VP10T-20WCC
5962H9475405QLA	65342	UT22VP10E-25PCA
5962H9475405QLC	65342	UT22VP10E-25PCC
5962H9475405QXA	65342	UT22VP10E-25UCA
5962H9475405QXC	65342	UT22VP10E-25UCC
5962H9475405QYA	65342	UT22VP10E-25WCA
5962H9475405QYC	65342	UT22VP10E-25WCC
5962H9475405VLA	65342	UT22VP10E-25PCA
5962H9475405VLC	65342	UT22VP10E-25PCC
5962H9475405VXA	65342	UT22VP10E-25UCA
5962H9475405VXC	65342	UT22VP10E-25UCC
5962H9475405VYA	65342	UT22VP10E-25WCA
5962H9475405VYC	65342	UT22VP10E-25WCC
5962H9475406QLA	65342	UT22VP10E-20PCA
5962H9475406QLC	65342	UT22VP10E-20PCC
5962H9475406QXA	65342	UT22VP10E-20UCA
5962H9475406QXC	65342	UT22VP10E-20UCC
5962H9475406QYA	65342	UT22VP10E-20WCA
5962H9475406QYC	65342	UT22VP10E-20WCC
5962H9475406VLA	65342	UT22VP10E-20PCA
5962H9475406VLC	65342	UT22VP10E-20PCC
5962H9475406VXA	65342	UT22VP10E-20UCA
5962H9475406VXC	65342	UT22VP10E-20UCC
5962H9475406VYA	65342	UT22VP10E-20WCA
5962H9475406VYC	65342	UT22VP10E-20WCC
5962H9475407QLA	65342	UT22VP10E-15PCA
5962H9475407QLC	65342	UT22VP10E-15PCC

See notes at end of table.

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DATE: 24-08-01

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9475407QXA	65342	UT22VP10E-15UCA
5962H9475407QXC	65342	UT22VP10E-15UCC
5962H9475407QYA	65342	UT22VP10E-15WCA
5962H9475407QYC	65342	UT22VP10E-15WCC
5962H9475407VLA	65342	UT22VP10E-15PCA
5962H9475407VLC	65342	UT22VP10E-15PCC
5962H9475407VXA	65342	UT22VP10E-15UCA
5962H9475407VXC	65342	UT22VP10E-15UCC
5962H9475407VYA	65342	UT22VP10E-15WCA
5962H9475407VYC	65342	UT22VP10E-15WCC
5962H9475408QLA	65342	UT22VP10T-15PCA
5962H9475408QLC	65342	UT22VP10T-15PCC
5962H9475408QXA	65342	UT22VP10T-15UCA
5962H9475408QXC	65342	UT22VP10T-15UCC
5962H9475408QYA	65342	UT22VP10T-15WCA
5962H9475408QYC	65342	UT22VP10T-15WCC
5962H9475408VLA	65342	UT22VP10T-15PCA
5962H9475408VLC	65342	UT22VP10T-15PCC
5962H9475408VXA	65342	UT22VP10T-15UCA
5962H9475408VXC	65342	UT22VP10T-15UCC
5962H9475408VYA	65342	UT22VP10T-15WCA
5962H9475408VYC	65342	UT22VP10T-15WCA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65342	Frontgrade Colorado Springs LLC 4350 Centennial Blvd. Colorado Springs, CO 80907-3486

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