

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. – jak	07-05-30	Thomas M. Hess
B	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	13-07-25	Thomas M. Hess
C	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - TTM	23-10-25	Muhammad A. Akbar



THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

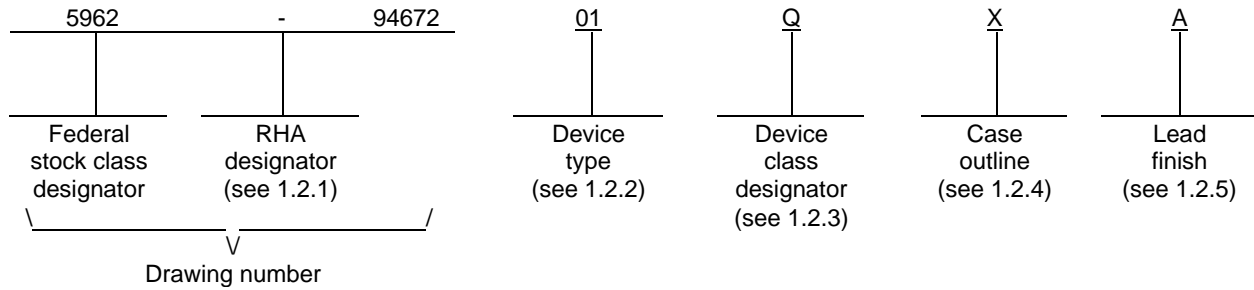
Revision Status of Sheets																						
REV	C	C	C	C	C																	
SHEET	23	24	25	26	27																	
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A																					
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE		PREPARED BY Thanh V. Nguyen					<b>DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990</b> <a href="https://www.dla.mil/LandandMaritime">https://www.dla.mil/LandandMaritime</a>														
		CHECKED BY Thanh V. Nguyen																			
		APPROVED BY Monica L. Poelking					<b>MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, SCAN TEST DEVICE WITH 18-BIT UNIVERSAL BUS TRANSCEIVER, THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON</b>														
		DRAWING APPROVAL DATE 94-06-08																			
AMSC N/A		REVISION LEVEL C					SIZE A		CAGE CODE <b>67268</b>				<b>5962-94672</b>								
										SHEET 1 OF 27											

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ABT18502	Scan test device with 18-bit universal bus transceiver, three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	68	Quad flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range ( $V_{CC}$ ).....	-0.5 V dc to +7.0 V dc
DC input voltage range (I/O ports) ( $V_{IN}$ ).....	-0.5 V dc to +5.5 V dc <u>4/</u>
DC input voltage range (except I/O ports) ( $V_{IN}$ ).....	-0.5 V dc to +7.0 V dc <u>4/</u>
DC output voltage range ( $V_{OUT}$ ).....	-0.5 V dc to +5.5 V dc <u>4/</u>
DC output current ( $I_{OL}$ ) (per output).....	+96 mA
DC input clamp current ( $I_{IK}$ ) ( $V_{IN} = < 0.0$ V).....	-18 mA
DC output clamp current ( $I_{OK}$ ) ( $V_{OUT} = < 0.0$ V).....	-50 mA
$V_{CC}$ current ( $I_{VCC}$ ).....	+582 mA
Ground current ( $I_{GND}$ ).....	+1190 mA
Storage temperature range ( $T_{STG}$ ).....	-65°C to +150°C
Lead temperature (soldering, 10 seconds).....	+300°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ).....	1.9°C/W
Junction temperature ( $T_J$ ).....	+175°C
Maximum power dissipation ( $P_D$ ).....	684 mW <u>5/</u>

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range ( $V_{CC}$ ).....	+4.5 V dc to +5.5 V dc
Input voltage range ( $V_{IN}$ ).....	+0.0 V dc to $V_{CC}$
Output voltage range ( $V_{OUT}$ ).....	+0.0 V dc to $V_{CC}$
Maximum low level input voltage ( $V_{IL}$ ).....	0.8 V
Minimum high level input voltage ( $V_{IH}$ ).....	2.0 V
Maximum high level output current ( $I_{OH}$ ).....	-24 mA
Maximum low level output current ( $I_{OL}$ ).....	+48 mA
Maximum input rise or fall rate ( $\Delta V/\Delta V$ ).....	10 ns/V
Minimum setup time ( $t_s$ ):	
mAn before mCLKAB $\uparrow$ or mBn before mCLKBA $\uparrow$ .....	4.0 ns
mAn before mLEAB $\downarrow$ or mBn before mLEBA $\downarrow$ , CLK high.....	3.5 ns
mAn before mLEAB $\downarrow$ or mBn before mLEBA $\downarrow$ , CLK low.....	2.0 ns
mAn, mBn, mCLKAB, mCLKBA, mLEAB, mLEBA, $\overline{mOEAB}$ , or $\overline{mOEBA}$	
before TCK $\uparrow$ .....	4.5 ns
TDI before TCK $\uparrow$ .....	7.5 ns
TMS before TCK $\uparrow$ .....	3.0 ns
Minimum hold time ( $t_h$ ):	
mAn after mCLKAB $\uparrow$ or mBn after mCLKBA $\uparrow$ .....	0.0 ns
mAn after mLEAB $\downarrow$ or mBn after mLEBA $\downarrow$ .....	2.0 ns
mAn, mBn, mCLKAB, mCLKBA, mLEAB, mLEBA, $\overline{mOEAB}$ , or $\overline{mOEBA}$	
after TCK $\uparrow$ .....	0.5 ns
TDI after TCK $\uparrow$ .....	0.5 ns
TMS after TCK $\uparrow$ .....	0.5 ns
Minimum pulse width: ( $t_w$ )	
mCLKAB or mCLKBA, high or low.....	3.5 ns
mLEAB or mLEBA high.....	3.5 ns
TCK high or low.....	8.0 ns
Minimum delay time, power-up to TCK $\uparrow$ ( $t_d$ ).....	50.0 ns <u>6/</u>
Minimum rise time, $V_{CC}$ power-up ( $t_r$ ).....	1 $\mu$ s <u>6/</u>
Maximum clock frequency: ( $f_{CLK}$ )	
mCLKAB or mCLKBA.....	100 MHz
TCK.....	50 MHz
Case operating temperature range ( $T_C$ ).....	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified  $V_{CC}$  range and case temperature range of -55°C to +125°C.

4/ The input and output negative voltage ratings may be exceeded provided that the input and output clamp current ratings are observed.

5/ Power dissipation values are derived using the formula  $P_D = V_{CC}I_{CC} + nV_{OL}I_{OL}$ , where  $V_{CC}$  and  $I_{OL}$  are as specified in 1.4 herein,  $I_{CC}$  and  $V_{OL}$  are as specified in table I herein, and n represents the total number of outputs.

6/ These parameters are not production tested.

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Non-Government publications. The following document form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the document which are DOD adopted are those listed in the issue of DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of documents cited in the solicitation.

### INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at <https://standards.ieee.org/standard/index.html>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

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3.2.5 Test access port controller and scan test registers. The test access port controller and scan test registers shall be as specified on figure 5.

3.2.6 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 6.

3.2.7 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 IEEE 1149.1 compliance. This device shall be compliant with IEEE 1149.1 - 1990.

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TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T <sub>c</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified		V <sub>CC</sub>	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
High level output voltage 3006	V <sub>OH</sub>	For all inputs affecting output under test, V <sub>IN</sub> = V <sub>IH</sub> = 2.0 V or V <sub>IL</sub> = 0.8 V	I <sub>OH</sub> = -3 mA	4.5 V	1, 2, 3	2.5		V
				5.0 V	1, 2, 3	3.0		V
			I <sub>OH</sub> = -24 mA	4.5 V	1, 2, 3	2.0		V
Low level output voltage 3007	V <sub>OL</sub>	For all inputs affecting output under test V <sub>IN</sub> = V <sub>IH</sub> = 2.0 V or V <sub>IL</sub> = 0.8 V I <sub>OL</sub> = +48 mA		4.5 V	1, 2, 3		0.55	V
Negative input clamp voltage 3022	V <sub>IC-</sub>	For input under test, I <sub>IN</sub> = -18 mA		4.5 V	1, 2, 3		-1.2	V
Input current high 3010	I <sub>IH</sub> <u>4/</u>	For input under test, V <sub>IN</sub> = V <sub>CC</sub>	mCLK, mLE, mOE, TCK	4.5 V	1, 2, 3		+1.0	μA
			A or B ports	4.5 V	1, 2, 3		+100	
			TDI, TMS	4.5 V	1, 2, 3		+10.0	
Input current low 3009	I <sub>IL</sub> <u>4/</u>	For input under test, V <sub>IN</sub> = GND	mCLK, mLE, mOE, TCK	4.5 V	1, 2, 3		-1.0	μA
			A or B ports	4.5 V	1, 2, 3		-100	
			TDI, TMS	4.5 V	1, 2, 3		-150	
Three-state output leakage current high 3021	I <sub>OZH</sub> <u>5/</u>	For control inputs affecting output under test, V <sub>IN</sub> = V <sub>IH</sub> = 2.0 V or V <sub>IL</sub> = 0.8 V V <sub>OUT</sub> = 2.7 V		5.5 V	1, 2, 3		50.0	μA
Three-state output leakage current low 3020	I <sub>OZL</sub> <u>5/</u>	For control inputs affecting output under test, V <sub>IN</sub> = V <sub>IH</sub> = 2.0 V or V <sub>IL</sub> = 0.8 V V <sub>OUT</sub> = 0.5 V		5.5 V	1, 2, 3		-50.0	μA
Off-state leakage current	I <sub>OFF</sub>	For input or output under test, V <sub>IN</sub> or V <sub>OUT</sub> = 5.5 V All other pins at 0.0 V		0.0 V	1		±100	μA
High-state leakage current	I <sub>CEX</sub>	For output under test, V <sub>OUT</sub> = 5.5 V Outputs at high logic state		5.5 V	1, 2, 3		50	μA
Output current 3011	I <sub>O</sub> <u>6/</u>	V <sub>OUT</sub> = 2.5 V		5.5 V	1, 2, 3	-50	-200	mA
Quiescent supply current delta, TTL input level	ΔI <sub>CC</sub> <u>7/</u>	For input under test, V <sub>IN</sub> = 3.4 V For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5 V	1, 2, 3		50	μA
Quiescent supply current, output high 3005	I <sub>CCH</sub>	For all inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 A A or B ports		5.5 V	1, 2, 3		5.5	mA
Quiescent supply current, output low 3005	I <sub>CCL</sub>			5.5 V	1, 2, 3		38	mA
Quiescent supply current, outputs disabled 3005	I <sub>CCZ</sub>			5.5 V	1, 2, 3		5.0	mA
Power up three-state output leakage current	I <sub>OZPU</sub>	mOEAB = mOEBA = 0.8 V V <sub>OUT</sub> = 2.7 V or 0.5 V		0.0 V or 2.0 V	1, 2, 3		±50	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T <sub>c</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified		V <sub>CC</sub>	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Power down three-state output leakage current	I <sub>OZPD</sub>	$\overline{mOEAB} = \overline{mOEBA} = 0.8\text{ V}$ V <sub>OUT</sub> = 2.7 V or 0.5 V		2.0 V or 0.0 V	1, 2, 3		±50	mA
Input capacitance 3012	C <sub>IN</sub>	T <sub>C</sub> = +25°C See 4.4.1b	Control inputs	5.0 V	4		6.0	pF
I/O capacitance 3012	C <sub>I/O</sub>		A or B ports	5.0 V	4		12.0	pF
Output capacitance 3012	C <sub>OUT</sub>		TDO	5.0 V	4		9.0	pF
Low level ground bounce noise	V <sub>OLP</sub> <u>8/</u>	V <sub>IH</sub> = 3.0 V V <sub>IL</sub> = 0.0 V T <sub>A</sub> = +25°C See 4.4.1d		5.0 V	4		900	mV
	V <sub>OLV</sub> <u>8/</u>			5.0 V	4		-800	mV
High level V <sub>CC</sub> bounce noise	V <sub>OHP</sub> <u>8/</u>	See figure 6		5.0 V	4		1500	mV
	V <sub>OHV</sub> <u>8/</u>			5.0 V	4		-700	mV
Functional tests 3014	<u>9/</u>	V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.8 V Verify output V <sub>O</sub> See 4.4.1c		4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	
NORMAL MODE								
Propagation delay time, mAn to mBn or mBn to mAn 3003	t <sub>PLH1</sub>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 7		5.0 V	9	2.0	5.6	ns
				4.5 V and 5.5 V	10, 11	2.0	6.5	
	t <sub>PHL1</sub>			5.0 V	9	2.0	6.6	ns
				4.5 V and 5.5 V	10, 11	2.0	7.2	
Propagation delay time, mCLKAB to mBn or mCLKBA to mAn 3003	t <sub>PLH2</sub>			5.0 V	9	2.5	6.7	ns
				4.5 V and 5.5 V	10, 11	2.5	8.2	
	t <sub>PHL2</sub>			5.0 V	9	2.5	5.7	ns
				4.5 V and 5.5 V	10, 11	2.5	7.1	
Propagation delay time, mLEAB to mBn or mLEBA to mAn 3003	t <sub>PLH3</sub>			5.0 V	9	2.5	7.4	ns
				4.5 V and 5.5 V	10, 11	2.5	8.5	
	t <sub>PHL3</sub>			5.0 V	9	2.5	6.5	ns
				4.5 V and 5.5 V	10, 11	2.5	7.8	

See foot notes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	V <sub>CC</sub>	Group A subgroups	Limits <u>3/</u>		Unit
					Min	Max	
NORMAL MODE - Continued							
Propagation delay time, output enable, <u>mOEAB</u> to mBn or <u>mOEBA</u> to mAn 3003	t <sub>PZH1</sub>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 7	5.0 V	9	2.0	7.3	ns
			4.5 V and 5.5 V	10, 11	2.0	8.5	
	t <sub>PZL1</sub>		5.0 V	9	2.5	7.2	ns
			4.5 V and 5.5 V	10, 11	2.5	8.3	
Propagation delay time, output disable, <u>mOEAB</u> to mBn or <u>mOEBA</u> to mAn 3003	t <sub>PHZ1</sub>	5.0 V	9	3.0	8.8	ns	
		4.5 V and 5.5 V	10, 11	3.0	10.6		
	t <sub>PLZ1</sub>	5.0 V	9	2.5	6.5	ns	
		4.5 V and 5.5 V	10, 11	2.5	7.4		
Maximum mCLKAB or mCLKBA frequency	f <sub>MAX</sub>	5.0 V	9	100		MHz	
		4.5 V and 5.5 V	10, 11	100			

TEST MODE

Propagation delay time, TCK↓ to mAn or mBn 3003	t <sub>PLH4</sub>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 7	5.0 V	9	2.5	12.4	ns
			4.5 V and 5.5 V	10, 11	2.5	16.4	
	t <sub>PHL4</sub>		5.0 V	9	2.5	11.8	ns
			4.5 V and 5.5 V	10, 11	2.5	14.6	
Propagation delay time, TCK↓ to TDO 3003	t <sub>PLH5</sub>	5.0 V	9	2.0	6.1	ns	
		4.5 V and 5.5 V	10, 11	2.0	7.0		
	t <sub>PHL5</sub>	5.0 V	9	2.0	6.3	ns	
		4.5 V and 5.5 V	10, 11	2.0	7.6		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	V <sub>CC</sub>	Group A subgroups	Limits <u>3/</u>		Unit
					Min	Max	
TEST MODE - Continued							
Propagation delay time, output enable, TCK↓ to mAn or Bn 3003	t <sub>PZH2</sub>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 7	5.0 V	9	4.5	13.5	ns
			4.5 V and 5.5 V	10, 11	4.5	17.0	
	t <sub>PZL2</sub>		5.0 V	9	5.0	13.2	ns
			4.5 V and 5.5 V	10, 11	5.0	15.8	
Propagation delay time, output enable, TCK↓ to TDO 3003	t <sub>PZH3</sub>	5.0 V	9	2.5	7.9	ns	
		4.5 V and 5.5 V	10, 11	2.5	8.2		
	t <sub>PZL3</sub>	5.0 V	9	3.0	7.8	ns	
		4.5 V and 5.5 V	10, 11	3.0	8.9		
Propagation delay time, output disable, TCK↓ to mAn or Bn 3003	t <sub>PHZ2</sub>	5.0 V	9	4.0	15.3	ns	
		4.5 V and 5.5 V	10, 11	4.0	18.5		
	t <sub>PLZ2</sub>	5.0 V	9	3.5	13.6	ns	
		4.5 V and 5.5 V	10, 11	3.5	16.7		
Propagation delay time, output enable, TCK↓ to TDO 3003	t <sub>PHZ3</sub>	5.0 V	9	3.0	9.2	ns	
		4.5 V and 5.5 V	10, 11	3.0	10.7		
	t <sub>PLZ3</sub>	5.0 V	9	3.0	6.8	ns	
		4.5 V and 5.5 V	10, 11	3.0	8.0		
Maximum TCK frequency	f <sub>MAX2</sub>	5.0 V	9	50		MHz	
		4.5 V and 5.5 V	10, 11	50			

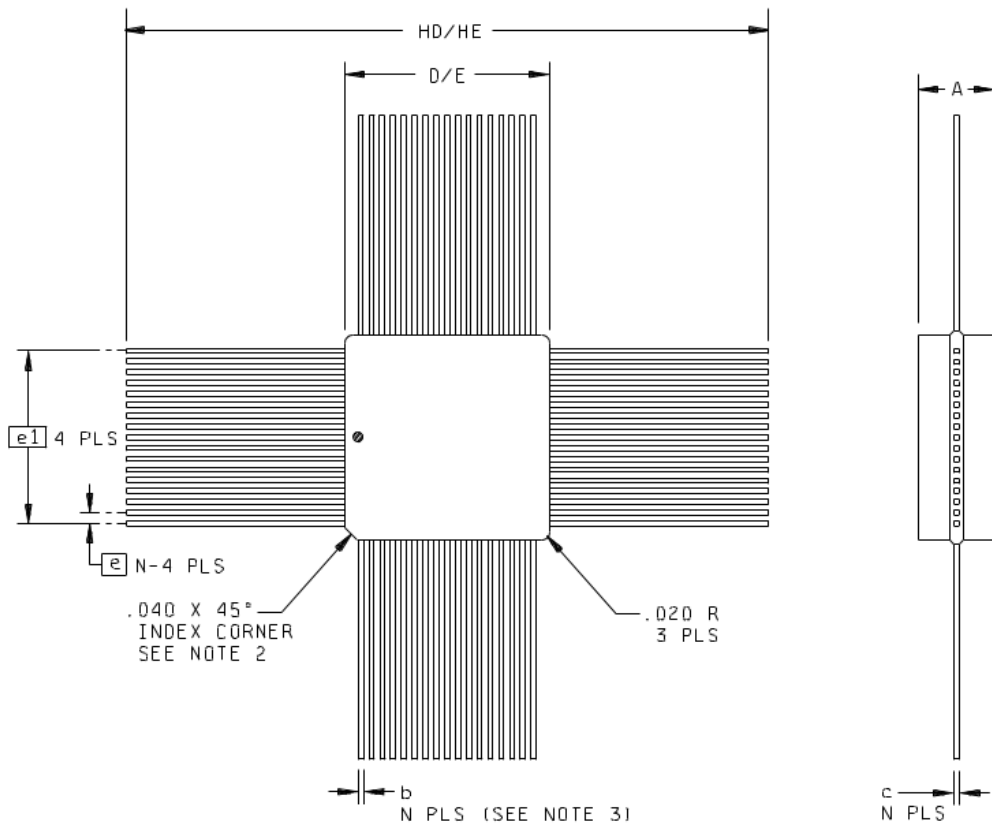
See footnotes on next sheet.

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TABLE I. Electrical performance characteristics – Continued.

- 1/ For tests not listed in the referenced MIL-STD-883 (e.g.  $\Delta I_{CC}$ ), utilize the general test procedure under the conditions listed herein.
- 2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all  $I_{CC}$  and  $\Delta I_{CC}$  tests where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For terminals not designated,  $V_{IN} = GND$  or  $V_{IN} \geq 3.0 V$ .
- 3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. Devices shall meet or exceed the limits specified in table I if tested at  $4.5 V \leq V_{CC} \leq 5.5 V$ .
- 4/ For I/O ports, the limit includes  $I_{OZH}$  or  $I_{OZL}$  leakage current from the output circuitry.
- 5/ For I/O ports, the limit includes  $I_{IH}$  or  $I_{IL}$  leakage current from the output circuitry.
- 6/ Not more than one output should be tested at one time, and the duration of the test condition should not exceed one second.
- 7/ This is the increase in supply current for each input that is at one of the specific TTL voltage levels rather than 0 V or  $V_{CC}$ . This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at  $V_{IN} = V_{CC} - 2.1 V$  (alternate method). When the test is performed using the alternate test method, the maximum limits is equal to the number of inputs at a high TTL input level times 50  $\mu A$ , and the preferred method and limits are guaranteed.
- 8/ This test is for qualification only. Ground and  $V_{CC}$  bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500 $\Omega$  of load resistance and a minimum of 50 pF of load capacitance (see figure 6). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested that, whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from  $V_{CC}$  to ground. The device manufacturer shall determine the values of these decoupling capacitors. The low and high level ground and  $V_{CC}$  bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50 $\Omega$  input impedance.  
  
 The device inputs shall be conditioned such that all outputs are at a high nominal  $V_{OH}$  level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at  $V_{OH}$  as all other outputs possible are switched from  $V_{OH}$  to  $V_{OL}$ .  $V_{OHV}$  and  $V_{OHP}$  are then measured from the nominal  $V_{OH}$  level to the largest negative and positive peaks, respectively (see figure 6). This is then repeated with the same outputs not under test switching from  $V_{OL}$  to  $V_{OH}$ .  
  
 The device inputs shall be conditioned such that all outputs are at a low nominal  $V_{OL}$  level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at  $V_{OL}$  as all other outputs possible are switched from  $V_{OL}$  to  $V_{OH}$ .  $V_{OLP}$  and  $V_{OLV}$  are then measured from the nominal  $V_{OL}$  level to the largest positive and negative peaks, respectively (see figure 6). This is then repeated with the same outputs not under test switching from  $V_{OH}$  to  $V_{OL}$ .
- 9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity in qualified devices. After incorporating allowable tolerances per MIL-STD-883,  $V_{IL} = 0.4 V$  and  $V_{IH} = 2.4 V$ . For outputs  $L \leq 0.8 V$ ,  $H \geq 2.0 V$ .

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Dimension	Inches		Millimeters	
	Min	Max	Min	Max
HD/HE	1.300	1.500	33.02	38.10
D/E	.485	.50	12.32	12.70
A	.134	.154	3.404	3.912
b	.008	.013	0.203	0.303
e	.025 BSC		0.635 BSC	
e1	.400 BSC		10.160 BSC	
c	.005	.007	0.127	0.178
N	68		68	

NOTES:

1. Dimensions are in inches. Millimeter equivalents are given for reference only.
2. A terminal 1 identification mark shall be located on the first side clockwise from the index corner. Terminal numbers shall increase in a counterclockwise direction when viewed as shown.
3. N is the maximum number of terminals.

FIGURE 1. Case outlines.

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Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	18	NC	35	NC	52	NC
2	V <sub>CC</sub>	19	C <sub>CC</sub>	36	V <sub>CC</sub>	53	V <sub>CC</sub>
3	TDO	20	2A1	37	TCK	54	1B9
4	1CLKAB	21	2A2	38	2CLKBA	55	1B8
5	1LEAB	22	2A3	39	2LEBA	56	1B7
6	GND	23	GND	40	GND	57	GND
7	$\overline{1OEAB}$	24	2A4	41	$\overline{2OEBA}$	58	1B6
8	1A1	25	2A5	42	2B9	59	1B5
9	1A2	26	2A6	43	2B8	60	1B4
10	1A3	27	2A7	44	2B7	61	1B3
11	1A4	28	2A8	45	2B6	62	1B2
12	1A5	29	2A9	46	2B5	63	1B1
13	GND	30	GND	47	GND	64	GND
14	1A6	31	$\overline{2OEAB}$	48	2B4	65	$\overline{1OEBA}$
15	1A7	32	2LEAB	49	2B3	66	1LEBA
16	1A8	33	2CLKAB	50	2B2	67	1CLKBA
17	1A9	34	TDI	51	2B1	68	TMS

NC = No internal connection.

Terminal descriptions	
Terminal symbol	Description
mAn (m = 1 to 2, n = 1 to 9)	Data inputs/outputs, A port
mBn (m = 1 to 2, n = 1 to 9)	Data inputs/outputs, B port
$\overline{mOEAB}$ , $\overline{mOEBA}$ (m = 1 to 2)	A-toB/B-to-A output enable control inputs
mCLKAB, mCLKBA (m = 1 to 2)	A-toB/B-to-A clock inputs
mLEAB, mLEBA (m = 1 to 2)	A-toB/B-to-A latch enable inputs
TDI	Test data input
TDO	Test data output
TMS	Test mode select input
TCK	Test clock input

FIGURE 2. Terminal connections.

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Device type 01				
Inputs				Outputs
$\overline{\text{mOEAB}}$	mLEAB	mCLKAB	mAn	mBn
L	L	L	X	B0
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

H = High voltage level

L = Low voltage level

X = Irrelevant

Z = Disabled

↑ = Low-to-high clock transition

B0 = The level of B before the indicated steady-state input conditions were established.

NOTE: A-to-B data flow is shown, B-to-A data flow is similar except using  $\overline{\text{mOEBA}}$ , mLEBA, and mCLKBA.

FIGURE 3. Truth table.

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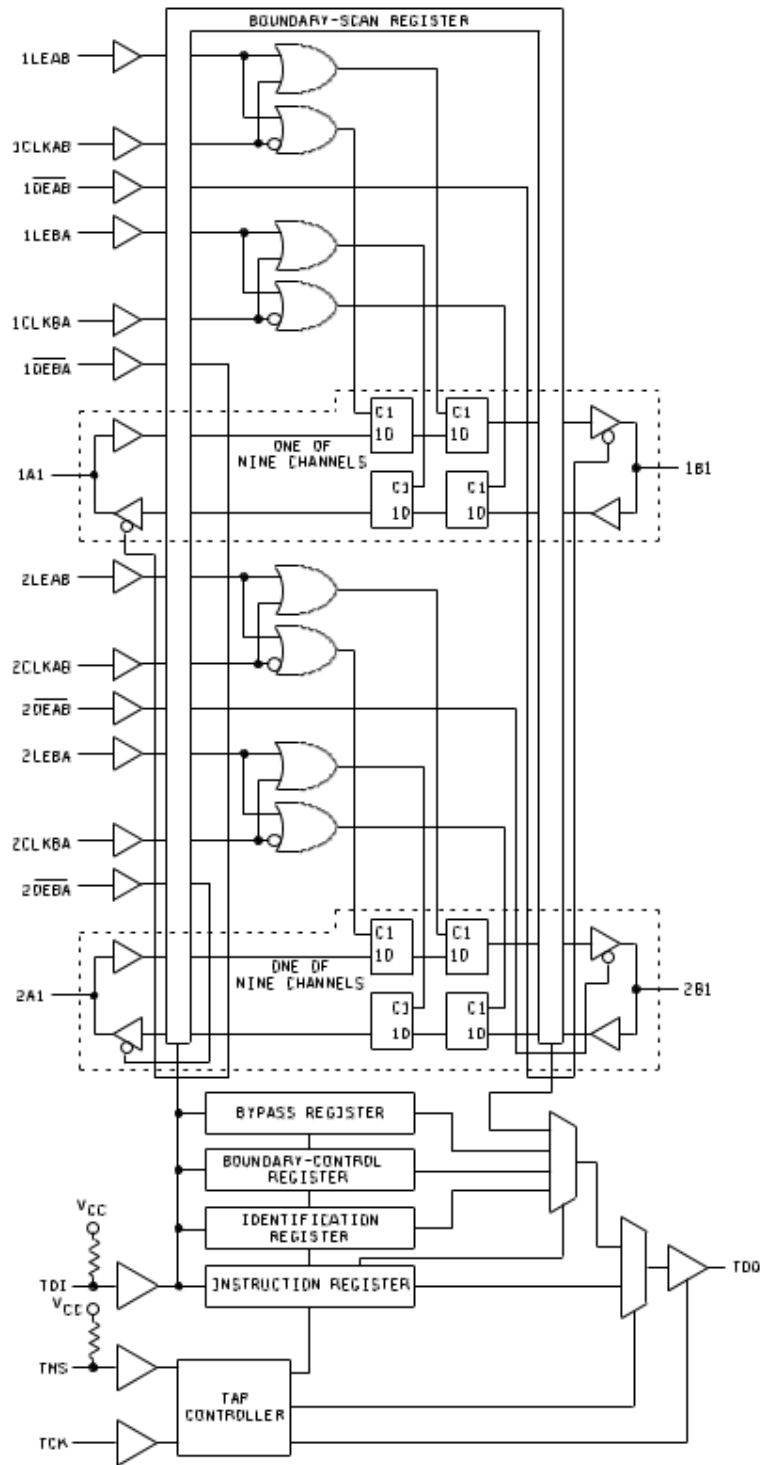


FIGURE 4. Block diagram.

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Test access port (TAP) controller state diagram

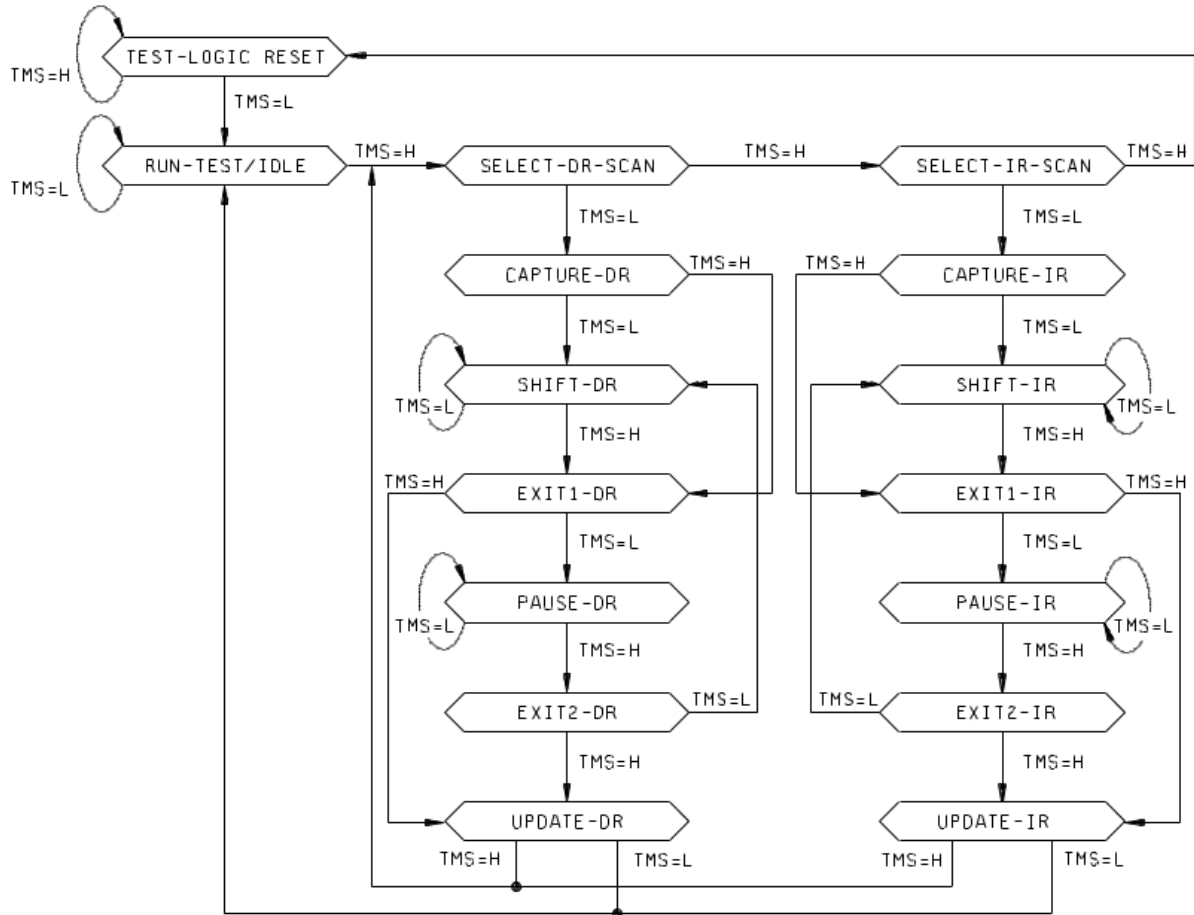
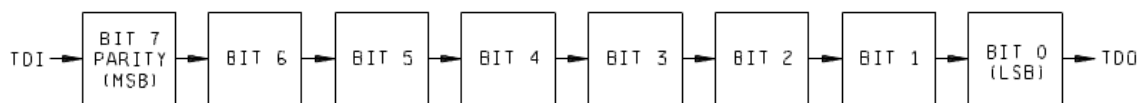


FIGURE 5. Test access port controller and scan test registers.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-94672</b>
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### Instruction register (IR) order of scan



NOTE: During capture-IR, the IR captures the binary value 10000001. At power up or in the test-logic-reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction.

### Instruction register opcodes

Binary code <u>1</u> / Bit 7 → Bit 0 MSB → LSB	Scope™ opcode	Description	Selected data register	Mode
00000000	EXTEST	Boundary scan	Boundary-scan	Test
10000001	BYPASS <u>2</u> /	Bypass scan	Bypass	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	INTEST	Boundary scan	Boundary-scan	Test
10000100	BYPASS <u>2</u> /	Bypass scan	Bypass	Normal
00000101	BYPASS <u>2</u> /	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/O	Bypass	Test
10001000	BYPASS <u>2</u> /	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary-scan	Normal
10001011	READBT	Boundary read	Boundary-scan	Test
00001100	CEKKTST	Boundary self test	Boundary-scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary-control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary-control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

1/ Bit 7 is used to maintain even parity in the 8-bit instruction.

2/ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in this device.

FIGURE 5. Test access port controller and scan test registers - Continued.

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Boundary-scan register (BSR) configuration

BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal
83	2OEAB	71	2A9-I	53	2A9-O	35	2B9-I	17	2B9-O
82	1OEAB	70	2A8-I	52	2A8-O	34	2B8-I	16	2B8-O
81	2OEBA	69	2A7-I	51	2A7-O	33	2B7-I	15	2B7-O
80	1OEBA	68	2A6-I	50	2A6-O	32	2B6-I	14	2B6-O
79	2CLKAB	67	2A5-I	49	2A5-O	31	2B5-I	13	2B5-O
78	1CLKBA	66	2A4-I	48	2A4-O	30	2B4-I	12	2B4-O
77	1CLKBA	65	2A3-I	47	2A3-O	29	2B3-I	11	2B3-O
76	2LEAB	64	2A2-I	46	2A2-O	28	2B2-I	10	2B2-O
75	1LEAB	63	2A1-I	45	2A1-O	27	2B1-I	9	2B1-O
74	2LEBA	62	1A9-I	44	1A9-O	26	1B9-I	8	1B9-O
73	2LEBA	61	1A8-I	43	1A8-O	25	1B8-I	7	1B8-O
72	1LEBA	60	1A7-I	42	1A7-O	24	1B7-I	6	1B7-O
---		59	1A6-I	41	1A6-O	23	1B6-I	5	1B6-O
---		58	1A5-I	40	1A5-O	22	1B5-I	4	1B5-O
---		57	1A4-I	39	1A4-O	21	1B4-I	3	1B4-O
---		56	1A3-I	38	1A3-O	20	1B3-I	2	1B3-O
---		55	1A2-I	37	1A2-O	19	1B2-I	1	1B2-O
---		54	1A1-I	36	1A1-O	18	1B1-I	0	1B1-O

NOTE: The source of data to be captured into the BSR during capture-DR is determined by the current instruction. The contents of the BSR may change during run-test/idle as determined by the current instruction. At power up or in the test-logic-reset state, the value of each boundary-scan cell (BSC) is reset to logic 0 except BSCs 83 through 80, which are reset to logic 1.

FIGURE 5. Test access port controller and scan test registers - Continued.

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Boundary-control register (BCR) configuration

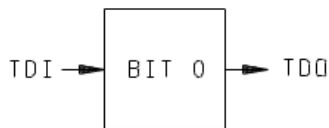
BCR bit number	Test control signal	BCR bit number	Test control signal	BCR bit number	Test control signal
20	MASK2.9	11	MASK1.9	2	OPCODE2
19	MASK2.8	10	MASK1.8	1	OPCODE1
18	MASK2.7	9	MASK1.7	0	OPCODE0
17	MASK2.6	8	MASK1.6	---	---
16	MASK2.5	7	MASK1.5	---	---
15	MASK2.4	6	MASK1.4	---	---
14	MASK2.3	5	MASK1.3	---	---
13	MASK2.2	4	MASK1.2	---	---
12	MASK2.1	3	MASK1.1	---	---

NOTE: During capture-DR (DR stands for data register), the contents of BCR are not changed. A power up or in the test-logic-reset state, the BCR is reset to the binary value of 00000000000000000010, which selects the PSA test operation with no input masking.

Boundary-control register opcodes

Binary code Bit 2 → Bit 0 MSB → LSB	Description
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/36-bit mode (PRPG)
X10	Parallel signature analysis/36-bit mode (PSA)
X11	Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT)

Bypass register order of scan



NOTE: During capture-DR, the bypass register captures a logic 0.

FIGURE 5. Test access port controller and scan test registers - Continued.

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		REVISION LEVEL <b>C</b>	SHEET <b>18</b>

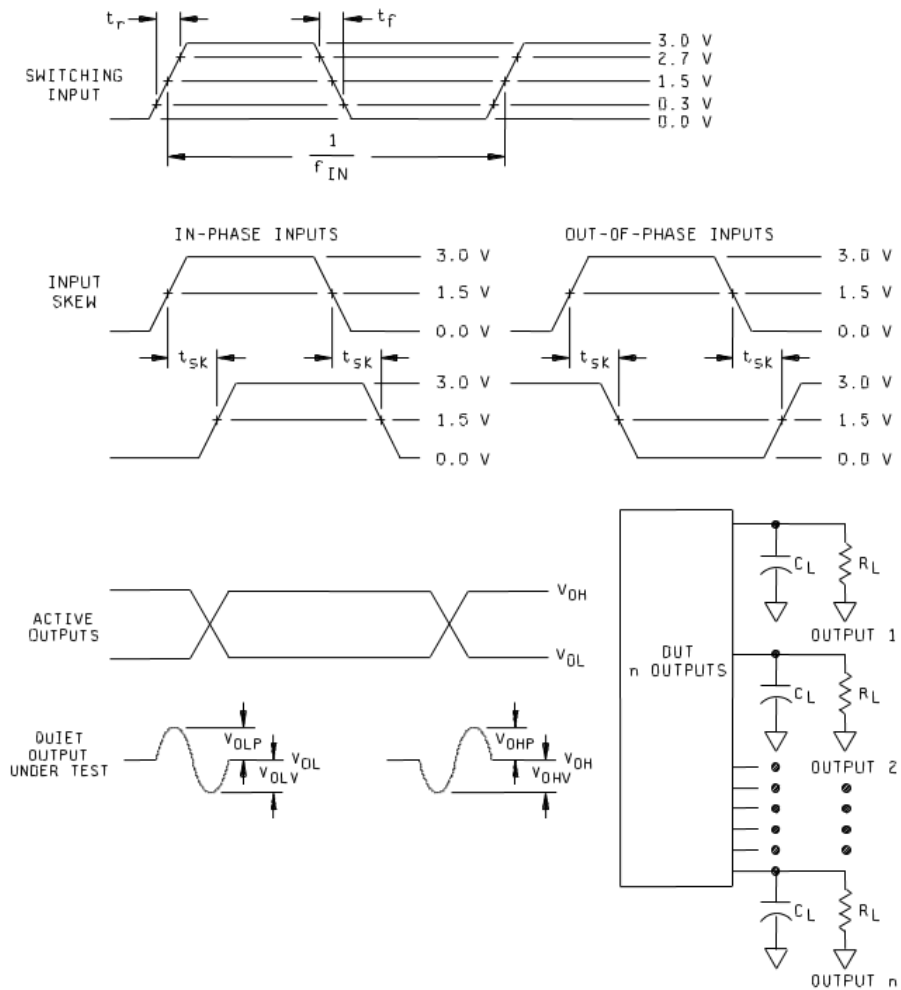
IDR bit number	Identification significance	IDR bit number	Identification significance	IDR bit number	Identification significance
31	VERSION3	27	PARTNUMBER15	11	MANUFACTURER10
30	VERSION2	26	PARTNUMBER14	10	MANUFACTURER09
29	VERSION1	25	PARTNUMBER13	9	MANUFACTURER08
28	VERSION0	24	PARTNUMBER12	8	MANUFACTURER07
---	---	23	PARTNUMBER11	7	MANUFACTURER06
---	---	22	PARTNUMBER10	6	MANUFACTURER05
---	---	21	PARTNUMBER9	5	MANUFACTURER04
---	---	20	PARTNUMBER8	4	MANUFACTURER03
---	---	19	PARTNUMBER7	3	MANUFACTURER02
---	---	18	PARTNUMBER6	2	MANUFACTURER01
---	---	17	PARTNUMBER5	1	MANUFACTURER00
---	---	16	PARTNUMBER4	0	LOGIC1
---	---	15	PARTNUMBER3	---	---
---	---	14	PARTNUMBER2	---	---
---	---	13	PARTNUMBER1	---	---
---	---	12	PARTNUMBER0	---	---

1/ For vendor 01295 products, bits 11-0 of the device identification register will always contain the binary value 00000101111 (02F, hex).

NOTE: During capture-DR, the binary value 00000000000000001100000010111 (0000602F, hex) is captured in the device identification register to identify this device as Texas Instruments SNJ54ABT18502, version 0.

FIGURE 5. Test access port controller and scan test registers - Continued.

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**NOTES:**

1.  $C_L$  includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2.  $R_L = 450\Omega \pm 1$  percent, chip resistor in series with a  $50\Omega$  termination. For monitored outputs, the  $50\Omega$  termination shall be the  $50\Omega$  characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
  - a.  $V_{IN} = 0.0$  V to 3.0 V; duty cycle = 50 percent;  $f_{IN} \geq 1$  MHz.
  - b.  $t_r, t_f = 3.0$  ns  $\pm 1.0$  ns. For input signal generators incapable of maintaining these values of  $t_r$  and  $t_f$ , the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the  $\pm 1.0$  ns tolerance and guaranteeing the results at 3.0 ns  $\pm 1.0$  ns; skew between any two switching input signals ( $t_{sk}$ )  $\leq 250$  ps.

FIGURE 6. Ground bounce waveforms and test circuit.

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		REVISION LEVEL <b>C</b>	SHEET <b>20</b>

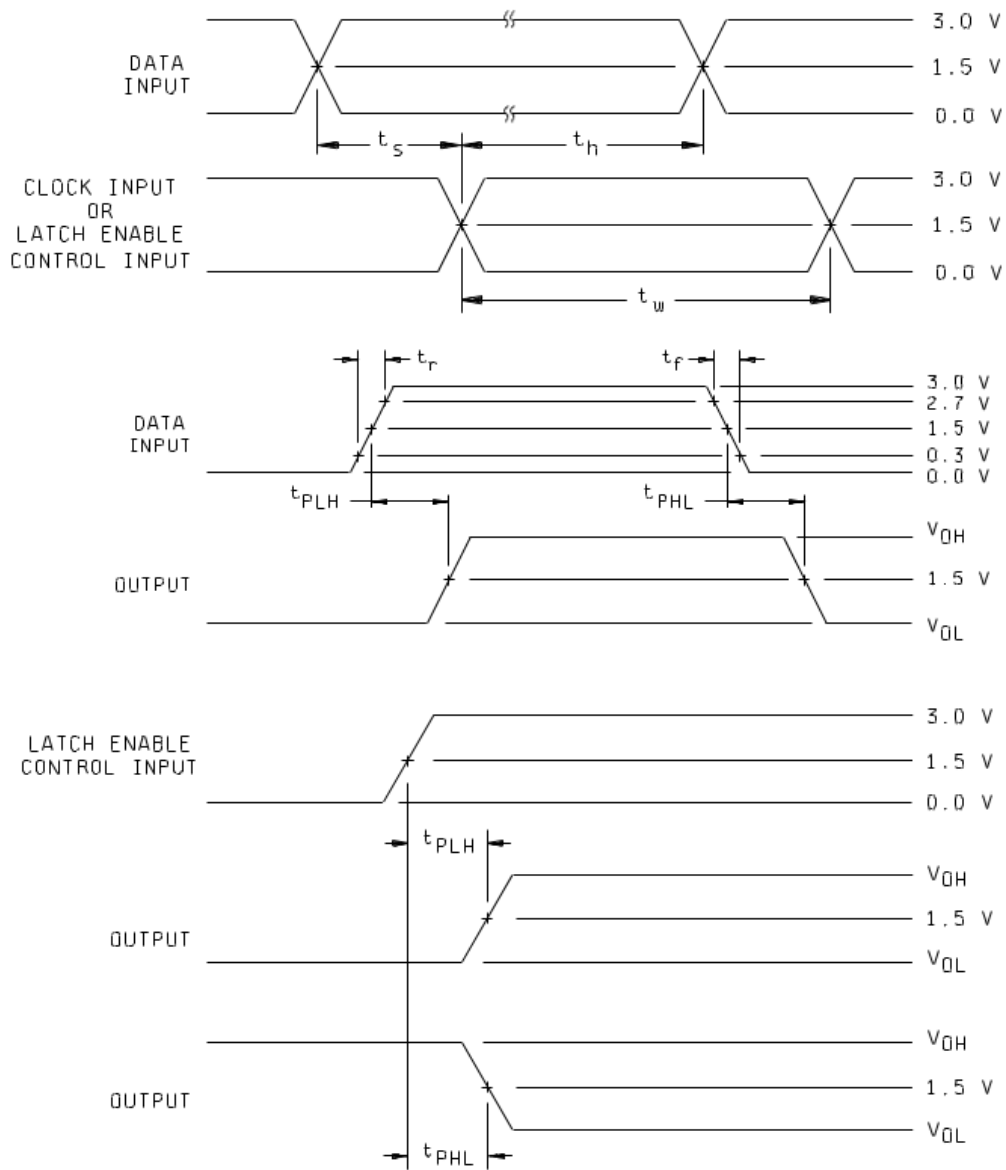


FIGURE 7. Switching waveforms and test circuit.

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COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-94672**

REVISION LEVEL  
**C**

SHEET **21**

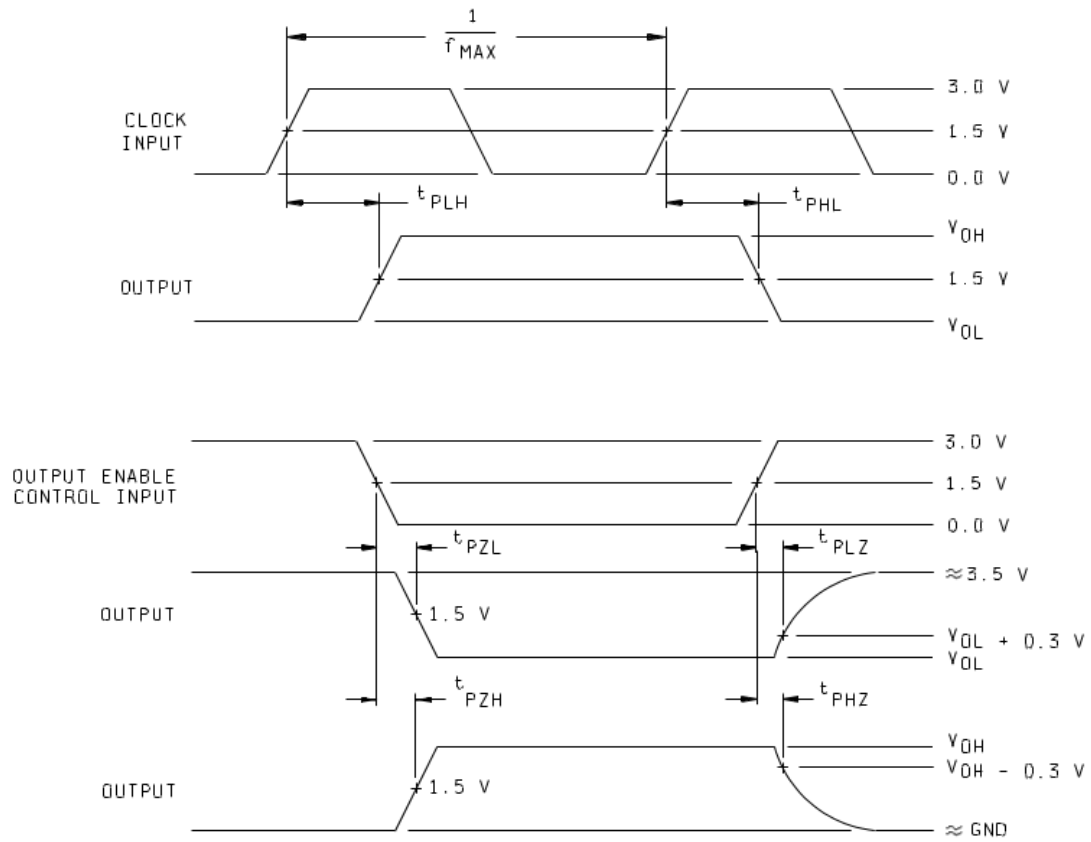


FIGURE 7. Switching waveforms and test circuit – Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-94672</b>
		REVISION LEVEL <b>C</b>	SHEET <b>22</b>

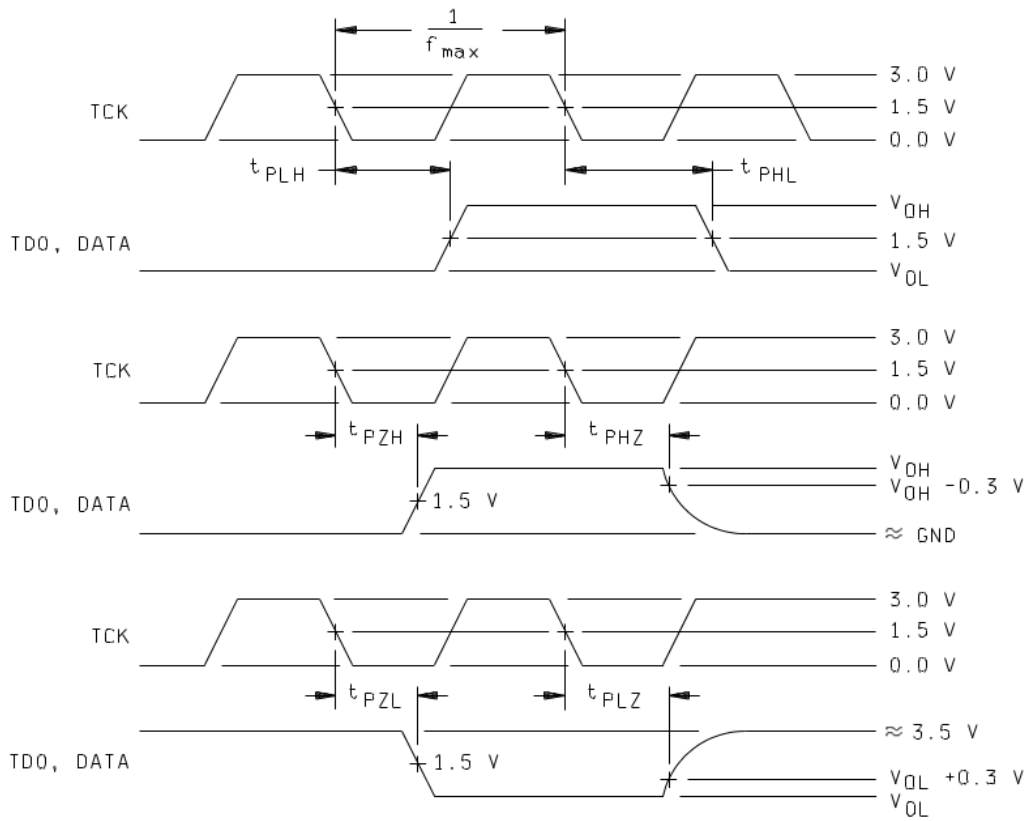
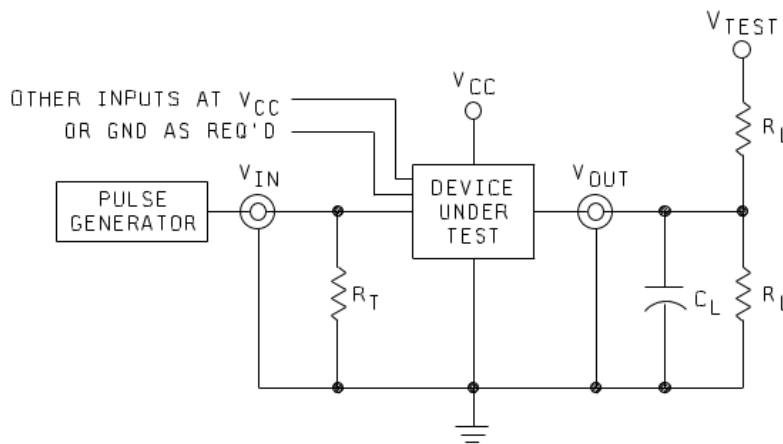
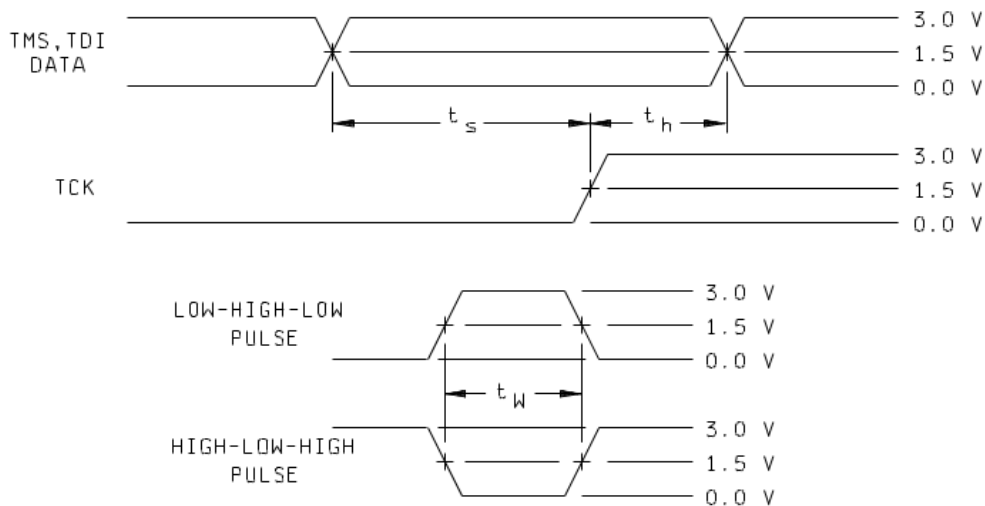


FIGURE 7. Switching waveforms and test circuit – Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-94672</b>
		REVISION LEVEL <b>C</b>	SHEET <b>23</b>



**NOTES:**

1. When measuring  $t_{PLZ}$  and  $t_{PZL}$ :  $V_{TEST} = 7.0\text{ V}$ .
2. When measuring  $t_{PHZ}$ ,  $t_{PZH}$ ,  $t_{PLH}$  and  $t_{PHL}$ :  $V_{TEST} = \text{open}$ .
3. The  $t_{PZL}$  and  $t_{PLZ}$  reference waveform is for the output under test with internal conditions such that the output is at  $V_{OL}$  except when disabled by the output enable control. The  $t_{PZH}$  and  $t_{PHZ}$  reference waveform is for the output under test with internal conditions such that the output is at  $V_{OH}$  except when disabled by the output enable control.
4.  $C_L = 50\text{ pF}$  minimum or equivalent (includes test jig and probe capacitance).
5.  $R_T = 50\Omega$  or equivalent.  $R_L = 500\Omega$  or equivalent.
6. Input signal from pulse generator:  $V_{IN} = 0.0\text{ V}$  to  $3.0\text{ V}$ ;  $PRR \leq 10\text{ MHz}$ ;  $t_r \leq 2.5\text{ ns}$ ;  $t_f \leq 2.5\text{ ns}$ ;  $t_r$  and  $t_f$  shall be measured from  $0.3\text{ V}$  to  $2.7\text{ V}$  and from  $2.7\text{ V}$  to  $0.3\text{ V}$ , respectively; duty cycle = 50 percent.
7. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
8. The outputs are measured one at a time with one transition per measurement.

FIGURE 7. Switching waveforms and test circuit – Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-94672</b>
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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b.  $C_{IN}$ ,  $C_{OUT}$ , and  $C_{I/O}$  shall be measured only for initial qualification and after process or design changes which may affect capacitance.  $C_{IN}$ ,  $C_{OUT}$ , and  $C_{I/O}$  shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test ( $V_{BIAS}$ ) = 2.5 V or 3.0 V. For  $C_{IN}$ ,  $C_{OUT}$ , and  $C_{I/O}$ , test all applicable pins on five devices with zero failures.

For  $C_{IN}$ ,  $C_{OUT}$ , and  $C_{I/O}$  a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the  $C_{IN}$ ,  $C_{OUT}$ , and  $C_{I/O}$  tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results for each device tested.

- c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

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- d. Ground and  $V_{CC}$  bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture.  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The package type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DLA Land and Maritime-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DLA Land and Maritime-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DLA Land and Maritime-VA data from testing on both fixtures that shall include all measured peak values for each device tested and detailed oscilloscope plots for each  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For  $V_{OHP}$ ,  $V_{OHV}$ ,  $V_{OLP}$ , and  $V_{OLV}$ , a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the  $V_{OHP}$ ,  $V_{OHV}$ ,  $V_{OLP}$ , and  $V_{OLV}$  tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturer shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results, along with the oscilloscope plots, for each device tested.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

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4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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DATE: 23-10-25

Approved sources of supply for SMD 5962-94672 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9467201QXA	01295	SNJ54ABT18502HV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Ln.  
P.O. Box 660199  
Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.