REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. – jak	07-05-30	Thomas M. Hess
B	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	13-06-21	Thomas M. Hess
C	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - TTM	20-08-21	Muhammad A. Akbar

REV																				
SHEET																				
REV		C	C	C	C	C	C	C	C	C										
SHEET		15	16	17	18	19	20	21	22	23										
REV STATUS	REV							C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET							1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

CHECKED BY
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APPROVED BY
Monica L. Poelking

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DRAWING APPROVAL DATE
94-04-26

MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, SCAN TEST DEVICE WITH OCTAL BUS TRANSCEIVER AND REGISTER, THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

REVISION LEVEL
C

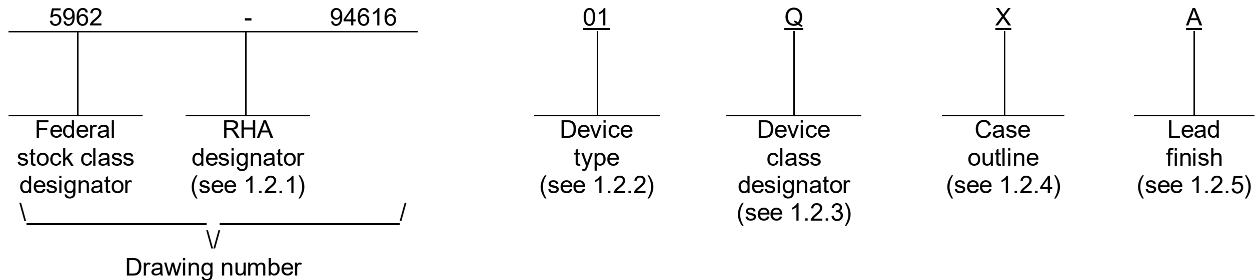
SIZE	CAGE CODE	
A	**67268**	**5962-94616**

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ABT8652	Scan test device with octal bus transceiver and register, three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP3-T28 or CDIP4-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (I/O ports) (V_{IN})	-0.5 V dc to +5.5 V dc 4/
DC input voltage range (except I/O ports) (V_{IN})	-0.5 V dc to +7.0 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to +5.5 V dc 4/
DC output current (I_{OL}) (per output)	+96 mA
DC input clamp current (I_{IK}) (V_{IN} = < 0.0 V)	-18 mA
DC output clamp current (I_{OK}) (V_{OUT} = < 0.0 V)	-50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D)	420 mW 5/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V
Minimum high level input voltage (V_{IH})	2.0 V
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+48 mA
Maximum input rise and fall rate ($\Delta t/\Delta V$)	10 ns/V
Minimum setup time (t_s):	
An before CLKAB↑ or Bn before CLKBA↑	5.1 ns
An, Bn, CLKAB, CLKBA, SAB, SBA, OEAB, or $\overline{OEBA}$ before TCK↑	7.0 ns
TDI before TCK↑	6.0 ns
TMS before TCK↑	6.0 ns
Minimum hold time (t_h):	
An before CLKAB↑ or Bn after CLKBA↑	0.5 ns
An, Bn, CLKAB, CLKBA, SAB, SBA, OEAB, $\overline{OEBA}$ or after TCK↑	0.6 ns
TDI after TCK↑	0.9 ns
TMS after TCK↑	0.9 ns
Minimum pulse width: (t_w)	
CLKAB or CLKBA high or low	3.0 ns
TCK high or low	5.0 ns
Minimum delay time, power-up to TCK↑ (t_d)	50.0 ns 6/
Minimum rise time, V_{CC} power-up (t_r)	1.0 µs 6/
Maximum clock frequency: (f_{CLK})	
TCK	50 MHz
CLKAB or CLKBA	100 MHz
Case operating temperature range (T_C)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ The input and output negative voltage ratings may be exceeded provided that the input and output clamp current ratings are observed.

5/ Power dissipation values are derived using the formula $P_D = V_{CC}I_{CC} + nV_{OL}I_{OL}$, where V_{CC} and I_{OL} are as specified in 1.4 herein, I_{CC} and V_{OL} are as specified in table I herein, and n represents the total number of outputs.

6/ These parameters are not production tested.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the document which are DOD adopted are those listed in the issue of DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at https://standards.ieee.org/standard/index.html.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Test access port controller and scan test registers. The test access port controller and scan test registers shall be as specified on figure 4.

3.2.6 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 5.

3.2.7 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. .

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 IEEE 1149.1 compliance. This device shall be compliant with IEEE 1149.1 - 1990.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \leq T_C \leq +125°C$ $+4.5 V \leq V_{CC} \leq +5.5 V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
High level output voltage 3006	V_{OH}	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V	$I_{OH} = -3$ mA	4.5 V	1, 2, 3	2.5		V
				5.0 V	1, 2, 3	3.0		V
			$I_{OH} = -24$ mA	4.5 V	1, 2, 3	2.0		V
Low level output voltage 3007	V_{OL}	For all inputs affecting output under test, $V_{IN} = V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V $I_{OL} = +48$ mA		4.5 V	1, 2, 3		0.55	V
Negative input clamp voltage 3022	V_{IC-}	For input under test, $I_{IN} = -18$ mA		4.5 V	1, 2, 3		-1.2	V
Input current high 3010	I_{IH} 4/	For input under test, $V_{IN} = V_{CC}$	CLK, S, OEAB, $\overline{OEBA}$, TCK	4.5 V	1, 2, 3		+1.0	μA
			A or B ports	4.5 V	1, 2, 3		+100	
			TDI, TMS	4.5 V	1, 2, 3		+10.0	
Input current low 3009	I_{IL} 4/	For input under test, $V_{IN} = 0.0$ V	CLK, S, OEAB, $\overline{OEBA}$, TCK	4.5 V	1, 2, 3		-1.0	μA
			A or B ports	4.5 V	1, 2, 3		-100	
			TDI, TMS	4.5 V	1, 2, 3		-160	
Three-state output leakage current high 3021	I_{OZH} 5/	For control inputs affecting output under test, $V_{IN} = V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V $V_{OUT} = 2.7$ V		5.5 V	1, 2, 3		50.0	μA
Three-state output leakage current low 3020	I_{OZL} 5/	For control inputs affecting output under test, $V_{IN} = V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V $V_{OUT} = 0.5$ V		5.5 V	1, 2, 3		-50.0	μA
Off-state leakage current	I_{OFF}	For input or output under test, V_{IN} or $V_{OUT} = 5.5$ V All other pins at 0.0 V		0.0 V	1		±100	μA
High-state leakage current	I_{CEX}	For output under test, $V_{OUT} = 5.5$ V Outputs at high logic state		5.5 V	1, 2, 3		50	μA
Output current 3011	I_O 6/	$V_{OUT} = 2.5$ V		5.5 V	1, 2, 3	-50	-180	mA
Quiescent supply current delta, output high 3005	ΔI_{CC} 7/	For input under test, $V_{IN} = 3.4$ V For all other inputs, $V_{IN} = V_{CC}$ or GND		5.5 V	1, 2, 3		1.5	mA
Quiescent supply current, output high 3005	I_{CCH}	For all inputs, $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$ A A or B ports		5.5 V	1, 2, 3		2.0	mA
Quiescent supply current, output low 3005	I_{CCL}			5.5 V	1, 2, 3		38	mA
Quiescent supply current, outputs disabled 3005	I_{CCZ}			5.5 V	1, 2, 3		2.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \leq T_C \leq +125°C$ $+4.5 V \leq V_{CC} \leq +5.5 V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Input capacitance 3012	C_{IN}	T_C = +25°C See 4.4.1b	Control inputs	5.0 V	4		15.3	pF
Input/output capacitance 3012	$C_{I/O}$		A or B ports	5.0 V	4		24.9	pF
Output capacitance 3012	C_{OUT}		TDO	5.0 V	4		24.2	pF
Low level ground bounce noise	V_{OLP} 8/	V_{IH} = 3.0 V V_{IL} = 0.0 V T_A = +25°C See 4.4.1d See figure 5		5.0 V	4		1500	mV
	V_{OLV} 8/			5.0 V	4		-1000	mV
High level V_{CC} bounce noise	V_{OHP} 8/			5.0 V	4		1600	mV
	V_{OHV} 8/			5.0 V	4		-550	mV
Functional tests 3014	9/	V_{IL} = 0.8 V, V_{IH} = 2.0 V Verify output V_O See 4.4.1c		4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	
NORMAL MODE								
Propagation delay time, An to Bn or Bn to An 3003	t_{PLH1}	C_L = 50 pF minimum R_L = 500 Ω See figure 6		5.0 V	9	2.0	5.1	ns
				4.5 V and 5.5 V	10, 11	2.0	6.0	
	t_{PHL1}			5.0 V	9	1.5	4.4	ns
				4.5 V and 5.5 V	10, 11	1.5	5.8	
Propagation delay time, CLKAB to Bn or CLKBA to An 3003	t_{PLH2}			5.0 V	9	2.5	5.3	ns
				4.5 V and 5.5 V	10, 11	2.5	6.3	
	t_{PHL2}			5.0 V	9	2.5	5.4	ns
				4.5 V and 5.5 V	10, 11	2.5	6.7	
Propagation delay time, SAB to Bn or SBA to An 3003	t_{PLH3}			5.0 V	9	2.0	6.1	ns
				4.5 V and 5.5 V	10, 11	2.0	7.5	
	t_{PHL3}			5.0 V	9	2.0	6.7	ns
				4.5 V and 5.5 V	10, 11	2.0	7.8	

See foot notes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \leq T_C \leq +125°C$ $+4.5 V \leq V_{CC} \leq +5.5 V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/		Unit
					Min	Max	
NORMAL MODE – Continued.							
Propagation delay time, output enable, OEAB to Bn or $\overline{OEBA}$ to An 3003	t_{PZH1}	C_L = 50 pF minimum R_L = 500 Ω See figure 6	5.0 V	9	1.7	5.4	ns
			4.5 V and 5.5 V	10, 11	1.7	6.7	
	t_{PZL1}		5.0 V	9	2.0	6.2	ns
			4.5 V and 5.5 V	10, 11	2.0	7.6	
Propagation delay time, output disable, OEAB to Bn or $\overline{OEBA}$ to An 3003	t_{PHZ1}		5.0 V	9	2.0	6.9	ns
			4.5 V and 5.5 V	10, 11	2.0	8.3	
	t_{PLZ1}		5.0 V	9	2.0	6.9	ns
			4.5 V and 5.5 V	10, 11	2.0	7.8	
Maximum CLKAB or CLKBA frequency	f_{MAX}		5.0 V	9	100		MHz
			4.5 V and 5.5 V	10, 11	100		
TEST MODE							
Propagation delay time, TCK↓ to An or Bn 3003	t_{PLH4}	C_L = 50 pF minimum R_L = 500 Ω See figure 6	5.0 V	9	3.5	10.2	ns
			4.5 V and 5.5 V	10, 11	3.3	13.7	
	t_{PHL4}		5.0 V	9	3.0	9.0	ns
			4.5 V and 5.5 V	10, 11	3.0	12.0	
Propagation delay time, TCK↓ to TDO 3003	t_{PLH5} 10/		5.0 V	9	2.5	5.5	ns
			4.5 V and 5.5 V	10, 11	2.5	7.0	
	t_{PHL5} 10/		5.0 V	9	2.5	5.5	ns
			4.5 V and 5.5 V	10, 11	2.5	7.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5 V \le V_{CC} \le +5.5 V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/		Unit
					Min	Max	
TEST MODE – Continued.							
Propagation delay time, output enable, TCK↓ to An or Bn 3003	t_{PZH2}	C_L = 50 pF minimum R_L = 500 Ω See figure 6	5.0 V	9	4.5	9.5	ns
			4.5 V and 5.5 V	10, 11	4.3	12.5	
	t_{PZL2}		5.0 V	9	4.5	10.5	ns
			4.5 V and 5.5 V	10, 11	4.5	13.5	
Propagation delay time, output enable, TCK↓ to TDO 3003	t_{PZH3}		5.0 V	9	2.5	5.5	ns
			4.5 V and 5.5 V	10, 11	2.5	7.0	
	t_{PZL3}		5.0 V	9	2.5	6.0	ns
			4.5 V and 5.5 V	10, 11	2.5	7.5	
Propagation delay time, output disable, TCK↓ to An or Bn 3003	t_{PHZ2}		5.0 V	9	3.5	12.9	ns
			4.5 V and 5.5 V	10, 11	3.5	14.0	
	t_{PLZ2}		5.0 V	9	3.0	10.5	ns
			4.5 V and 5.5 V	10, 11	3.0	13.5	
Propagation delay time, output disable, TCK↓ to TDO 3003	t_{PHZ3}		5.0 V	9	3.0	7.0	ns
			4.5 V and 5.5 V	10, 11	3.0	9.0	
	t_{PLZ3}		5.0 V	9	3.0	6.5	ns
			4.5 V and 5.5 V	10, 11	3.0	8.0	
Maximum TCK frequency	f_{MAX2}		4.5 V and 5.5 V	9	50		MHz
				10, 11	50		

See footnotes on next sheet.

TABLE I. Electrical performance characteristics – Continued.

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For terminals not designated, V_{IN} = GND or $V_{IN} \geq 3.0$ V.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. Devices shall meet or exceed the limits specified in table I if tested at $4.5 \text{ V} \leq V_{CC} \leq 5.5$ V.

4/ For I/O ports, the limit includes I_{OZH} or I_{OZL} leakage current from the output circuitry.

5/ For I/O ports, the limit includes I_{IH} or I_{IL} leakage current from the output circuitry.

6/ Not more than one output should be tested at one time, and the duration of the test condition should not exceed one second.

7/ This is the increase in supply current for each input that is at one of the specific TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). When the test is performed using the alternate test method, the maximum limits is equal to the number of inputs at a high TTL input level times 1.5 mA, and the preferred method and limits are guaranteed.

8/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 5). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested that, whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The device manufacturer shall determine the values of these decoupling capacitors. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity in qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs L ≤ 0.8 V, H ≥ 2.0 V.

Device type	01	
Case outlines	X	3
Terminal number	Terminal symbol	
1	CLKAB	B4
2	SAB	B3
3	OEAB	B2
4	A1	B1
5	A2	$\overline{OEBA}$
6	A3	SBA
7	GND	CLKBA
8	A4	CLKAB
9	A5	SAB
10	A6	OEAB
11	A7	A1
12	A8	A2
13	TDO	A3
14	TMS	GND
15	TCK	A4
16	TDI	A5
17	B8	A6
18	B7	A7
19	B6	A8
20	B5	TDO
21	V_{CC}	TMS
22	B4	TCK
23	B3	TDI
24	B2	B8
25	B1	B7
26	$\overline{OEBA}$	B6
27	SBA	B5
28	CLKBA	V_{CC}

Terminal descriptions	
Terminal symbol	Description
An (n = 1 to 8)	Data inputs/outputs, A port
Bn (n = 1 to 8)	Data inputs/outputs, B port
CLKAB/CLKBA	A-to-B/B-to-A clock input
SAB, SBA	A-to-B/B-to-A output data source select inputs
OEAB/$\overline{OEBA}$	A-to-B/B-to-A output enable control inputs
TDI	Test data input
TDO	Test data output
TMS	Test mode select input
TCK	Test clock input

FIGURE 1. Terminal connections.

Inputs						Data I/Os		Operation
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	An	Bn	
L	H	H or L	H or L	X	X	Input disabled	Input disabled	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified 1/	Store A, hold B data
H	H	↑	↑	X 2/	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	unspecified 1/	Input	Hold A, store B
L	L		↑	X	X 2/	Output	Input	Stored B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Input	Output	Stored A data to B bus and stored B data to A bus

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low-to-high transition

1/ The data output functions can be enabled or disabled by a variety of level combinations at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

2/ When select control is low, clocks can occur simultaneously. When select control is high, clocks must be staggered in order to load both registers.

FIGURE 2. Truth table.

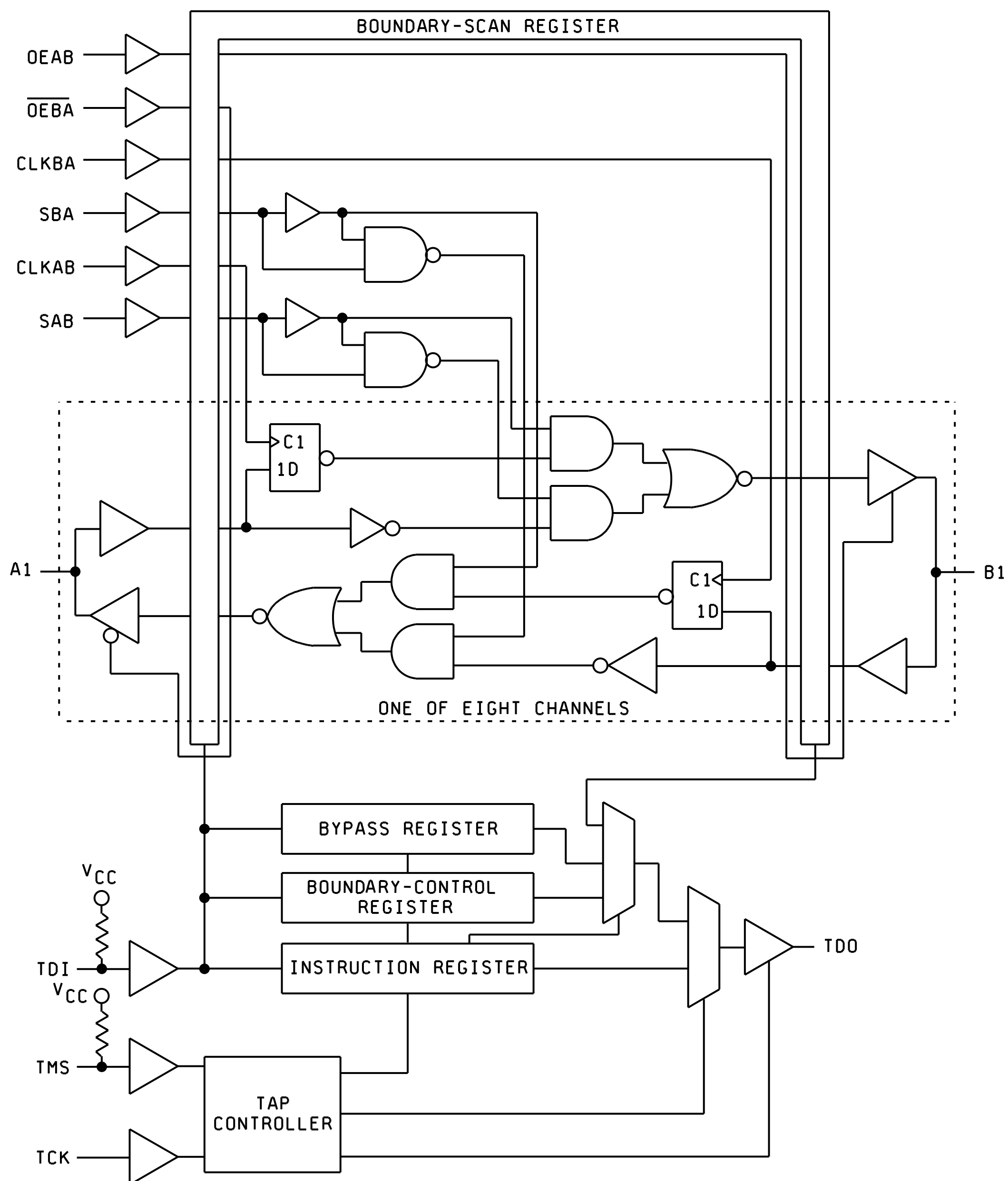


FIGURE 3. Block diagram.

Test access port (TAP) controller state diagram.

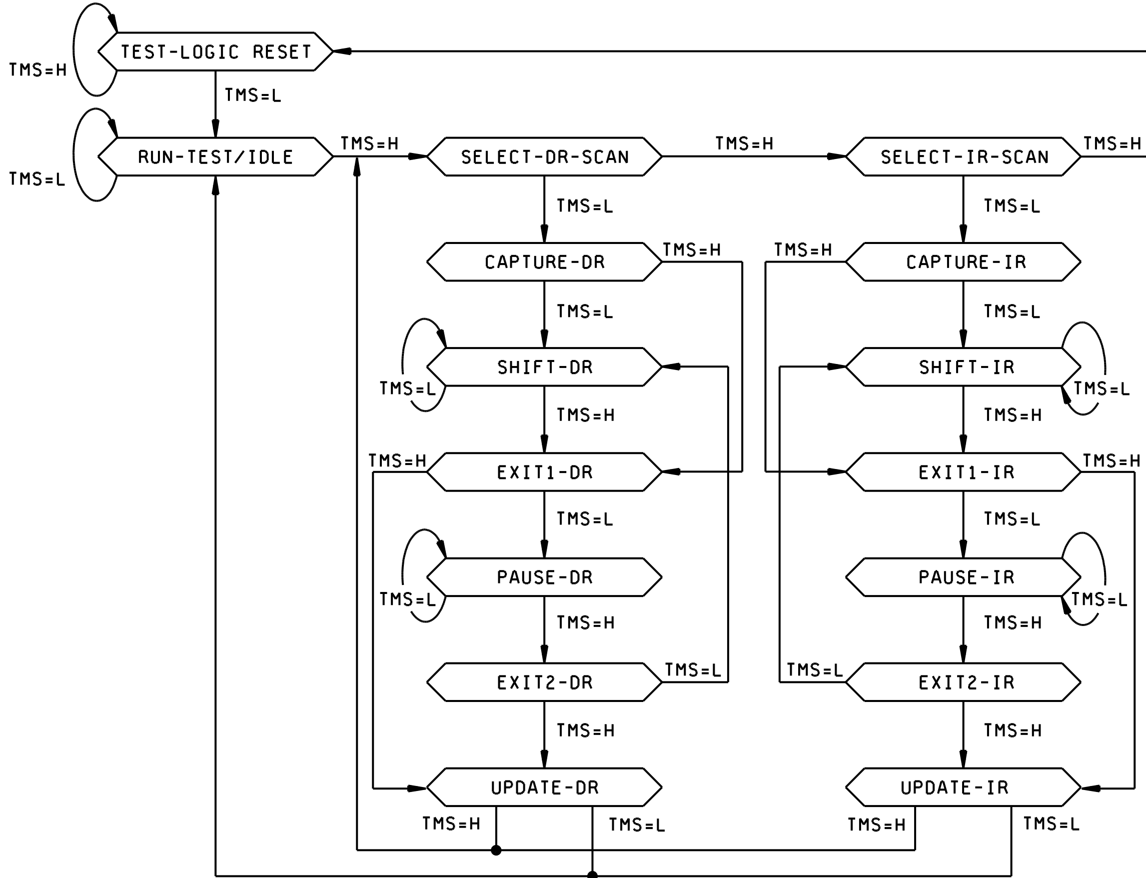
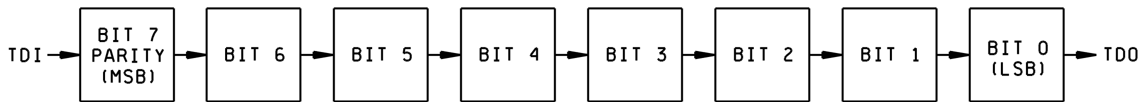


FIGURE 4. Test access port controller and scan test registers.

Instruction register (IR) order of scan



NOTE: During capture-IR, the IR captures the binary value 10000001. At power up or in the test-logic-reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction.

Instruction register opcodes

Binary code 1/ Bit 7 → Bit 0 MSB → LSB	Scope™ opcode	Description	Selected data register	Mode
00000000	EXTEST	Boundary scan	Boundary-scan	Test
10000001	BYPASS 2/	Bypass scan	Bypass	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	INTEST	Boundary scan	Boundary-scan	Test
10000100	BYPASS 2/	Bypass scan	Bypass	Normal
00000101	BYPASS 2/	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/O	Bypass	Test
10001000	BYPASS 2/	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary-scan	Normal
10001011	READBT	Boundary read	Boundary-scan	Test
00001100	CELLTST	Boundary self test	Boundary-scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary-control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary-control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

1/ Bit 7 is used to maintain even parity in the 8-bit instruction.

2/ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in this device.

FIGURE 4. Test access port controller and scan test registers - Continued.

Boundary-scan register (BSR) configuration

BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal
37	OEAB	31	A8-I	23	A8-O	15	B8-I	7	B8-O
36	$\overline{\text{OEBA}}$	30	A7-I	22	A7-O	14	B7-I	6	B7-O
35	CLKAB	29	A6-I	21	A6-O	13	B6-I	5	B6-O
34	CLKBA	28	A5-I	20	A5-O	12	B5-I	4	B5-O
33	SAB	27	A4-I	19	A4-O	11	B4-I	3	B4-O
32	SBA	26	A3-I	18	A3-O	10	B3-I	2	B3-O
- - -	- - -	25	A2-I	17	A2-O	9	B2-I	1	B2-O
- - -	- - -	24	A1-I	16	A1-O	8	B1-I	0	B1-O

Boundary-control register (BCR) configuration

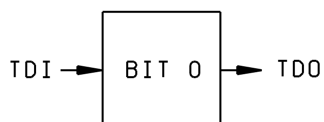
BCR bit number	Test control signal	BCR bit number	Test control signal	BCR bit number	Test control signal
10	MASK8	6	MASK4	2	OPCODE2
9	MASK7	5	MASK3	1	OPCODE1
8	MASK6	4	MASK2	0	OPCODE0
7	MASK5	3	MASK1	- - -	- - -

NOTE: During capture-DR (DR stands for data register), the contents of BCR are not changed. A power up or in the test-logic-reset state, the BCR is reset to the binary value of 00000000010 which selects the PSA test operation with no input masking.

Boundary-control register opcodes

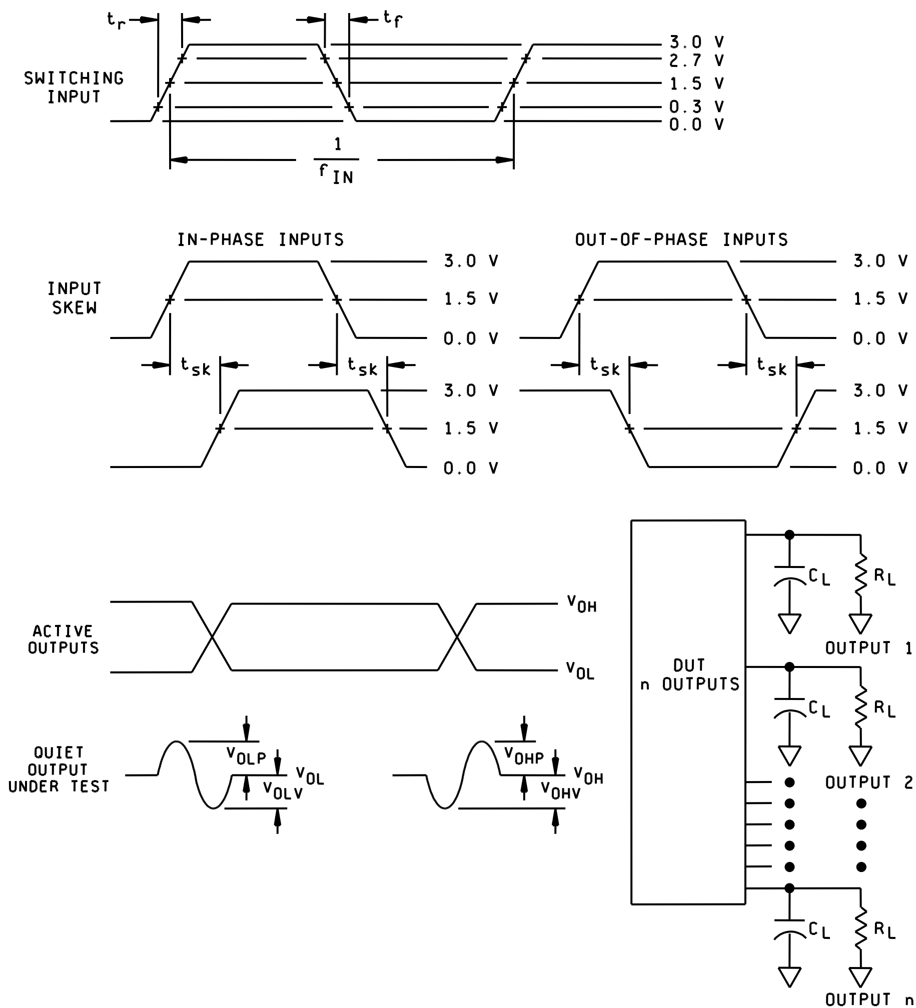
Binary code Bit 2 → Bit 0 MSB → LSB	Description
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-ramdom pattern generation/16-bit mode (PRPG)
X10	Parallel signature analysis/16-bit mode (PSA)
X11	Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT)

Bypass register order of scan



NOTE: During capture-DR, the bypass register capturers a logic 0.

FIGURE 4. Test access port controller and scan test registers - Continued.



NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq$ 1 MHz.
   b. t_r, t_f = 3.0 ns ±1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching input signals (t_{sk}): ≤ 250 ps.

FIGURE 5. Ground bounce waveforms and test circuit.

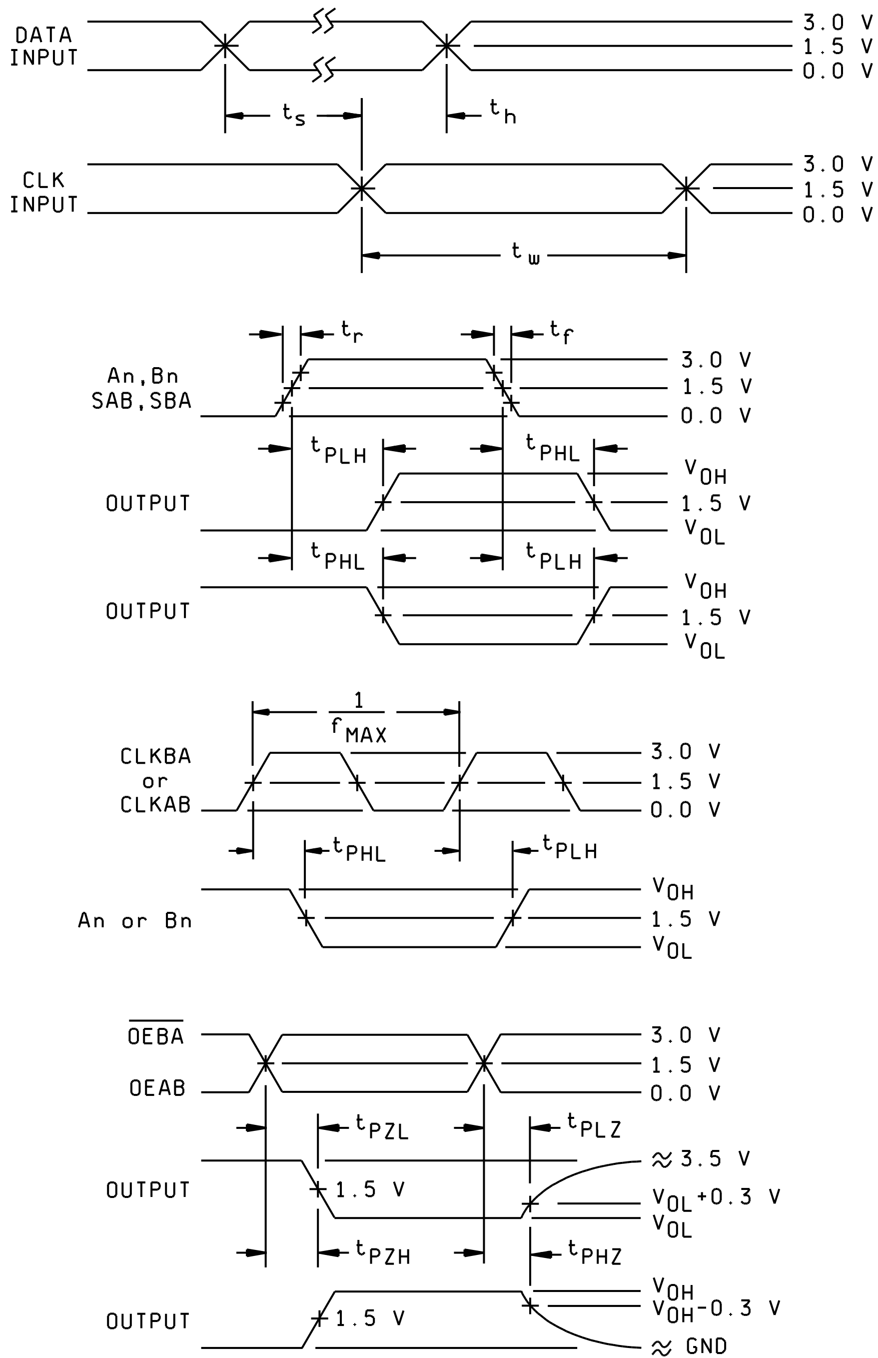


FIGURE 6. Switching waveforms and test circuit.

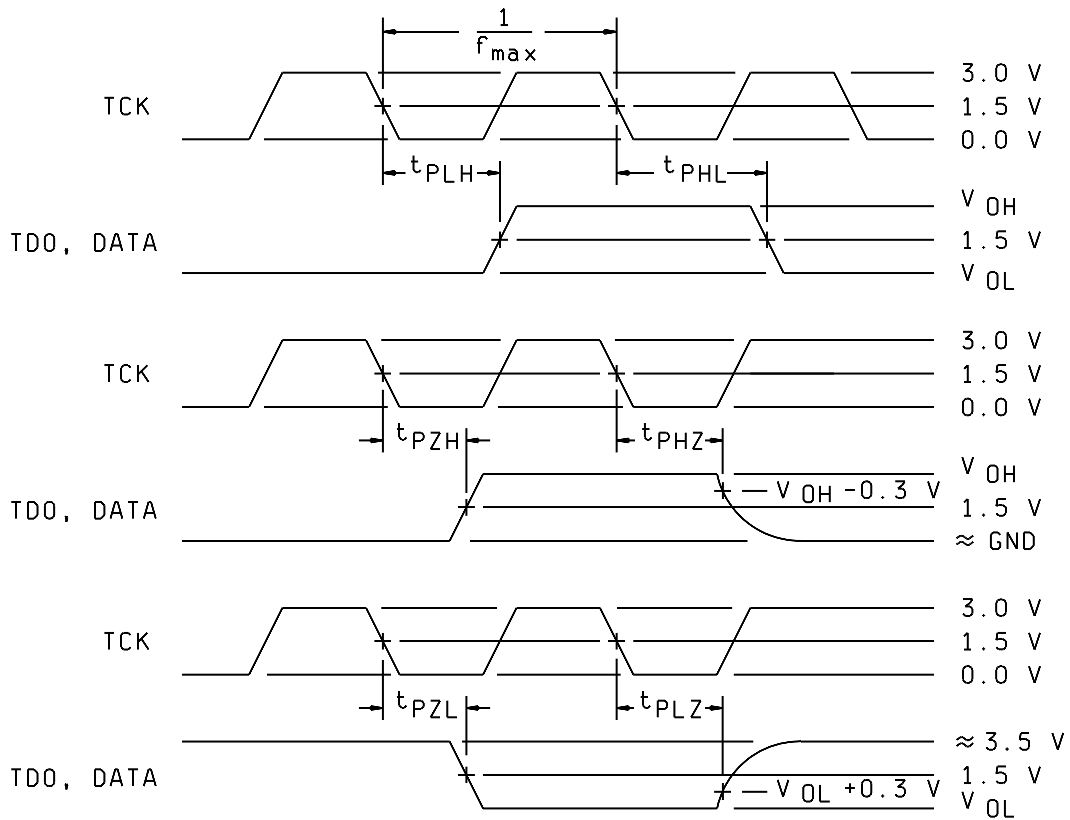
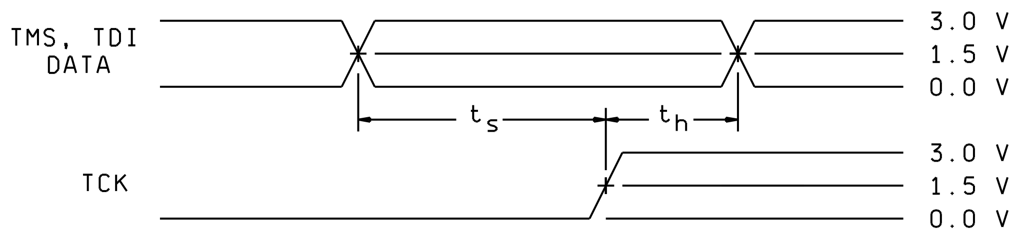
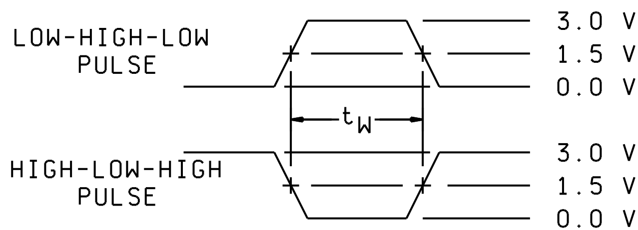
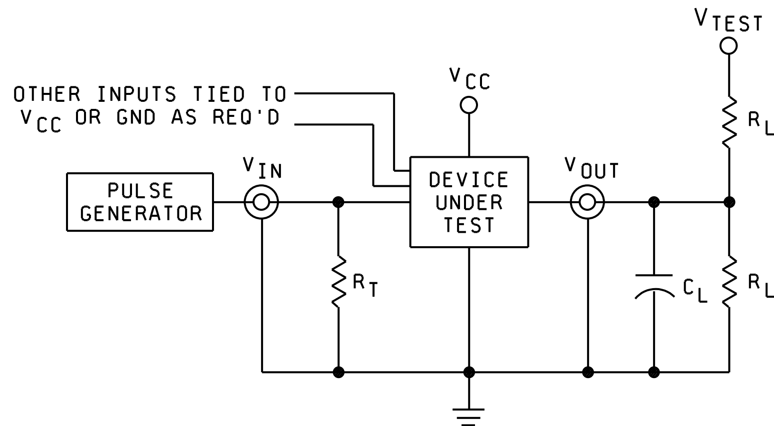


FIGURE 6. Switching waveforms and test circuit – Continued.







NOTES:

1. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 7.0 V.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH} and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_T = 50Ω or equivalent. R_L = 500Ω or equivalent.
6. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
7. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
8. The outputs are measured one at a time with one transition per measurement.

FIGURE 6. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. C_{IN}, C_{OUT}, and $C_{I/O}$, shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN}, C_{OUT}, and $C_{I/O}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN}, C_{OUT}, and $C_{I/O}$, test all applicable pins on five devices with zero failures.

For C_{IN}, C_{OUT}, and $C_{I/O}$ a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the C_{IN}, C_{OUT}, and $C_{I/O}$ tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results for each device tested.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The package type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DLA Land and Maritime-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DLA Land and Maritime-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DLA Land and Maritime-VA data from testing on both fixtures that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For V_{OHP}, V_{OHV}, V_{OLP}, and V_{OLV}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the V_{OHP}, V_{OHV}, V_{OLP}, and V_{OLV} tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturer shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results, along with the oscilloscope plots, for each device tested.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-08-21

Approved sources of supply for SMD 5962-94616 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9461601QXA	01295	SNJ54ABT8652JT
5962-9461601Q3A	3/	SNJ54ABT8652FK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.