REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 04, 05, and 06. Add case outlines D and H. Make changes to 1.3, table I, and figure 1.	96-11-07	R. MONNIN
B	Replaced reference to MIL-STD-973 with reference to MIL-PRF-38535. Drawing updated to reflect current requirements. - gt	04-01-08	R. MONNIN
C	Update boilerplate paragraph to current MIL-PRF-38535 requirements. - ro	11-12-06	C. SAFFLE

REV																				
SHEET																				
REV	C																			
SHEET	15																			
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

CHECKED BY
RAJESH R. PITHADIA

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
94-04-14

MICROCIRCUIT, LINEAR, JFET-INPUT SINGLE/DUAL/QUAD OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

AMSC N/A

REVISION LEVEL
C

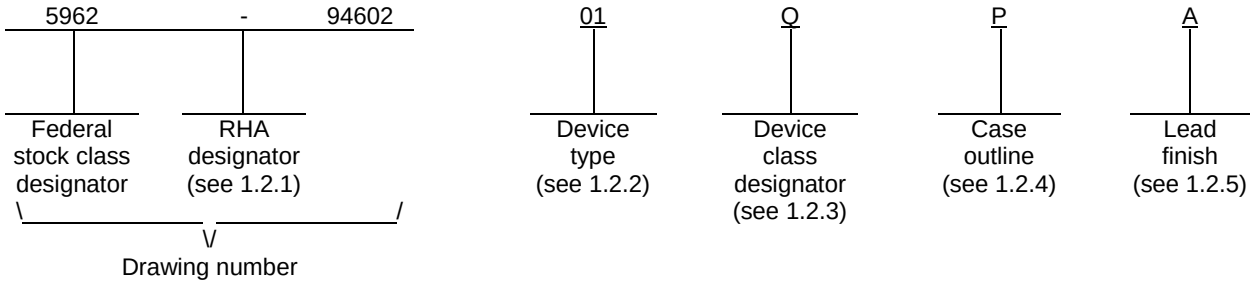
SIZE	CAGE CODE	
A	**67268**	**5962-94602**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TLE2071M	JFET-input operational amplifier
02	TLE2072M	JFET-input dual operational amplifier
03	TLE2074M	JFET-input quad operational amplifier
04	TLE2071AM	JFET-input operational amplifier
05	TLE2072AM	JFET-input dual operational amplifier
06	TLE2074AM	JFET-input quad operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
H	GDFP1-F10 or CDFP2-F10	10	Flat pack
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage ($+V_{CC}$) ..... +19 V dc
Supply voltage ($-V_{CC}$) ..... -19 V dc
Differential input voltage 3/ ..... $+V_{CC}$ to $-V_{CC}$
Input voltage range (V_I) (any input) ..... $+V_{CC}$ to $-V_{CC}$
Input current (I_I) (each input) ..... ±1 mA
Output current (I_O) ..... ±80 mA
Total current into $+V_{CC}$ terminal ..... 160 mA
Total current into $-V_{CC}$ terminal ..... -160 mA
Duration of short circuit current at (or below) +25°C 4/ ..... Unlimited
Storage temperature range ..... -65°C to +150°C
Junction temperature ..... +150°C
Power dissipation (P_D):
Case C 5/ ..... 1375 mW
Case D 5/ ..... 680 mW
Case H 5/ ..... 675 mW
Case P 5/ ..... 1050 mW
Case 2 5/ ..... 1375 mW
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage ($\pm V_{CC}$) ..... ±2.25 V dc minimum, ±19 V dc maximum
Common-mode input voltage (V_{IC}) ($\pm V_{CC}$ = ±5 V) ..... -0.8 V dc minimum, 5 V dc maximum
Common-mode input voltage (V_{IC}) ($\pm V_{CC}$ = ±15 V) ..... -10.8 V dc minimum, 15 V dc maximum
Ambient operating free-air temperature (T_A) ..... -55°C to +125°C
Source resistance from ground to input terminals (R_S) ..... 50 Ω

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltage values, except differential voltages, are with respect to the midpoint between $+V_{CC}$ and $-V_{CC}$.

3/ Differential voltages are at the noninverting input with respect to the inverting input.

4/ The output may be shorted to either supply. Temperature and supply voltage must be limited to ensure that the maximum dissipation rating is not exceeded.

5/ Above T_A = +25°C derate at a factor of 11 mW/°C for cases C and 2, 8 mW/°C for case D, 5.4 mW/°C for case H, and 8.4 mW/°C for case P.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 61 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Input offset voltage	V_{IO}	V_{CC} = ±5 V, V_{IC} = 0 V, R_S = 50 Ω	1	01	-4	4	mV
			2, 3		-9.2	9.2	
			1	02	-6	6	
			2, 3		-10.5	10.5	
			1	03	-5	5	
			2, 3		-10.5	10.5	
			1	04	-2	2	
			2, 3		-7.2	7.2	
			1	05	-3.5	3.5	
			2, 3		-8	8	
			1	06	-3	3	
			2, 3		-8.5	8.5	
		V_{CC} = ±15 V, V_{IC} = 0 V, R_S = 50 Ω	1	01	-4	4	
			2, 3		-9.2	9.2	
			1	02	-6	6	
			2, 3		-10.5	10.5	
			1	03	-5	5	
			2, 3		-10.5	10.5	
			1	04	-2	2	
			2, 3		-7.2	7.2	
			1	05	-3.5	3.5	
			2, 3		-8	8	
			1	06	-3	3	
			2, 3		-8.5	8.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset current	I_{IO}	V_{CC} = ±5 V, V_{IC} = 0 V, R_S = 50 Ω, T_A = -55°C, +125°C	2, 3	All	-20	20	nA
		V_{CC} = ±15 V, V_{IC} = 0 V, R_S = 50 Ω, T_A = -55°C, +125°C	2, 3		-20	20	
Input bias current	I_{IB}	V_{CC} = ±5 V, V_{IC} = 0 V, R_S = 50 Ω, T_A = -55°C, +125°C	2, 3	All	-60	60	nA
		V_{CC} = ±15 V, V_{IC} = 0 V, R_S = 50 Ω, T_A = -55°C, +125°C	2, 3		-60	60	
Common-mode input voltage range	V_{ICR}	V_{CC} = ±5 V	1	All	-1 to 5		V
			2, 3		-0.8 to 5		
		V_{CC} = ±15 V	1	01, 04	-11 to 15		
			2, 3		-10.9 to 15		
			1	02, 03, 05, 06	-11 to 15		
			2, 3		-10.8 to 15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Maximum positive peak output voltage swing	$+V_{OM}$	V_{CC} = ±5 V, I_{OUT} = -200 μA	1	All	3.8		V
			2, 3		3.6		
		V_{CC} = ±5 V, I_{OUT} = -2 mA	1		3.5		
			2, 3		3.3		
		V_{CC} = ±5 V, I_{OUT} = -20 mA	1		1.5		
			2, 3		1.4		
		V_{CC} = ±15 V,	1		13.8		
		I_{OUT} = -200 μA	2, 3		13.6		
		V_{CC} = ±15 V, I_{OUT} = -2 mA	1		13.5		
			2, 3		13.3		
		V_{CC} = ±15 V,	1		11.5		
		I_{OUT} = -20 mA	2, 3		11.4		
Maximum negative peak output voltage swing	$-V_{OM}$	V_{CC} = ±5 V, I_{OUT} = 200 μA	1	All	-3.8		V
			2, 3		-3.6		
		V_{CC} = ±5 V, I_{OUT} = 2 mA	1		-3.5		
			2, 3		-3.3		
		V_{cc} = ±5 V, I_{OUT} = 20 mA	1		-1.5		
			2, 3		-1.4		
		V_{CC} = ±15 V,	1		-13.8		
		I_{OUT} = 200 μA	2, 3		-13.6		
		V_{CC} = ±15 V, I_{OUT} = 2 mA	1		-13.5		
			2, 3		-13.3		
		V_{CC} = ±15 V, I_{OUT} = 20 mA	1		-11.5		
			2, 3		-11.4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Large signal differential voltage amplification	A_{VD}	V_{CC} = ±5 V, V_O = ±2.3 V, R_L = 600 Ω	1	All	80		dB
			2, 3		78		
		V_{CC} = ±5 V, V_O = ±2.3 V, R_L = 2 kΩ	1		90		
			2, 3		88		
		V_{CC} = ±5 V, V_O = ±2.3 V, R_L = 10 kΩ	1		95		
			2, 3		93		
		V_{CC} = ±15 V, V_O = ±10 V, R_L = 600 Ω	1		80		
			2, 3		78		
		V_{CC} = ±15 V, V_O = ±10 V, R_L = 2 kΩ	1		90		
			2, 3		88		
		V_{CC} = ±15 V, V_O = ±10 V, R_L = 10 kΩ	1		95		
			2, 3		93		
Common-mode rejection ratio	CMRR	V_{CC} = ±5 V, R_S = 50 Ω, V_{IC} = V_{ICR} minimum	1	All	70		dB
			2, 3		68		
		V_{CC} = ±15 V, R_S = 50 Ω, V_{IC} = V_{ICR} minimum	1		80		
			2, 3		78		
Supply-voltage rejection ratio ($\Delta+V_{CC}/\Delta V_{IO}$)	k_{SVR}	V_{CC} = ±5 V or ±15 V, R_S = 50 Ω	1	All	82		dB
			2, 3		80		
Supply current	I_{CC}	V_{CC} = ±5 V, V_O = 0 V, no load	1	01, 04	1.35	2.2	mA
			2, 3			2.2	
			1	02, 05	2.7	3.6	
			2, 3			3.6	
			1	03, 06	5.2	7.5	
			2, 3			7.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Supply current	I_{CC}	V_{CC} = ±15 V, V_O = 0 V, no load	1	01, 04	1.35	2.2	mA
			2, 3			2.2	
			1	02, 05	2.7	3.6	
			2, 3			3.6	
			1	03, 06	5.2	7.5	
			2, 3			7.5	
Positive slew rate	+SR	V_{CC} = ±15 V, R_L = 2 kΩ, C_L = 100 pF, A_V = -1, $V_{O(PP)}$ = 10 V	4	01, 04	30		V/µs
			5, 6		22		
			4	02, 05	28		
			5, 6		20		
			4	03, 06	25		
			5, 6		20		
Negative slew rate	-SR	V_{CC} = ±15 V, R_L = 2 kΩ, C_L = 100 pF, A_V = -1, $V_{O(PP)}$ = 10 V	4	01, 04	30		V/µs
			5, 6		22		
			4	02, 03, 05, 06	30		
			5, 6		20		

1/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

Device types	01 and 04			02 and 05		
Case outlines	H	P	2	H	P	2
Terminal number	Terminal symbol					
1	NC	OFFSET N1	NC	NC	OUTPUT 1	NC
2	OFFSET N1	-INPUT	OFFSET N1	OUTPUT 1	-INPUT 1	OUTPUT 1
3	-INPUT	+INPUT	NC	-INPUT 1	+INPUT 1	NC
4	+INPUT	$-V_{CC}$	NC	+INPUT 1	$-V_{CC}$	NC
5	$-V_{CC}$	OFFSET N2	-INPUT	$-V_{CC}$	+INPUT 2	-INPUT 1
6	OFFSET N2	OUTPUT	NC	+INPUT 2	-INPUT 2	NC
7	OUTPUT	$+V_{CC}$	+INPUT	-INPUT 2	OUTPUT 2	+INPUT 1
8	$+V_{CC}$	NC	NC	OUTPUT 2	$+V_{CC}$	NC
9	NC	---	NC	$+V_{CC}$	---	NC
10	NC	---	$-V_{CC}$	NC	---	$-V_{CC}$
11	---	---	NC	---	---	NC
12	---	---	OFFSET N2	---	---	+INPUT 2
13	---	---	NC	---	---	NC
14	---	---	NC	---	---	NC
15	---	---	OUTPUT	---	---	-INPUT 2
16	---	---	NC	---	---	NC
17	---	---	$+V_{CC}$	---	---	OUTPUT 2
18	---	---	NC	---	---	NC
19	---	---	NC	---	---	NC
20	---	---	NC	---	---	$+V_{CC}$

NC = No connection

FIGURE 1. Terminal connections.

Device types	03 and 06	
Case outlines	C and D	2
Terminal number	Terminal symbol	
1	OUTPUT 1	NC
2	-INPUT 1	OUTPUT 1
3	+INPUT 1	-INPUT 1
4	$+V_{CC}$	+INPUT 1
5	+INPUT 2	NC
6	-INPUT 2	$+V_{CC}$
7	OUTPUT 2	NC
8	OUTPUT 3	+INPUT 2
9	-INPUT 3	-INPUT 2
10	+INPUT 3	OUTPUT 2
11	$-V_{CC}$	NC
12	+INPUT 4	OUTPUT 3
13	-INPUT 4	-INPUT 3
14	OUTPUT 4	+INPUT 3
15	---	NC
16	---	$-V_{CC}$
17	---	NC
18	---	+INPUT 4
19	---	-INPUT 4
20	---	OUTPUT 4

NC = No connection

FIGURE 1. Terminal connections – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1,2,3,4 1/	1,2,3,4 1/	1,2,3,4 1/
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1 with exception of input offset voltage (V_{IO}).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

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Approved sources of supply for SMD 5962-94602 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9460201QHA	01295	TLE2071MUB
5962-9460201QPA	01295	TLE2071MJGB
5962-9460201Q2A	01295	TLE2071MFKB
5962-9460202QHA	01295	TLE2072MUB
5962-9460202QPA	01295	TLE2072MJGB
5962-9460202Q2A	01295	TLE2072MFKB
5962-9460203QCA	01295	TLE2074MJB
5962-9460203QDA	01295	TLE2074MWB
5962-9460203Q2A	01295	TLE2074MFKB
5962-9460204QDA	01295	TLE2071AMWB
5962-9460204QPA	01295	TLE2071AMJGB
5962-9460204QHA	01295	TLE2071AMUB
5962-9460204Q2A	01295	TLE2071AMFKB
5962-9460205QPA	01295	TLE2072AMJGB
5962-9460205QHA	01295	TLE2072AMUB
5962-9460205Q2A	01295	TLE2072AMFKB

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9460206QCA	01295	TLE2074AMJB
5962-9460206QDA	01295	TLE2074AMWB
5962-9460206Q2A	01295	TLE2074AMFKB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.