

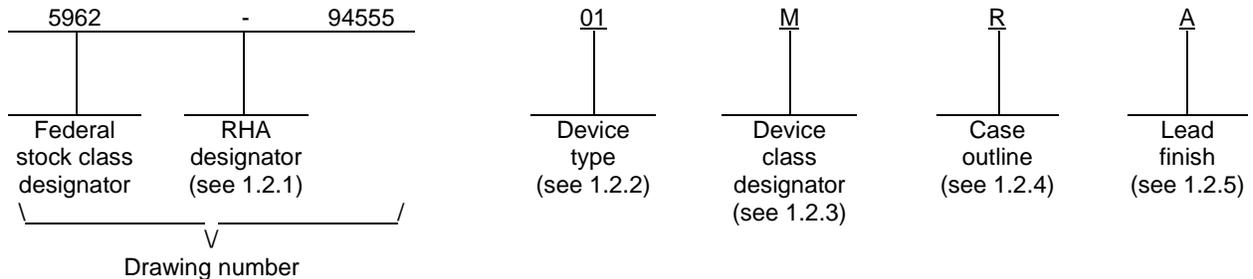
REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	In accordance with N.O.R. 5962-R182-94.	94-04-26	M. A. Frye
B	In accordance with N.O.R. 5962-R192-94.	94-06-01	M. A. Frye
C	In accordance with N.O.R. 5962-R059-95.	95-01-25	M. A. Frye
D	In accordance with N.O.R. 5962-R206-95.	95-10-11	M. A. Frye
E	In accordance with N.O.R. 5962-R094-96.	96-04-10	M. A. Frye
F	In accordance with N.O.R. 5962-R252-97.	97-03-21	R. Monnin
G	Incorporate previous notice of revisions. Redrawn.	97-07-10	R. Monnin
H	Add a footnote to unity gain bandwidth and slew rate tests in table I. Update boilerplate. -rrp	01-05-07	R. Monnin
J	Add footnote <u>3/</u> to tests t_{OD} , t_{DO} , and t_D , in table I. Add footnote <u>6/</u> to tests PS , t_{OS} , and f_{MAX} in table I. - gt	02-04-03	R. Monnin
K	Make change to input supply current test limit as specified under table I. - ro	03-01-10	R. Monnin
L	Add device type 02 and case outline K. Editorial changes throughout. - drw	11-12-14	Charles F. Saffle

REV																			
SHEET																			
REV	L																		
SHEET	15																		
REV STATUS OF SHEETS	REV	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
PMIC N/A	PREPARED BY Rick C. Officer	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p> <p align="center">MICROCIRCUIT, LINEAR, PHASE SHIFT RESONANT CONTROLLER MONOLITHIC SILICON</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY Rajesh R. Pithadia																		
	APPROVED BY Michael A. Frye																		
	DRAWING APPROVAL DATE 94-04-05																		
AMSC N/A	REVISION LEVEL L	SIZE A	CAGE CODE 67268	5962-94555															
		SHEET		1 OF 15															

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>UVLO Turn-on</u>	<u>UVLO Turn-off</u>
01	UC1875	Phase shift resonant controller	10.75 V	9.25 V
02	UC1875	Phase shift resonant controller	10.75 V	9.25 V

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
X	CQCC1-N28B	28	Square leadless chip carrier with thermal pads
3	CQCC1-N28	28	Square leadless chip carrier
K	GDFP2-F24 or CDFP3-F24	24	Flatpack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage (V_C , V_{IN}).....	20 V
Output current, source or sink:	
DC	0.5 A
Pulse (0.5 μ s)	3 A
Analog I/O pins	-0.3 V to 5.3 V
Operating junction temperature (T_J)	150°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case R	7°C/W
Case 3	5.4°C/W
Case K	5.6°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case R	85°C/W
Cases X and 3	65°C/W
Case K	70.14°C/W

1.4 Recommended operating conditions.

Supply voltage (V_C , V_{IN}).....	12 V
Ambient operating temperature (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.4 Timing diagram. The timing diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 116 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Supply current section							
Input current startup	I _{IS}	V _{IN} = 8 V, V _C = 20 V, R _{SLOPE} = open, I _{DELAY} = 0 mA	1,2,3	All		600	μA
Output switch supply current startup	I _{IS}	V _{IN} = 8 V, V _C = 20 V, R _{SLOPE} = open, I _{DELAY} = 0 mA	1,2,3	All		100	μA
Input supply current	I _{IN}		1,2,3	All		44	mA
Output switch supply current	I _C		1,2,3	All		30	mA
Voltage reference section							
Output voltage	V _{OUT}	T _A = +25°C	1	All	4.92	5.08	V
Load regulation	V _{LD}	V _{REF} = -10 mA	1,2,3	All		20	mV
Line regulation	V _{LN}	+V _{IN} = 11 V to 20 V	1,2,3	All		10	mV
Total variation	V _T	Line, load, temperature	1,2,3	All		5.1	V
Error amplifier section							
Offset voltage	V _{IO}		1,2,3	All		15	mV
Input bias current	I _{IB}		1,2,3	All		3	μA
Open loop voltage gain	A _{VOL}	V _{COMP} = 1 V to 4 V	4,5,6	All	60		dB
Common mode rejection ratio	CMRR	V _{CM} = 1.5 V to 5.5 V	4,5,6	All	75		dB
Power supply rejection ratio	PSRR	V _{IN} = 11 V to 20 V	4,5,6	All	85		dB
Output sink current	I _{SI}	V _{COMP} = 1 V	1,2,3	All	1		mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Error amplifier section - Continued							
Output source current	ISO	V _{COMP} = 4 V	1,2,3	All		-0.5	mA
Output voltage, high	V _{OH}	I _{COMP} = -0.5 mA	1,2,3	All	4	5	V
Output voltage, low	V _{OL}	I _{COMP} = 1 mA	1,2,3	All	0	1	V
Unity gain bandwidth <u>3/</u>	UGBW		4,5,6	01	5		MHz
				02	7		
Slew rate <u>3/</u>	SR		4,5,6	All	6		V/μs
Pulse width modulator section							
Zero phase shift voltage	VZPS	<u>4/</u>	1,2,3	All	0.55		V
Pulse width modulator <u>5/ 6/</u> phase shift	PS	V _{COMP} > (ramp peak + ramp offset)	4,5,6	01	98	102	%
				02	96	104	
				All	0	2	
Output skew <u>5/ 6/</u>	t _{OS}	V _{COMP} < 1 V	9,10,11	All		±20	ns
Ramp to output delay <u>3/</u>	t _{OD}		9,10,11	All		125	ns
Oscillator section							
Initial accuracy	IA	T _A = +25°C	4	01	0.85	1.15	MHz
				02	0.85	1.19	
Voltage stability	VS	V _{IN} = 11 V to 20 V	4,5,6	All		2	%
Total variation	VT	Line, temperature	1,2,3	All	0.80	1.20	MHz
Clock output pulse width	t _{CLKO}	R _{CLK/SYNC} = 3.9 kΩ	4,5,6	All		100	ns
Maximum frequency <u>6/</u>	f _{MAX}	R _{fSET} = 5 kΩ	4,5,6	All	2		MHz

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Ramp generator / slope compensation section							
Minimum ramp current	I _{RMIN}	I _{SLOPE} = 10 μA, V _{fSET} = V _{REF}	1,2,3	All		-14	μA
Maximum ramp current	I _{RMAX}	I _{SLOPE} = 1 mA, V _{fSET} = V _{REF}	1,2,3	All	-0.8		mA
Ramp peak, clamping level voltage	V _{CL}	R _{fSET} = 100 kΩ	1,2,3	All	3.8		V
Current limit section							
Input bias current	I _{IB}	C _{+C/S} = 3 V	1,2,3	All		5	μA
Threshold voltage	V _{TH}		1,2,3	All	2.4	2.6	V
Delay to output <u>3/</u>	t _{DO}		9,10,11	All		150	ns
SOFT-START / reset delay section							
Charge current	I _{CH}	V _{S-S} = 0.5 V	1,2,3	All	-20	-3	μA
Discharge current	I _{DCH}	V _{S-S} = 1 V	1,2,3	All	120		μA
Restart threshold voltage	V _{RTH}		1,2,3	All	4.3		V
OUTPUT drivers section							
Output low level voltage	V _{OL}	I _{OUT} = 50 mA	1,2,3	All		0.4	V
Output high level voltage	V _{OH}	I _{OUT} = -50 mA	1,2,3	All		2.5	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
DELAY SET section							
DELAY SET voltage	V _{DS}	I _{DELAY} = -500 μA	1,2,3	All	2.3	2.6	V
DELAY time <u>3/</u>	t _D	I _{DELAY} = -250 μA <u>7/</u>	9,10,11	All	150	600	ns

- 1/ Unless otherwise specified, V_S = +V_{IN} = 12 V, frequency set resistance R_{fSET} = 12 kΩ, frequency set capacitance C_{fSET} = 330 pF, slope resistance R_{SLOPE} = 12 kΩ, ramp capacitance C_{RAMP} = 200 pF, DELAY SET capacitance C_{DS A-B} = C_{DS C-D} = 0.01 μF, DELAY SET current I_{DS A-B} = I_{DS C-D} = -500 μA.
- 2/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
- 3/ Not production tested.
- 4/ Zero phase shift voltage has a temperature coefficient of about -2 mV/°C.
- 5/ Phase shift percentage (0% = 0°, 100% = 180°) is defined as: $\theta = (200/T) \phi \%$. θ is the phase shift, and ϕ and T are defined in figure 3. At 0% phase shift, ϕ is the output skew.
- 6/ Not tested at -55°C but guaranteed by bench testing.
- 7/ Delay time can be programmed via resistors from the delay set pins to ground. Delay time = (62.5×10^{-12}) seconds/ I_{DELAY}. I_{DELAY} = delay set voltage/R_{DELAY}. The recommended range for I_{DELAY} is 25μA ≤ I_{DELAY} ≤ 1 mA.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) T_A = +125°C, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

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Device types	01		02
Case outlines	R	X and 3	K
Terminal number	Terminal symbol		
1	V _{REF}	V _{IN}	N/C
2	E/A OUT (COMP)	POWER GND	V _{REF}
3	E/A (-)	OUTPUT B (OUT B)	E/A OUT (COMP)
4	E/A (+)	OUTPUT A (OUT A)	E/A (-)
5	C/S (+)	N/C	E/A (+)
6	SOFT-START	N/C	C/S (+)
7	DELAY SET C/D	DELAY SET A/B	SOFT-START
8	OUTPUT D (OUT D)	FREQ SET	DELAY SET C/D
9	OUTPUT C (OUT C)	CLOCK/SYNC	OUTPUT D (OUT D)
10	V _C	SLOPE	OUTPUT C (OUT C)
11	V _{IN}	RAMP	V _C
12	POWER GND	N/C	N/C
13	OUTPUT B (OUT B)	N/C	N/C
14	OUTPUT A (OUT A)	GND	V _{IN}
15	DELAY SET A/B	N/C	POWER GND
16	FREQ SET	V _{REF}	OUTPUT B (OUT B)
17	CLOCK/SYNC	E/A OUT (COMP)	OUTPUT A (OUT A)
18	SLOPE	N/C	DELAY SET A/B
19	RAMP	N/C	FREQ SET
20	GND	E/A (-)	CLOCK/SYNC
21	---	E/A (+)	SLOPE
22	---	C/S (+)	RAMP
23	---	SOFT-START	GND
24	---	DELAY SET C/D	N/C
25	---	N/C	---
26	---	OUTPUT D (OUT D)	---
27	---	OUTPUT C (OUT C)	---
28	---	V _C	---

N/C = No connection

FIGURE 1. Terminal connections.

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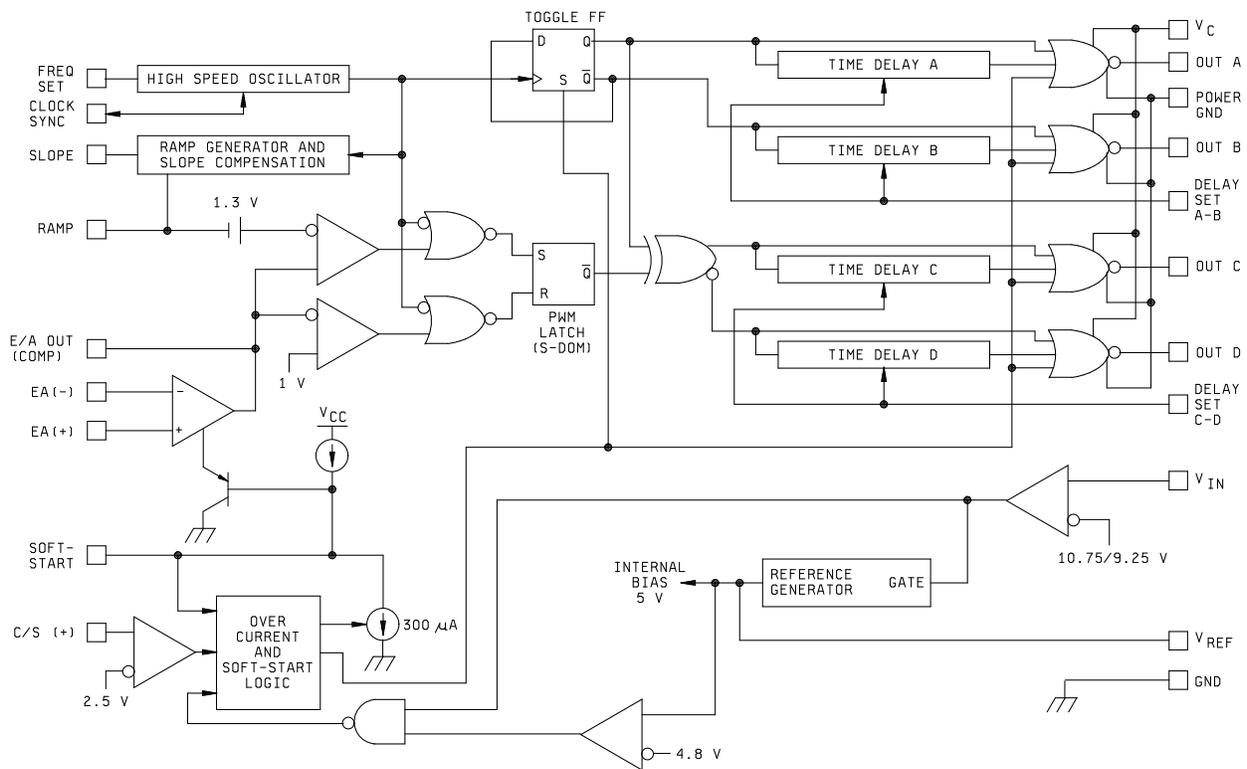


FIGURE 2. Logic diagram.

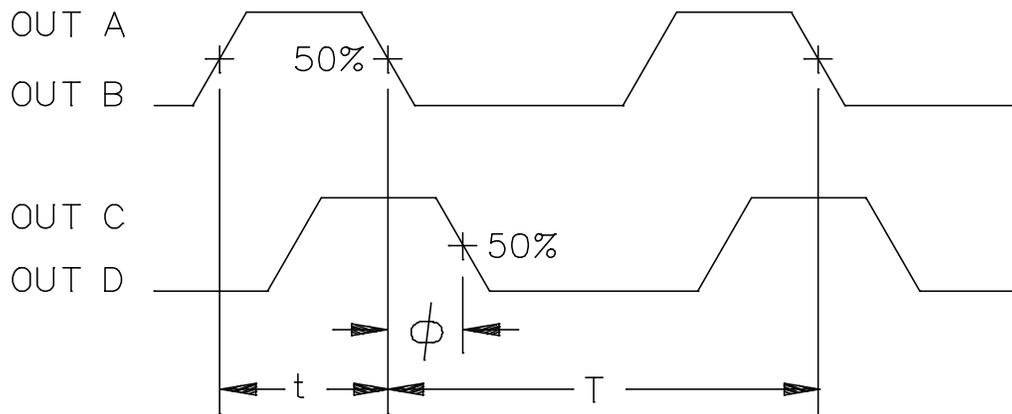
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Phase shift, output skew and delay time definitions.

Duty cycle = t/T . Period = T . $T_{DHL} (A \text{ to } C) = T_{DHL} (B \text{ to } D) = \phi$

FIGURE 3. Timing diagram.

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4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>1/</u>	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>1/</u>	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>1/</u> , <u>2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 4	1, 4	1, 4 <u>2/</u>
Group D end-point electrical parameters (see 4.4)	1, 4	1, 4	1, 4
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test. Delta Limits. $T_A = +25^\circ\text{C}$. 1/

Parameters	Symbol	Device type	Delta Limits
Output switch supply current	I _C	02	+/- 4.4 mA
Reference output voltage	V _{OUT}		+/- 0.0508 V
Error amp offset voltage	V _{IO}		+/- 1.45 mV

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table IIA herein.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions.

GND	Signal ground. All voltages are measured with respect to ground (GND). The timing capacitor, on the FREQ SET pin, and bypass capacitor on the V _{REF} pin, bypass capacitors on V _{IN} and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.
PWR GND	Power ground. V _C should be bypassed with a ceramic capacitor from the V _C pin to the section of the ground plane that is connected to PWR GND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a signal point to optimize noise rejection and minimize DC drops.
V _C	Output switch supply voltage. This pin supplies power to the drivers and their associated bias circuitry. Connect V _C to a stable source above 3 V for normal operation, above 12 V for best performance. This supply should be bypassed directly to the PWR GND pin with low ESR, low ESL capacitors.
V _{IN}	Primary chip supply voltage. This pin supplies power to the logic and analog circuitry on the integrated circuitry that is not directly associated with driving the output stages.
FREQ SET	Oscillator frequency set pin. A resistor and a capacitor from FREQ SET to GND will set oscillator frequency according to the following relationship: $f = 4/(R_{fSET} \times C_{RAMP})$.
CLK/SYNC	Bi-directional clock and synchronization pin. Used as an output, this pin provides a clock signal. As an input, this pin provides a synchronization point.
SLOPE	Set ramp slope compensation. A resistor from this pin to V _{CC} will set the current used to generate the ramp. Connecting this resistor to the DC input line will provide voltage feed forward.

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RAMP	Voltage ramp. This pin is the input to the pulse width modulator comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope: (dV/dT) = (sense voltage/RSLOPE x CRAMP).
E/A OUT (COMP)	Error amplifier output. This is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.
E/A(+)	This pin is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the E/A(-) pin.
E/A(-)	This pin is normally connected to the voltage divider resistors which sense the power supply output level.
SOFT START	SOFT START will remain at GND as long as V _{IN} is below the UVLO threshold. SOFT START will be pulled up to about 4.8 V by an internal 9 μA current source when V _{IN} becomes valid (assuming a non-fault condition). In the event of a current-fault (C/S (+) voltage exceeding 2.5 V), SOFT START will be pulled to GND and then ramp to 4.8 V. If a fault occurs during the SOFT START cycle, the outputs will be immediately disabled and SOFT START must charge fully prior to resetting the fault latch. For paralleled controllers, the SOFT START pins may be paralleled to a single capacitor, but the change currents will be additive.
CURRENT SENSE (+)	The positive input to the current-fault comparator whose reference is set internally to fixed 2.5 V (separate from V _{REF}). When the voltage at this pin exceeds 2.5 V, the current-fault latch is set, the outputs are forced off and a SOFT START cycle is initiated. If a constant voltage above 2.5 V is applied to this pin the outputs are disabled from switching and held in a low state until the C/S (+) pin is brought below 2.5 V. The outputs may begin switching at 0 degrees phase shift before the SOFT START pin begins to rise, this condition will not prematurely deliver power to the load.
OUTPUTS A, B, C, D	The outputs are 2 A totem-pole drivers optimized for both MOSFET gates and level shifting transformers. The outputs operate as pair with a nominal 50% duty cycle. The A-B pair is intended to drive one half bridge in the external power stage and is synchronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with respect to the A-B outputs.
DELAY SET A-B, DELAY SET C-D	Output delay control. The users programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half bridges to accommodate differences in the resonant capacitor charging currents.
VREF	This pin is an accurate 5 V voltage reference. This output is capable of delivering about 60 mA to peripheral circuitry and is internally short circuit current limited.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-12-14

Approved sources of supply for SMD 5962-94555 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9455501M3A	01295	UC1875L/883BC
5962-9455501MRA	01295	UC1875J/883BC
5962-9455501MXA	<u>3/</u>	UC1875LP/883BC
5962-9455501V3A	01295	UC1875LQMLV
5962-9455501VRA	01295	UC1875JQMLV
5962-9455502VKA	01295	UC1875W-SP

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments, Incorporated
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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