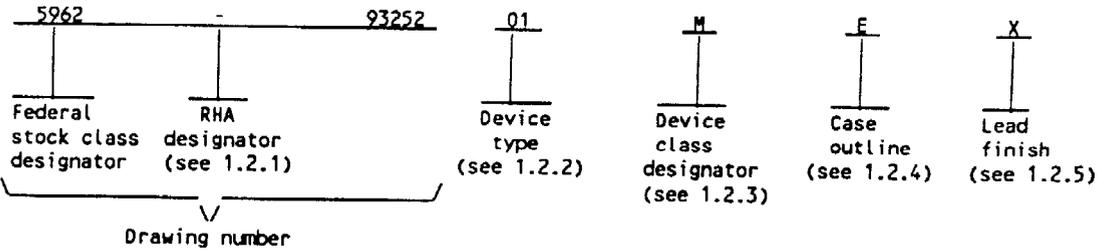


1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54AC2526	1-to-8 minimum skew clock driver with multiplexed clock inputs

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
Z	CQCC1-N20	20	Leadless-chip-carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 2

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage range (V_{OUT})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC input clamp current (I_{IK}):	
$V_{IN} = -0.5$ V	-20 mA
$V_{IN} = V_{CC} + 0.5$ V	+20 mA
DC output clamp current (I_{OK}):	
$V_{OUT} = -0.5$ V	-20 mA
$V_{OUT} = V_{CC} + 0.5$ V	+20 mA
DC output current (I_{OUT}) per output pin	± 50 mA
DC V_{CC} or GND current (I_{CC} , I_{GND}) per pin	± 400 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D)	500 mW

1.4 Recommended operating conditions. 2/ 3/ 4/

Supply voltage range (V_{CC})	+3.0 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL}):	
$V_{CC} = 3.0$ V	0.90 V dc
$V_{CC} = 3.6$ V	1.08 V dc
$V_{CC} = 4.5$ V	1.35 V dc
$V_{CC} = 5.5$ V	1.65 V dc
Minimum high level input voltage (V_{IH}):	
$V_{CC} = 3.0$ V	2.10 V dc
$V_{CC} = 3.6$ V	2.52 V dc
$V_{CC} = 4.5$ V	3.15 V dc
$V_{CC} = 5.5$ V	3.85 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum input edge rate ($\Delta V/\Delta t$)	125 mV/ns
(V_{IN} from 30% to 70% of V_{CC})	
Maximum high level output current (I_{OH}):	
$V_{CC} = 3.0$ V and 3.6 V	-12 mA
$V_{CC} = 4.5$ V and 5.5 V	-24 mA
Maximum low level output current (I_{OL}):	
$V_{CC} = 3.0$ V and 3.6 V	12 mA
$V_{CC} = 4.5$ V and 5.5 V	24 mA

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 5/

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
- 2/ Unless otherwise noted, all voltages are referenced to GND.
- 3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
- 4/ Operation from 0.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery back up systems. Data retention implies no input transitions and no stored data loss with the following conditions: $V_{IH} \geq 70\%$ of V_{CC} , $V_{IL} \leq 30\%$ of V_{CC} , $V_{OH} \geq 70\%$ of V_{CC} at -20 μ A, $V_{OL} \leq 30\%$ of V_{CC} at 20 μ A.
- 5/ Values will be added when they become available from the qualified source.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 3

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATIONS (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of the LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 4

- 3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.
- 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.
- 3.2.3 Truth table. The truth table shall be as specified on figure 2.
- 3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.
- 3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.
- 3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.
- 3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range. Test conditions for these specified characteristics and limits are as specified in table I.
- 3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.
- 3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.
- 3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.
- 3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.
- 3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.
- 3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
- 3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

- 4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
- 4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93252

REVISION LEVEL

SHEET

5

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T _C ≤ +125°C +3.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class 3/	V _{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
High level output voltage 3006	V _{OH1} 5/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -50 μA	All All	3.0 V	1, 2, 3	2.9		V
	V _{OH2} 5/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -50 μA	All All	4.5 V	1, 2, 3	4.4		V
	V _{OH3}	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -50 μA	All All	5.5 V	1, 2, 3	5.4		V
	V _{OH4} 5/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -12 mA	All All	3.0 V	1, 2, 3	2.4		V
	V _{OH5}	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -24 mA	All All	4.5 V	1, 2, 3	3.7		V
	V _{OH6} 5/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -24 mA	All All	5.5 V	1, 2, 3	4.7		V
	V _{OH7} 6/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -50 mA	All All	5.5 V	1, 2, 3	3.85		V
Low level output voltage 3007	V _{OL1} 5/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OL} = 50 μA	All All	3.0 V	1, 2, 3		0.1	V

See footnotes at end of table.

STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93252

REVISION LEVEL

SHEET

6

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T _C ≤ +125°C +3.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class 3/	V _{CC}	Group A subgroups	Limits 4/		Unit	
						Min	Max		
Low level output voltage 3007	V _{OL2} 5/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OL} = 50 μA	All All	4.5 V	1, 2, 3		0.1	V	
	V _{OL3}	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OL} = 50 μA	All All	5.5 V	1, 2, 3		0.1	V	
	V _{OL4} 5/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OL} = 12 mA	All Q, V	3.0 V	1, 3		0.4	V	
					2		0.5		
			All M		1		0.4		
					2, 3		0.5		
	V _{OL5}	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OL} = 24 mA	All Q, V	4.5 V	1, 3		0.4	V	
			2			0.5			
All M			1			0.4			
			2, 3			0.5			
V _{OL6} 5/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OL} = 24 mA	All Q, V	5.5 V	1, 3		0.4	V		
				2		0.5			
		All M		1		0.4			
				2, 3		0.5			
V _{OL7} 6/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND I _{OL} = 50 mA	All All	5.5 V	1, 2, 3		1.65	V		
Positive input clamp voltage 3022	V _{IC+}	For input under test I _{IN} = 1 mA	All Q, V	GND	1	0.4	1.5	V	
Negative input clamp voltage 3022	V _{IC-}	For input under test I _{IN} = -1 mA	All Q, V	Open	1	-0.4	-1.5	V	
Input current high 3010	I _{IH}	For input under test V _{IN} = V _{CC} For all other inputs V _{IN} = V _{CC} or GND	All Q, V	5.5 V	1		0.1	μA	
						2			1.0
					All M	1			0.1
						2, 3			1.0

See footnotes at end of table.

STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93252

REVISION LEVEL

SHEET

7

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T _C ≤ +125°C +3.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class 3/	V _{CC}	Group A subgroups	Limits 4/		Unit	
						Min	Max		
Input current low 3009	I _{IL}	For input under test V _{IN} = GND For all other inputs V _{IN} = V _{CC} or GND	All Q, V	5.5 V	1		-0.1	μA	
						All M	2		
					2, 3				1
Input capacitance 3012	C _{IN}	T _C = +25°C See 4.4.1c	All All	GND	4		10	pF	
Power dissipation capacitance	C _{PD} Z/	For CK0: f _{IN} = 1 MHz V _{IH} = V _{CC} V _{IL} = GND Duty cycle = 50% T _C = +25°C See 4.4.1c	All All	5.0 V	4		850	pF	
Quiescent supply current, output high 3005	I _{CCH}	For all inputs V _{IN} = V _{CC} or GND	All Q, V	5.5 V	1		2.0	μA	
						All M	2		
					2, 3				1
Quiescent supply current, output low 3005	I _{CCL}		All Q, V	5.5 V	1		2.0	μA	
						All M	2		
					2, 3				1
Latch-up input/output over-voltage	I _{CC} (O/V1) B/	t _W ≥ 100 μs, t _{cool} ≥ t _W 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V V _{over} = 10.5 V	All Q, V	5.5 V	2		200	mA	
Latch-up input/output positive over-current	I _{CC} (O/I1+) B/	t _W ≥ 100 μs, t _{cool} ≥ t _W 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V I _{trigger} = +120 mA	All Q, V	5.5 V	2		200	mA	
Latch-up input/output negative over-current	I _{CC} (O/I1-) B/	t _W ≥ 100 μs, t _{cool} ≥ t _W 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V I _{trigger} = -120 mA	All Q, V	5.5 V	2		200	mA	
Latch-up supply over-voltage	I _{CC} (O/V2) B/	t _W ≥ 100 μs, t _{cool} ≥ t _W 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V V _{over} = 9.0 V	All Q, V	5.5 V	2		100	mA	

See footnotes at end of table.

STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93252

REVISION LEVEL

SHEET

8

TABLE 1. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T _C ≤ +125°C +3.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class 3/	V _{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Truth table test output voltage 3014	9/	For all inputs V _{IN} = V _{IH} or V _{IL} Verify output V _{OUT} See 4.4.1b	All All	3.0 V	7, 8	L	H	
				4.5 V	7, 8	L	H	
Propagation delay time, clock to output, CK0 or CK1 to Om 3003	t _{PLH1} , t _{PHL1} 10/	C _L = 50 pF minimum R _L = 500Ω See figure 4	All All	3.0 V	9	4.5	11.0	ns
					10	5.5	13.0	
					11	3.5	10.0	
				4.5 V	9	3.0	8.5	
					10	4.2	10.2	
					11	2.5	8.0	
Propagation delay time, select to output, SEL to Om 3003	t _{PLH2} , t _{PHL2} 10/		All All	3.0 V	9	5.0	12.0	ns
					10	6.0	14.0	
					11	4.0	11.0	
				4.5 V	9	3.5	9.5	
					10	4.7	11.2	
					11	3.0	9.0	
Common edge output skew time, Om to Om 3003	t _{OSHL} , t _{OSLH} 11/ 12/		All All	3.0 V	9, 10, 11		1.5	ns
				4.5 V	9, 10, 11		1.0	
Opposite edge output skew time, Om to Om 3003	t _{OST} 11/ 12/		All All	3.0 V	9, 10, 11		1.5	ns
				4.5 V	9, 10, 11		1.0	
Pin skew time, Om 3003	t _{PS} 11/ 12/		All All	3.0 V	9, 10, 11		1.5	ns
				4.5 V	9, 10, 11		1.0	
Output rise and fall time, Om 3004	t _{RISE} , t _{FALL} 11/		All All	3.0 V	9, 11		4.0	ns
					10		5.0	
				4.5 V	9, 11		3.0	
					10		4.0	

See footnotes on next sheet.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 9

TABLE I. Electrical performance characteristics - Continued.

- 1/ For tests not listed in MIL-STD-883 [e.g. I_{CC} (O/V1)], utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.
- 2/ The values to be used for V_{IH} and V_{IL} shall be the V_{IH} minimum and V_{IL} maximum values listed in section 1.4, herein. Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:
 - a. For V_{IC+} tests, the GND terminal can be open. $T_C = +25^\circ\text{C}$.
 - b. For V_{IC-} tests, the V_{CC} terminal shall be open. $T_C = +25^\circ\text{C}$.
 - c. For all I_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.
- 3/ The word "All" in the device type and device class column means for all device types and classes.
- 4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet the limits specified in table I, as applicable, at $3.0\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ and $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$.
- 5/ For device classes Q and V, this test is guaranteed, if not tested, to the limits specified in table I herein.
- 6/ Transmission driving tests are performed at $V_{CC} = 5.5\text{ V}$ dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{IN}$ or GND, the test is guaranteed for $V_{IN} = V_{IH}$ or V_{IL} .
- 7/ Power dissipation capacitance (C_{PD}) shall be tested by loading all outputs with a 50 pF minimum load capacitance (measured from output pin to GND) and conditioning CK0 with the signal specified in table I, herein. The other input pins, CK1 and SEL are tied to 0.0 V. The resulting I_{CC} current is then measured. C_{PD} is then calculated using the following equation:

$$C_{PD} = \frac{I_{CCD}}{V_{CC} \times 10^6} - 400\text{ pF}$$

where I_{CCD} is the I_{CC} measured.

Under the conditions specified in table I, herein, for CK0 and CK1 over frequencies (f) of 1 MHz to 100 MHz, C_{PD} is guaranteed to meet the limits calculated with the following equation:

$$C_{PD} = 850\text{ pF} - (1.2 \times 10^{-18} \times f)$$

C_{PD} determines both the power consumption (P_D) and current consumption (I_S). Where

$$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$$

$$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC}$$

and f is the frequency of the input signal and C_L is the external output load capacitance.

- 8/ See JEDEC Standard No. 17 for electrically induced latch-up test methods and procedures. The values listed for $V_{trigger}$, $I_{trigger}$, and V_{over} are to be accurate within ± 5 percent.
- 2/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. For $V_{CC} = 4.5\text{ V}$ and 5.5 V , $H \geq 2.5\text{ V}$ and $L < 2.5\text{ V}$. For $V_{CC} = 3.0\text{ V}$ and 3.6 V , $H \geq 1.5\text{ V}$ and $L < 1.5\text{ V}$. Alternatively, for any value of V_{CC} , $H \geq 0.50V_{CC}$ and $L < 0.50V_{CC}$ are acceptable. For all device classes, functional tests at $V_{CC} = 3.0\text{ V}$, 3.6 V , and 5.5 V are guaranteed, if not tested. Tests at $V_{CC} = 3.0\text{ V}$ are required for RHA specified devices only ($T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$). Functional tests may be performed using the allowable relaxations, per MIL-STD-883, of V_{IH} minimum -0, +20% and V_{IL} maximum -50, +0% (i.e., at $V_{CC} = 3.0\text{ V}$, V_{IH} minimum +20% = 2.52 V and V_{IL} maximum -50% = 0.45 V; at $V_{CC} = 4.5\text{ V}$, V_{IH} minimum +20% = 3.78 V and V_{IL} maximum -50% = 0.68 V), and guarantee this test with input levels of V_{IH} minimum and V_{IL} maximum.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 10

TABLE I. Electrical performance characteristics - Continued.

- 10/ AC limits at $V_{CC} = 5.5$ V are equal to the limits at $V_{CC} = 4.5$ V and guaranteed by testing at $V_{CC} = 4.5$ V. AC limits at $V_{CC} = 3.6$ V are equal to the limits at $V_{CC} = 3.0$ V and guaranteed by testing at $V_{CC} = 3.0$ V. Minimum propagation delay time limits for $V_{CC} = 5.5$ V and $V_{CC} = 3.6$ V are guaranteed by guardbanding the minimum limits for testing at $V_{CC} = 4.5$ V and $V_{CC} = 3.0$ V, respectively, to 0.5 ns greater than the limits specified in table I, herein. For propagation delay tests, all paths must be tested.
- 11/ This test is required only for Group A testing. These tests shall be measured only for initial qualification and after process or design changes which may affect dynamic performance (see 4.4.1 herein).
- 12/ For skew parameters, t_{OSLH} is the absolute value of the difference between the t_{PLH} of an output O_m and the t_{PLH} of any other output O_n ; t_{OSHL} is the absolute value of the difference between the t_{PHL} of an output O_m and the t_{PHL} of any other output O_n ; t_{OST} is the absolute value of the difference between the maximum t_{PLH} of any output O_m and with the minimum t_{PHL} of any output O_n , and also the absolute value of the difference between the maximum t_{PHL} of any output O_m and with the minimum t_{PLH} of any output O_n ; and t_{PS} is the absolute value of the difference between the t_{PHL} and t_{PLH} of any output O_m . The limits for t_{OST} specified in table I, herein, apply to either of the two test conditions for t_{OST} as described herein. For all skew parameters, $m = 0$ to 7; $n = 0$ to 7; and m is not equal to n .

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 11

Device type	01	
Case outlines	E, F	2
Terminal number	Terminal symbol	
1	00	NC
2	02	00
3	NC	02
4	GND	NC
5	V _{CC}	GND
6	SEL	NC
7	04	V _{CC}
8	06	SEL
9	07	04
10	05	06
11	CK1	NC
12	GND	07
13	V _{CC}	05
14	CK0	CK1
15	03	GND
16	01	NC
17	---	V _{CC}
18	---	CK0
19	---	03
20	---	01

Terminal descriptions	
Terminal symbol	Description
CK0, CK1	Clock inputs
SEL	Select input
On (n = 0 to 7)	Outputs

FIGURE 1. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 12

Inputs			Outputs
CK0	CK1	SEL	On
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

H = High voltage level
L = Low voltage level
X = Irrelevant

FIGURE 2. Truth table.

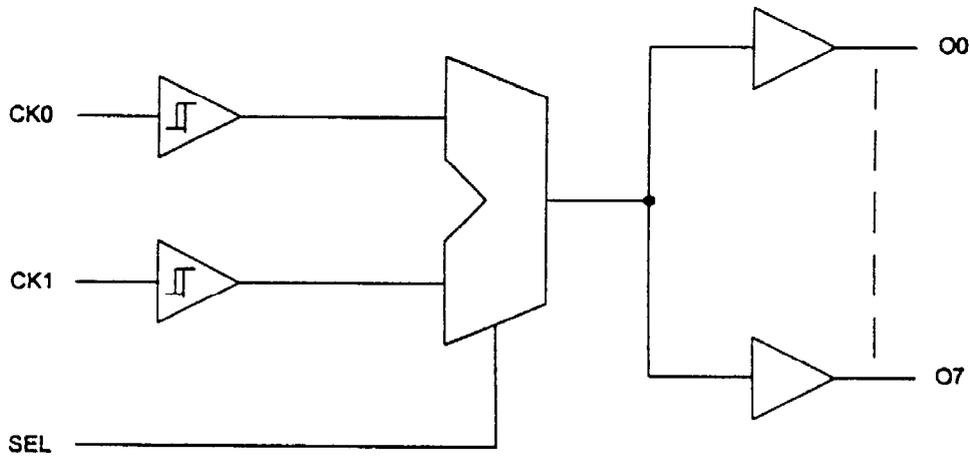


FIGURE 2. Logic diagram.

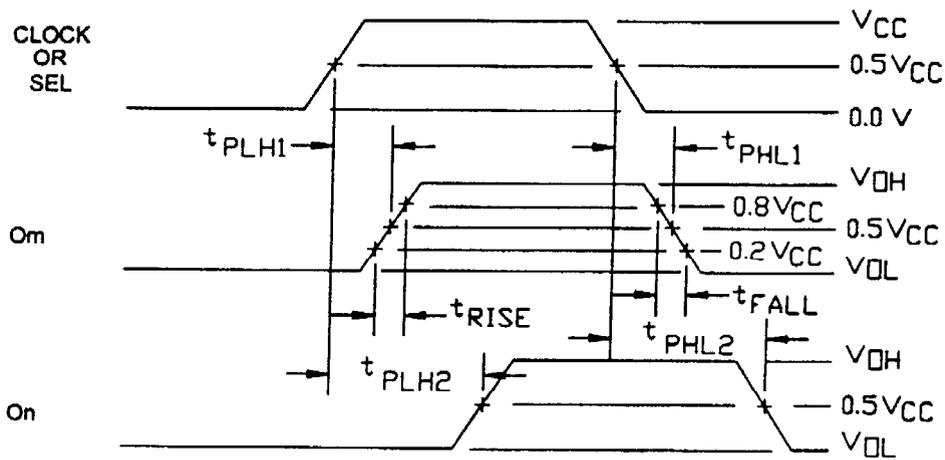
STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93252

REVISION LEVEL

SHEET
13



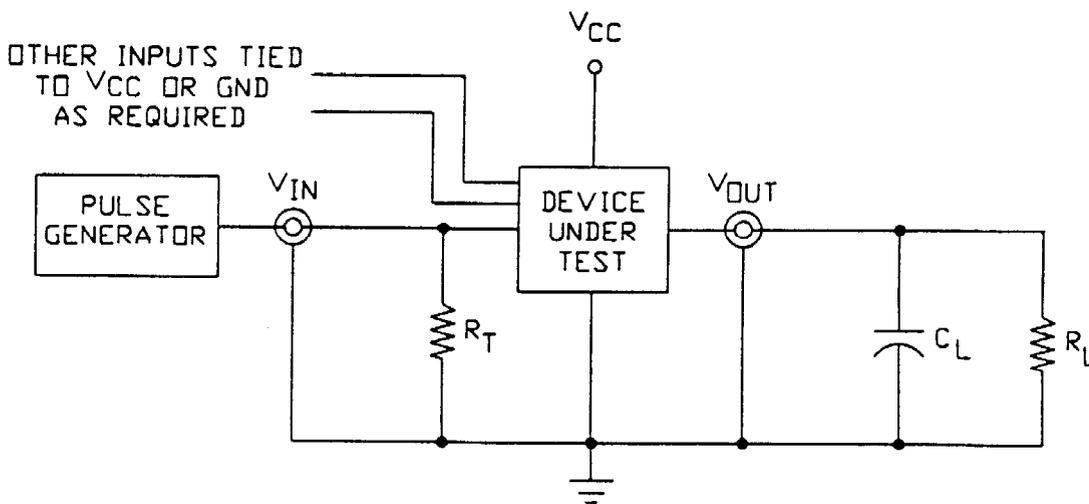
$$t_{OSHL} = |t_{PHL1} - t_{PHL2}|$$

$$t_{OSLH} = |t_{PLH1} - t_{PLH2}|$$

$$t_{OST} = |t_{PLH1} - t_{PHL2}| \text{ and } |t_{PHL1} - t_{PLH2}|$$

$$t_{PS} = |t_{PLH1} - t_{PHL1}|$$

t_{PHL1} and t_{PLH1} are the t_{PHL} and t_{PLH} , respectively, for the output under test, O_m . t_{PHL2} and t_{PLH2} are the t_{PHL} and t_{PLH} , respectively, for any other output, O_n . Where $m = 0$ to 7 , $n = 0$ to 7 , and m is not equal to n .



NOTES:

1. $C_L = 50$ pF minimum or equivalent (includes test jig and probe capacitance).
2. $R_L = 500\Omega$ or equivalent.
3. $R_T = 50\Omega$ or equivalent.
4. Input signal from pulse generator: $V_{IN} = 0.0$ V to V_{CC} ; $PRR \leq 10$ MHz; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns; t_r and t_f shall be measured from 10% of V_{CC} to 90% of V_{CC} and from 90% of V_{CC} to 10% of V_{CC} , respectively; duty cycle = 50 percent. For t_{OSHL} , t_{OSLH} , t_{OST} , t_{PS} , t_{RISE} , and t_{FALL} , $PRR \leq 100$ MHz.
5. The t_{PHL} and t_{PLH} parameters shall be tested at a minimum input frequency of 1 MHz. The t_{OSHL} , t_{OSLH} , t_{OST} , t_{PS} , t_{RISE} , and t_{FALL} parameters shall be tested at a minimum input frequency of 10 MHz.
6. The outputs are measured one at a time.

FIGURE 5. Switching waveforms and test circuit.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 14

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A = +125^\circ\text{C}$, minimum.

(3) For device class M, unless otherwise noted, method 1015 of MIL-STD-883 shall be followed.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall test all possible input to output logic patterns. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{PD} , test all applicable pins on five devices with zero failures.

d. Latch-up tests are required for device classes Q and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. Test all applicable pins on five devices with zero failures.

e. The t_{OSHL} , t_{OSLH} , t_{OST} , t_{PS} , t_{RISE} , and t_{FALL} tests shall be measured only for initial qualification and after process or design changes which may affect dynamic performance. Test twelve devices at $T_C = -55^\circ\text{C}$, $+25^\circ\text{C}$, and $+125^\circ\text{C}$, with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

STANDARD
MICROCIRCUIT DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-93252

REVISION LEVEL

SHEET

15

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3 3/	1, 2, 3, 7, 8 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

- 1/ PDA applies to subgroup 1.
- 2/ PDA applies to subgroups 1 and 7.
- 3/ Delta limits shall be required only on table I, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table III.

TABLE III. Delta limits at +25°C.

Parameter 1/	Device types	Limits
I_{CCH}, I_{CCL}	All	± 100 nA

- 1/ These parameters shall be recorded before and after the required burn-in and life test to determine the delta limits.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 16

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and RHA levels for device class M shall be M and D.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331, and as follows:

GND	Ground zero voltage potential.
I_{CC}	Quiescent supply current.
I_{IL}	Input current low.
I_{IH}	Input current high.
T_C	Case temperature.
T_A	Ambient temperature.
V_{CC}	Positive supply voltage.
C_{IN}	Input terminal-to-GND capacitance.
C_{PD}	Power dissipation capacitance.
V_{IC+}	Positive input clamp voltage.
V_{IC-}	Negative input clamp voltage.
t_w	Trigger duration (width).
O/V	Latch-up over-voltage.
O/I	Latch-up over-current.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 17

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings.	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93252
		REVISION LEVEL	SHEET 18

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-11-17

Approved sources of supply for SMD 5962-93252 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 and QML-38535 during the next revision. MIL-BUL-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103 and QML-38535.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9325201QFA	27014	54AC2526FMQB
5962-9325201VFA	27014	54AC2526W-QMLV

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

27014

Vendor name
and address

National Semiconductor
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Point of contact: 333 Western Avenue
South Portland, ME 04106

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