REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R281-94.	94-10-07	Monica L. Poelking
B	Update boilerplate to MIL-PRF-38535 requirements. Update figure 4 waveforms and notes. - CFS	05-05-09	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-07-17	Thomas M. Hess
D	Update boilerplate to MIL-PRF-38535 requirements. - DRH	23-10-24	Muhammad A. Akbar

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV																						
SHEET																						
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D					
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17					

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
93-10-18

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL, CMOS, TEST BUS CONTROLLER, MONOLITHIC SILICON

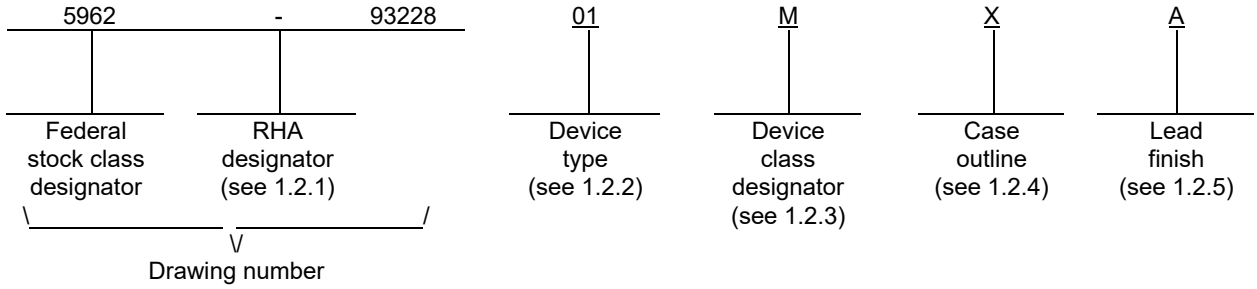
AMSC N/A	REVISION LEVEL D	SIZE A	CAGE CODE **67268**	**5962-93228**
		SHEET	1 OF 17	

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT8990	Test bus controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	68	Ceramic quad flat pack
Y	CMGA15-P69	69	Pin grid array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7.0 V dc
Input voltage range	-0.5 V dc to V_{CC}
Output voltage range	-0.5 V dc to V_{CC}
Input clamp current	±20 mA
Output clamp current	±20 mA
Continuous output current	±25 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline X	1.856°C/W
Case outline Y	See MIL-STD-1835
Power dissipation (P_D)	980 mW

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V ≤ V_{CC} ≤ 5.5 V
High level input voltage (V_{IH})	2 V minimum
Low level input voltage (V_{IL})	0.8 V maximum
Input voltage (V_{IN})	0 V to V_{CC}
Output voltage (V_{OUT})	0 V to V_{CC}
High level output current (I_{OH})	-8 mA
Low level output current (I_{OL})	8 mA
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at https://www.ieee.org/.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. Device type 01 shall be compliant with IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH1}	I_{OH} = -20 µA, V_{CC} = 4.5 V	1, 2, 3	All	4.4		V
		I_{OH} = -8 mA, V_{CC} = 4.5 V			3.7		
High level output voltage	V_{OH2}	I_{OH} = -20 µA, V_{CC} = 5.5 V	1, 2, 3	All	5.4		V
		I_{OH} = -8 mA, V_{CC} = 5.5 V			4.7		
Low lever output voltage	V_{OL}	I_{OL} = 20 µA, V_{CC} = 4.5 V, 5.5 V	1, 2, 3	All		0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V, 5.5 V				0.5	
Input current, ADRS, $\overline{RD}$, $\overline{WR}$, $\overline{TCKI}$	I_{I1}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V	1, 2, 3	All		±1	µA
Input current, $\overline{TDI}$, $\overline{TOFF}$, $\overline{TRST}$	I_{I2}	V_{IN} = V_{CC}, V_{CC} = 5.5 V	1, 2, 3	All		±1	µA
		V_{IN} = GND, V_{CC} = 5.5 V				±250	
High-impedance state output current ($\overline{INT}$, $\overline{RDY}$, TCKO, TDO, TMS)	I_{OZ1}	V_{OUT} = V_{CC} or GND V_{CC} = 5.5 V	1, 2, 3	All		±10	µA
High-impedance state output current (DATA, TMS/EVENT)	I_{OZ2}	V_{OUT} = V_{CC}, V_{CC} = 5.5 V	1, 2, 3	All		±10	µA
		V_{OUT} = GND, V_{CC} = 5.5 V				±250	
Supply current	I_{CC}	V_{IN} = V_{CC} or GND, I_O = 0 V_{CC} = 5.5 V	1, 2, 3	All		450	µA
Input capacitance	C_{IN}	See 4.4.1.c	4	All		5.5	pF
Input/output capacitance	$C_{I/O}$	See 4.4.1.c	4	All		8.4	pF
Output capacitance	C_{OUT}	See 4.4.1.c	4	All		5.7	pF
Functional test		See 4.4.1.b	7, 8	All			
Clock frequency	f_{clock}		9, 10, 11	All		30	MHz
Pulse duration	t_w	WR low	9, 10, 11	All	5.5		ns
		Event high or low			8		
		TCKI high or low			10.5		
		TRST low			6		
Setup time	t_{su}	ADRS before WR↑	9, 10, 11	All	6.5		ns
		DATA before WR↑			6		
		EVENT before TCKI↑			6		
		EVENT before TCKI↓			5		
		TDI before TCKI↑			2		
		TDI before TCKI↓			2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time	t_h	ADRS after WR↑	9, 10, 11	All	5.5		ns
		DATA after WR↑			5.5		
		EVENT after TCKI↑			5.5		
		EVENT after TCKI↓			5		
		TDI after TCKI↑			4		
		TDI after TCKI↓			4		
Maximum frequency	f_{MAX}	$V_{CC} = 5.0\ V$, $T_A = 25°C$	9, 10, 11	All	30		MHz
ADRS to DATA	t_{PLH1}, t_{PHL1}	See figure 4. $V_{CC} = 4.5\ V$	9, 10, 11	All	8	43	ns
RD↑ to RDY	t_{PLH2}				5.3	17	
WR↑ to RDY	t_{PLH3}				2.5	16	
TCKI↑ to INT	t_{PLH4}				3.7	16	
	t_{PHL4}				5.5	15	
TCKI↑ to RDY	t_{PHL5}				4.4	15	
TCKI↑ to TCKO	t_{PLH5}				3.3	17	
TCKI↓ to TCKO	t_{PLH6}				2.3	19	
TCKI↓ to TCKO	t_{PHL6}				3.6	17	
TCKI↓ to TDO	t_{PLH7}				2.9	19	
	t_{PHL7}				5.2	20	
TCKI↓ to TMS	t_{PLH8}				3.1	19	
	t_{PHL8}				5.1	19	
TCKI↓ to TMS/EVENT	t_{PLH9}				1.5	19	
	t_{PHL9}				3.5	20	
RD↓ to DATA	t_{PZH1}				3.8	21	
	t_{PZL1}				6.8	28	
TCKI↑ to INT	t_{PZH2}				4.9	19	
TCKI↑ to RDY	t_{PZH3}				3.6	19	
TCKI↓ to TCKO	t_{PZH4}				4.1	23	
	t_{PZL4}				4.8	20	
TCKI↓ to TDO	t_{PZH5}				4.3	22	
	t_{PZL5}				5	20	
TCKI↓ to TMS	t_{PZH6}				4.6	23	
	t_{PZL6}				5.1	20	
TCKI↓ to TMS/EVENT	t_{PZH7}				2	21	
	t_{PZL7}				3.2	20	
TOFF↑ to TCKO	t_{PZH8}				4.6	16	
	t_{PZL8}				3.1	14	
TOFF↑ to TDO	t_{PZH9}				4.4	15	
	t_{PZL9}				3.5	14	

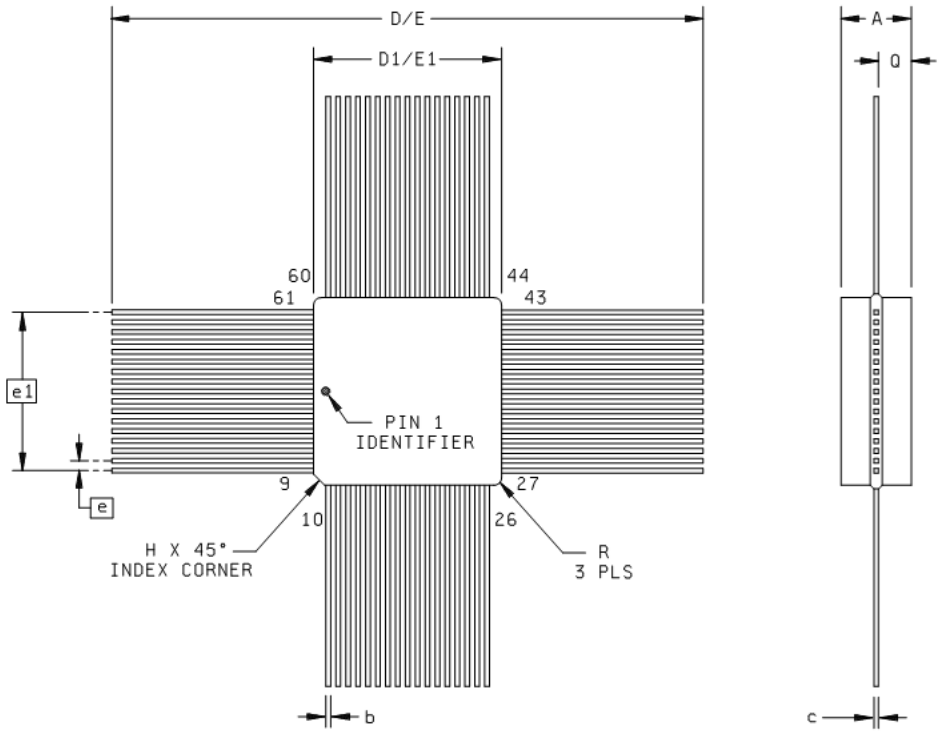
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TOFF↑ to TMS	t_{PZH10}	See figure 4.	9, 10, 11	All	3.1	16.2	ns
	t_{PZL10}	V_{CC} = 4.5 V			1.9	16.7	
TOFF↑ to TMS/EVENT	t_{PZH11}				2.3	15.3	
	t_{PZL11}				2.7	16.4	
RD↑ to DATA	t_{PHZ12}				3.8	18.4	
	t_{PLZ12}				4.1	17.1	
TCKI↓ to TCKO	t_{PHZ13}				6.7	20.4	
	t_{PLZ13}				4.8	21.1	
TCKI↓ to TDO	t_{PHZ14}				5.1	21.7	
	t_{PLZ14}				5	20.7	
TCKI↓ to TMS	t_{PHZ15}				6.9	22.4	
	t_{PLZ15}				4.6	20.6	
TCKI↓ to TMS/EVENT	t_{PHZ16}				4.7	22.5	
	t_{PLZ16}				2.8	20.5	
TOFF↓ to TCKO	t_{PHZ17}				5	15.6	
	t_{PLZ17}				4.4	15.5	
TOFF↓ to TDO	t_{PHZ18}				5.6	16.6	
	t_{PLZ18}				4.6	15.4	
TOFF↓ to TMS	t_{PHZ19}				4.8	19.1	
	t_{PLZ19}				4.4	17	
TOFF↓ to TMS/EVENT	t_{PHZ20}				4.5	18.8	
	t_{PLZ20}				2.4	17.1	
TRST↓ to DATA	t_{PHZ21}				5.7	23	
	t_{PLZ21}				4.2	20.3	
TRST↓ to INT	t_{PHZ22}				6	19.6	
	t_{PLZ22}				6.1	18	
TRST↓ to RDY	t_{PHZ23}				6.5	18.8	
	t_{PLZ23}				4.8	17.8	
TRST↓ to TMS/EVENT	t_{PHZ24}				6	21.1	
	t_{PLZ24}				4.2	20	

1/ The following signals are active low: $\overline{RD}$, $\overline{RDY}$, $\overline{WR}$, $\overline{INT}$, $\overline{TOFF}$, and $\overline{TRST}$. Unless otherwise specified, al test conditions shall be the worst case conditions.

Case X



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.404	3.912	.134	.154
b	.203	.330	.008	.013
c	.127	.178	.005	.007
D/E	33.02	38.10	1.300	1.500
D1/E1	12.32	12.70	.485	.500
e	.635 BSC		.025 BSC	
e1	10.160 BSC		.400 BSC	
H	1.02 BSC		.040 BSC	
Q	1.524	2.032	.060	.080
R	.51 BSC		.020 BSC	

FIGURE 1. Case outlines.

Device types:	01		
Case outline:	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	35	V_{CC}
2	ADRS0	36	DATA14
3	NC	37	NC
4	ADRS1	38	DATA15
5	ADRS2	39	$\overline{TOFF}$
6	NC	40	NC
7	ADRS3	41	TDI0
8	ADRS4	42	TDI1
9	NC	43	NC
10	NC	44	NC
11	DATA0	45	TCK1
12	DATA1	46	TCK0
13	NC	47	NC
14	DATA2	48	TDO
15	DATA3	49	TMS0
16	NC	50	NC
17	DATA4	51	TMS1
18	GND	52	GND
19	V_{CC}	53	V_{CC}
20	NC	54	NC
21	DATA5	55	TMS2/EVENT0
22	DATA6	56	TMS3/EVENT1
23	NC	57	NC
24	DATA7	58	TMS4/EVENT2
25	DATA8	59	TMS5/EVENT3
26	NC	60	NC
27	NC	61	NC
28	DATA9	62	$\overline{TRST}$
29	DATA10	63	$\overline{WR}$
30	NC	64	NC
31	DATA11	65	$\overline{RD}$
32	DATA12	66	$\overline{RDY}$
33	NC	67	NC
34	DATA13	68	$\overline{INT}$

NC = No connection

FIGURE 2. Terminal connections.

Device types:	01		
Case outline:	Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
A2	NC	F2	NC
A3	ADDR4	F10	GND
A4	NC	F11	NC
A5	ADDR1	G1	DATA5
A6	ADDR0	G2	NC
A7	NC	G10	NC
A8	$\overline{INT}$	G11	TMS1
A9	$\overline{RD}$	H1	NC
A10	$\overline{TRST}$	H2	DATA6
B1	DATA0	H10	TDO
B2	NC	H11	TMS0
B3	ADDR3	J1	DATA8
B4	ADDR2	J2	DATA7
B5	NC	J10	TCK0
B6	NC	J11	NC
B7	GND	K1	NC
B8	$\overline{RDY}$	K2	NC
B9	$\overline{WR}$	K3	DATA10
B10	NC	K4	DATA11
B11	NC	K5	NC
C1	DATA2	K6	NC
C2	DATA1	K7	V_{CC}
C3	NC	K8	DATA15
C10	TMS4	K9	TDI0
C11	TMS5	K10	NC
D1	DATA4	K11	TCKI
D2	DATA3	L2	DATA9
D10	TMS3	L3	NC
D11	NC	L4	DATA12
E1	NC	L5	DATA13
E2	GND	L6	NC
E10	V_{CC}	L7	DATA14
E11	TMS2	L8	TOFF
F1	V_{CC}	L9	TDI1
		L10	NC

NC = No connection

FIGURE 2. Terminal connections - Continued.

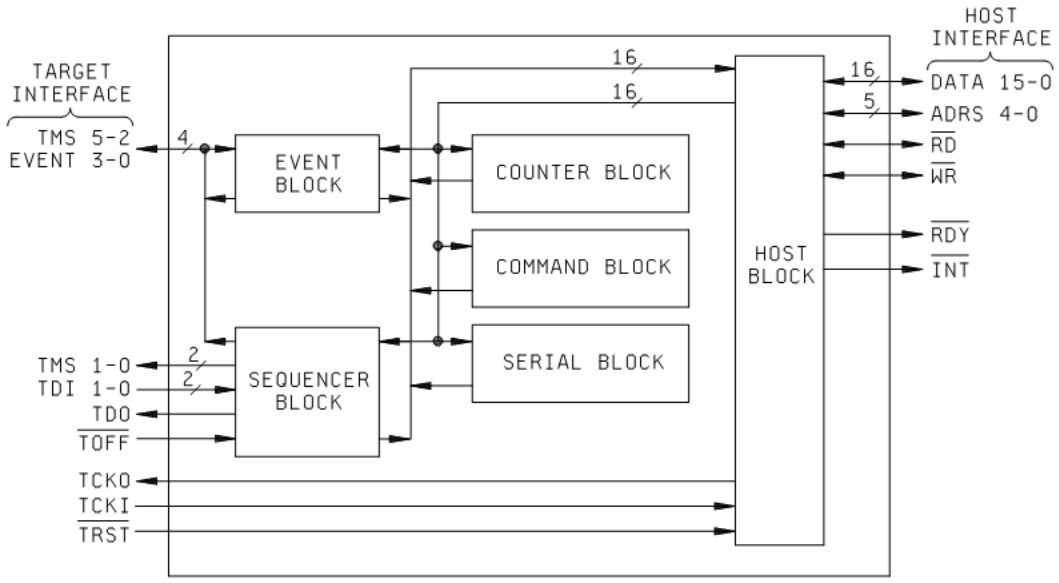
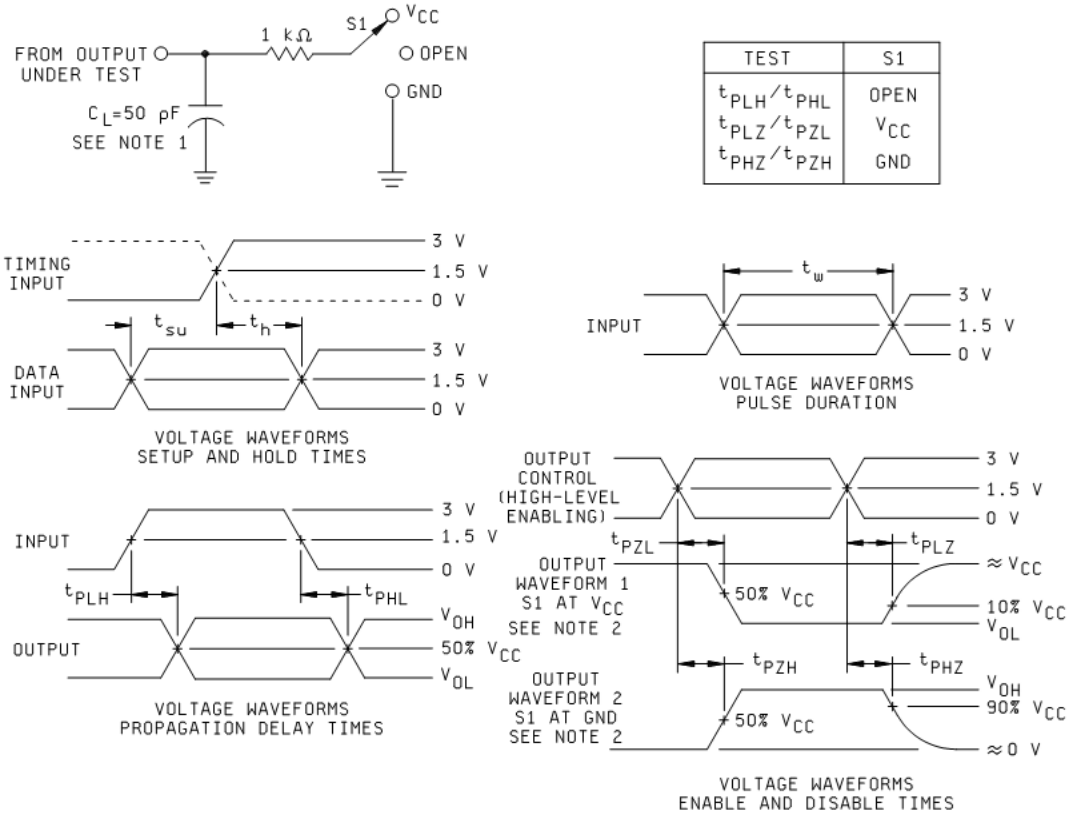


FIGURE 3. Functional block diagram.



Notes:

1. CL includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: t_r = t_f = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
4. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

6.7 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in table III as follows:

TABLE III. Pin descriptions.

Pin name	Description
ADRS(4-0)	The address input pins form the 5-bit address bus used to interface the Test Bus Controller (TBC) to its host. The TBC register to be written to or read from is selected via the address bus.
DATA(15-0)	The data pins form the 16-bit bidirectional data bus used to interface the TBC to its host. Information is written to and read from the TBC registers via the data bus.
$\overline{\text{INT}}$	The interrupt output pin transmits an interrupt signal to the host.
$\overline{\text{RD}}$	The read input pin is the output enable for the data bus. It is used as the strobe for reading data from the selected TBC register.
$\overline{\text{RDY}}$	The ready output pin transmits a status signal to the host. When the TBC is ready to accept read or write operations from the host, $\overline{\text{RDY}}$ is asserted. Otherwise, when the TBC is in recovery from a read, write, command, or reset operation, $\overline{\text{RDY}}$ is not asserted.
$\overline{\text{TOFF}}$	The test off input pin is the output enable for all output and I/O pins of the target interface.
$\overline{\text{TRST}}$	The test reset pin is used to initiate hardware and software reset operations of the TBC. Hardware reset begins when $\overline{\text{TRST}}$ is asserted. Software reset begins when $\overline{\text{TRST}}$ is released and proceeds synchronously to the test clock input (TCKI), completing in a predetermined number of cycles.
$\overline{\text{WR}}$	The write input pin is the strobe for writing data to a TBC data register. Signals present at the data and address buses are captured on the rising edge of $\overline{\text{WR}}$.
TCKI	The test clock input pin is the clock input for the TBC. Most operations of the TBC are synchronous to TCKI. When enabled, all target interface outputs change on the falling edge of TCKI. Sampling of target interface inputs may be configured to occur on either the rising edge or falling edge of TCKI.
TCKO	The test clock output pin distributes the test clock to the target(s). The TCKO pin may be configured to be disabled, constant zero, constant one, or to follow TCKI. When TCKO follows TCKI, it delays the test clock signal to match the delay of generating the test data output (TDO) and test mode select (TMS) signals.
TDI(1-0)	The test data input pins are the serial inputs for shifting test data from the target(s). The TDI inputs may be directly connected to the TDO pins of the target(s).
TDO	The test data output pin is the serial output for shifting test data into the target(s). The TDO output may be directly connected to the TDO pins of the target(s).
TMS(1-0)	The test mode select output pins transmit TMS signals to the target(s), thereby directing them through their test access port (TAP) controller states. The TMS outputs may be directly connected to the TMS pins of the target(s).
TMS(5-2)/EVENT(3-0)	The test mode select/event pins may be configured for use as either test mode select outputs or event I/O pins. As test mode select outputs, they function similarly to the TMS(1-0) pins above. As event I/O pins, they can be used to receive/transmit interrupt signals to/from the target(s).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-10-24

Approved sources of supply for SMD 5962-93228 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9322801MXA	01295	SNJ54ACT8990HV
5962-9322801MYA	01295	SNJ54ACT8990GB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.