REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R085-95.	95-03-07	M. A. Frye
B	Changes in accordance with NOR 5962-R067-99.	99-06-07	R. Monnin
C	Update boilerplate to reflect current requirements. Redrawn. -rrp	02-04-30	R. Monnin
D	Redraw. Remove class M requirements throughout. Update paragraphs to MIL-PRF-38535 requirements. - drw	14-05-02	Charles F. Saffle
E	Update paragraphs to current MIL-PRF-38535 requirements. - drw	20-01-30	James R. Eschmeyer

REV																				
SHEET																				
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SHEET																				

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

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DRAWING APPROVAL DATE
94-04-01

REVISION LEVEL
E

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, LINEAR, BUS TRANSCEIVER, DIFFERENTIAL, MONOLITHIC SILICON

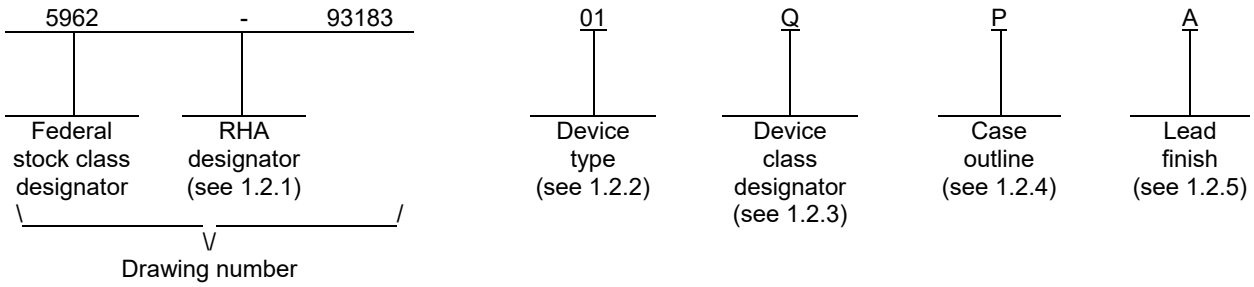
SIZE	CAGE CODE	
A	**67268**	**5962-93183**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	55LBC176	Differential bus transceivers

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC}) 2/	7 V dc
Voltage range at any bus terminal	-10 V dc to 15 V dc
Enable input voltage	5.5 V
Storage temperature range	-65°C to +150°C
Lead temperature, soldering 1.6 mm (1/16 inch) from case for 10 seconds	+260°C
Power dissipation (P_D):	
Case P 3/	1050 mW
Case 2 3/	1375 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range, (V_{CC})	4.75 V dc min, 5.25 V dc max
Voltage at any bus terminal (separately or common mode), (V_I or V_{IC})	-7 V dc min, 12 V dc max
High level input voltage, (V_{IH}) D, DE, and $\overline{RE}$	2 V dc min
Low level input voltage, (V_{IL}) D, DE, and $\overline{RE}$	0.8 V dc max
Differential input voltage, (V_{ID}) 4/	±12 V dc max
High level output current, (I_{OH}) Driver	-60 mA max
Receiver	-400 µA max
Low-level output current, (I_{OL}) Driver	60 mA max
Receiver	8 mA max
Operating ambient temperature (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
3/ Above T_A = 25°C, derate at a factor of 8.4 mW/°C for case P and 11.0 mW/°C for case 2.
4/ Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DRIVER SECTION							
Input clamp voltage	V_{IC}	I_I = -18 mA	1, 2, 3	01		-1.5	V
Output voltage	V_O	I_O = 0	1, 2, 3	01	0	6	V
Differential output voltage	$\|V_{OD1}\|$	I_O = 0	1, 2, 3	01	1.5	6	V
Differential output voltage	$\|V_{OD2}\|$	R_L = 54Ω	1, 2, 3	01	1.1		V
Differential output voltage	V_{OD3}	V_{test} = -7 V to 12 V	1, 2, 3	01	1.1		V
Change in magnitude of differential output voltage 1/	$\Delta\|V_{OD}\|$	R_L = 54Ω and 100Ω	1, 2, 3	01		±0.2	V
Common-mode output voltage 2/	V_{OC}	R_L = 54Ω and 100Ω	1, 2, 3	01	-1	3	V
Change in magnitude of common-mode output voltage 1/	$\Delta\|V_{OC}\|$	R_L = 54Ω and 100Ω	1, 2, 3	01		±0.2	V
Output current 3/	I_O	Output disabled, V_O = 12 V	1, 2, 3	01		1	mA
		Output disabled, V_O = -7 V				-0.8	
High-level input current	I_{IH}	V_I = 2.4 V	1, 2, 3	01		-100	µA
Low-level input current	I_{IL}	V_I = 0.4 V	1, 2, 3	01		-100	µA
Supply current, receiver disabled and driver enabled	I_{CC1}	V_I = 0 or V_{CC}, No load	1, 2, 3	01		1.75	mA
Supply current, receiver and driver disabled	I_{CC2}	V_I = 0 or V_{CC}, No load	1, 2, 3	01		0.25	mA
Functional tests	FT	See 4.4.1b	7, 8	01			
Short-circuit output current	I_{OS}	V_O = -7 V	1, 2, 3	01		-250	mA
		V_O = 0 V				-150	
		$V_O = V_{CC}$				250	
		V_O = 12 V				250	
Differential-output delay time	t_{DDH}/ t_{DDL}	R_L = 54Ω, C_L = 50 pF, See figure 3	9, 10, 11	01	8	31	ns
Pulse skew ($\|t_{DDH} - t_{DDL}\|$)	$t_{sk(p)}$	R_L = 54Ω, C_L = 50 pF, See figure 3	9, 10, 11	01		10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DRIVER SECTION – continued							
Output enable time to high level	t_{PZH}	$R_L = 110\Omega$, $C_L = 50$ pF, See figure 3	9, 10, 11	01		65	ns
Output enable time to low level	t_{PZL}	$R_L = 110\Omega$, $C_L = 50$ pF, See figure 3	9, 10, 11	01		65	ns
Output disable time from high level	t_{PHZ}	$R_L = 110\Omega$, $C_L = 50$ pF, See figure 3	9, 10, 11	01		105	ns
Output disable time from low level	t_{PLZ}	$R_L = 110\Omega$, $C_L = 50$ pF, See figure 3	9, 10, 11	01		105	ns
RECEIVER SECTION							
Differential-input high-threshold voltage	V_{TH}	$V_O = 2.7$ V, $I_O = -0.4$ mA	1, 2, 3	01		0.2	V
Differential-input low-threshold voltage 2/	V_{TL}	$V_O = 0.5$ V, $I_O = 8$ mA	1, 2, 3	01	-0.2		V
Enable-input clamp voltage	V_{IC}	$I_I = -18$ mA	1, 2, 3	01		-1.5	V
High-level output voltage	V_{OH}	$V_{ID} = 200$ mV, $I_{OH} = -400\ \mu A$	1, 2, 3	01	2.7		V
Low-level output voltage	V_{OL}	$V_{ID} = 200$ mV, $I_{OL} = 8$ mA	1, 2, 3	01		0.45	V
Functional tests	FT	See 4.4.1b	7, 8	01			
High-impedance-state output current	I_{OZ}	$V_O = 0.4$ V to 2.4 V	1, 2, 3	01		± 20	μA
Line input current 3/	I_I	Other input = 0 V, $V_I = 12$ V	1, 2, 3	01		1	mA
		Other input = 0 V, $V_I = -7$ V				-0.8	
High-level enable-input current	I_{IH}	$V_{IH} = 2.7$ V	1, 2, 3	01		-100	μA
Low-level enable-input current	I_{IL}	$V_{IL} = 0.4$ V	1, 2, 3	01		-100	μA
Input resistance	r_i		1, 2, 3	01	12		$k\Omega$
Supply current, receiver enabled and driver disabled	I_{CC1}	$V_I = 0$ or V_{CC}, No load	1, 2, 3	01		3.9	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RECEIVER SECTION - continued							
Supply current, receiver and driver disabled	I_{CC2}	V_I = 0 or V_{CC}, No load	1,2,3	01		0.25	mA
Propagation delay time, low-to-high level output	t_{PLH}	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See figure 4	9,10,11	01	11	37	ns
Propagation delay time, high-to-low level output	t_{PHL}	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See figure 4	9,10,11	01	11	55	ns
Pulse skew ($\lvert t_{PLH} - t_{PHL} \rvert$)	$t_{sk(p)}$	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See figure 4	9,10,11	01		22	ns
Output enable time to high level	t_{PZH}	C_L = 15 pF, See figure 4	9,10,11	01		34	ns
Output enable time to low level	t_{PZL}	C_L = 15 pF, See figure 4	9,10,11	01		34	ns
Output disable time from high level	t_{PHZ}	C_L = 15 pF, See figure 4	9,10,11	01		34	ns
Output disable time from low level	t_{PLZ}	C_L = 15 pF, See figure 4	9,10,11	01		34	ns

1/ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively that occur when the input is changed from a high level to a low level.
2/ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this drawing for common-mode output voltage and threshold voltage levels only.
3/ This applies for both power on and power off; refer to EIA standard RS-485 for exact conditions.

Device type	01	
Case outlines	P	2
Terminal number	Terminal symbol	
1	R	NC
2	$\overline{RE}$	R
3	DE	NC
4	D	NC
5	GND	$\overline{RE}$
6	A	NC
7	B	DE
8	V_{CC}	NC
9	---	NC
10	---	D
11	---	NC
12	---	GND
13	---	NC
14	---	NC
15	---	A
16	---	NC
17	---	B
18	---	NC
19	---	NC
20	---	V_{CC}

NC = No connect

FIGURE 1. Terminal connections.

DRIVER

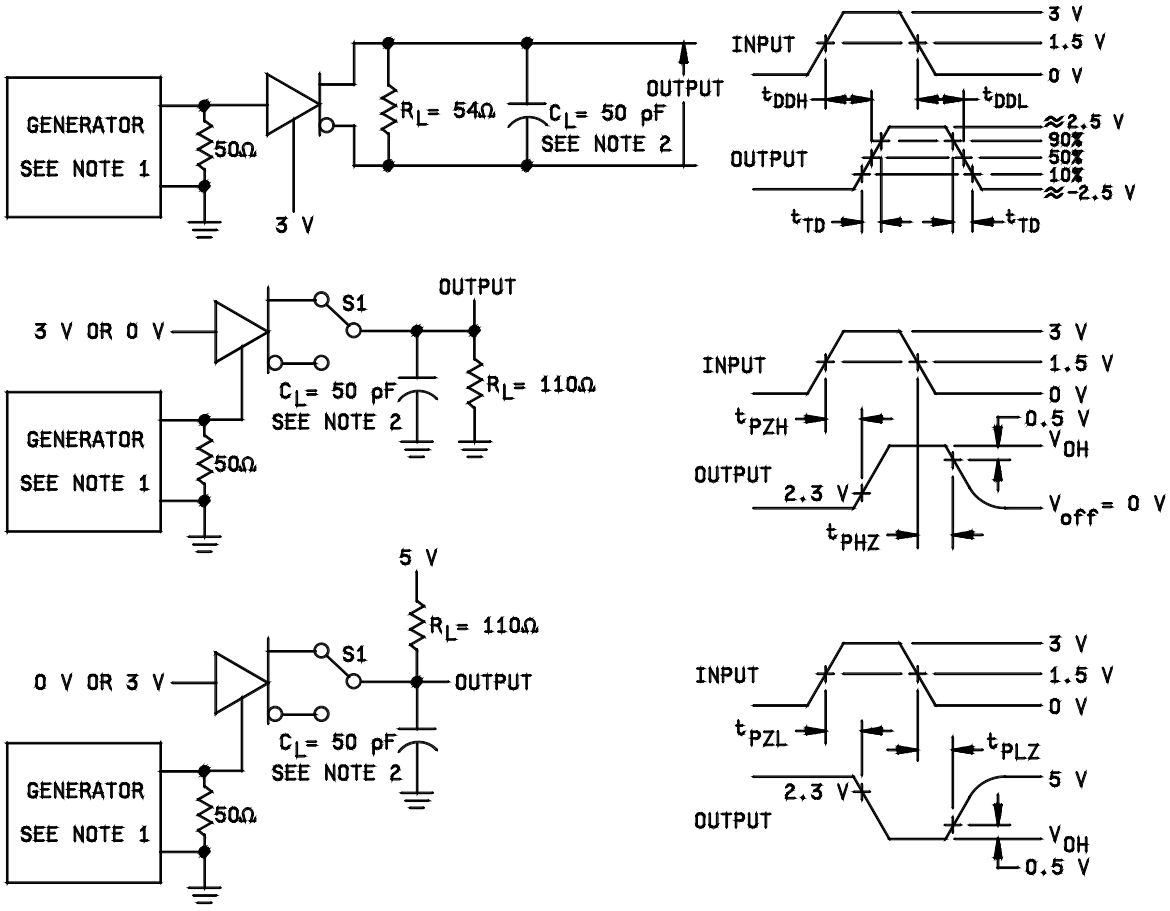
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

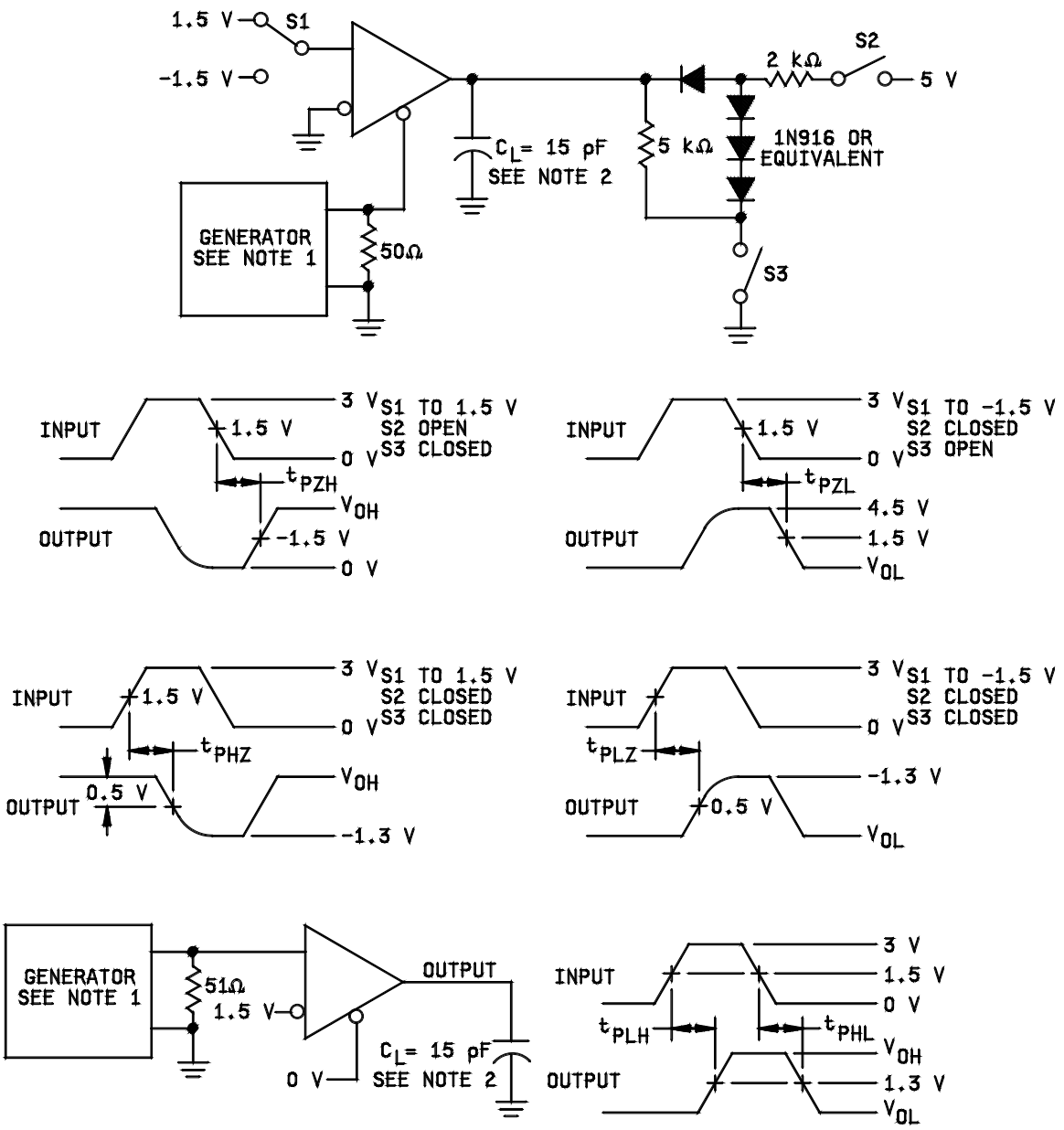
H = High voltage level
L = Low voltage level
? = Indeterminate
X = Irrelevant
Z = High impedance (off)

FIGURE 2. Truth tables.



Notes: 1. Input pulse generator characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50Ω.
2. C_L = includes probe and jig capacitance.

FIGURE 3. Driver test circuits and timing waveforms.



Notes: 1. Input pulse generator characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50Ω.
2. C_L = includes probe and jig capacitance.

FIGURE 4. Receiver test circuits and timing waveforms.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q, and V subgroups 7 and 8 tests shall be sufficient to verify the truth table.

c. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	- - -	- - -

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-01-30

Approved sources of supply for SMD 5962-93183 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9318301QPA	01295	SNJ55LBC176JG
5962-9318301Q2A	01295	SNJ55LBC176FK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243