

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. gap	01-05-01	Raymond Monnin
B	Boilerplate update and part of five year review. tcr	06-05-18	Raymond Monnin
C	Update drawing to the current requirements of MIL-PRF-38535. – glg	14-12-18	Charles Saffle



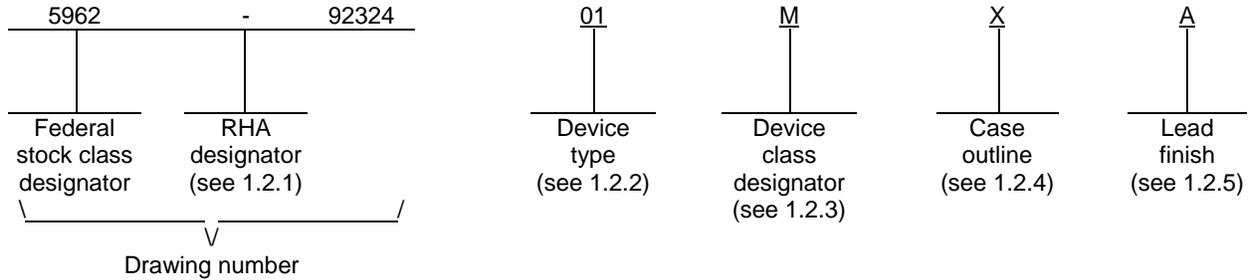
REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C												
SHEET	15	16	17	18	19	20	21	22												
REV STATUS OF SHEETS	REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Jeff Bowling	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p> <p>MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 8K X 8 NON-VOLATILE STATIC RAM MONOLITHIC SILICON</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Jeff Bowling																		
	APPROVED BY Michael A. Frye																		
	DRAWING APPROVAL DATE 94-02-16																		
REVISION LEVEL C	SIZE A	CAGE CODE 67268	5962-92324																
		SHEET 1 OF 22																	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Access Time</u>	<u>Store Cycle</u>	<u>Recall Cycle</u>	<u>Endurance</u>
01	11C68	8K X 8 NVSRAM	55 ns	12 ms	25 μs	10,000 cycles
02	11C68	8K X 8 NVSRAM	45 ns	12 ms	25 μs	10,000 cycles
03	11C68	8K X 8 NVSRAM	35 ns	12 ms	25 μs	10,000 cycles
04	11C68	8K X 8 NVSRAM	55 ns	12 ms	25 μs	100,000 cycles
05	11C68	8K X 8 NVSRAM	45 ns	12 ms	25 μs	100,000 cycles
06	11C68	8K X 8 NVSRAM	35 ns	12 ms	25 μs	100,000 cycles

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CDIP3-T28 or GDIP4-T28	28	Dual -in -line
Y	CQCC3-N28	28	Rectangular leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.6 V dc to 7.0 V dc
Voltage on DQ ₍₀₋₇₎ with outputs in high Z state	-0.5 V to ($V_{CC} + 0.5$ V)
Input voltage operating range (V_{IH} , V_{IL})	-0.6 V dc to 7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Maximum output current	15 mA
Lead temperature (soldering)	300°C
Junction temperature (T_J) 3/	175°C
Thermal resistance, junction to case (θ_{JC}):	See MIL-STD-1835
Data retention	10 Years to nonvolatile array (minimum)
Endurance (as store cycles to non-volatile array)	Per 1.2.2

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input voltage, low range (V_{IL})	V_{SS} -0.5 V dc to 0.8 V dc, all inputs
Input voltage, high range (V_{IH})	2.2 V dc to $V_{CC}+0.5$ V dc, all inputs

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may affect reliability. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied.
- 2/ All voltages are referenced to V_{SS} (ground).
- 3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of this document are available on line at <http://www.jedec.org> or from JEDEC - Solid State Technology Association, 3103 North 10th Street, Suite 247, Arlington, VA 22201;)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

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3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

3.11 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.12 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process changes which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V V _{SS} = 0 V, I _{OUT} = 0 mA unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current (any input)	I _{IL}	V _{CC} = 5.5 V V _{IN} = V _{SS} to V _{CC}	1, 2, 3	All		±1	μA
High impedance output leakage current	I _{OL}	V _{CC} = 5.5 V V _{IN} = V _{SS} to V _{CC}	1, 2, 3	All		±5	μA
Input logic "1" voltage	V _{IH}	All Inputs	1, 2, 3	All	2.2	V _{CC} +.5	V
Input logic "0" voltage	V _{IL}	All Inputs	1, 2, 3	All	V _{SS} -.5	0.8	V
Output logic "1" voltage	V _{OH}	I _{OH} = -4 mA	1, 2, 3	All	2.4		V
Output logic "0" voltage	V _{OL}	I _{OL} = 8 mA	1, 2, 3	All		0.4	V
V _{CC} current <u>1/</u>	I _{CC1}	Addresses cycling at t _{AVAV}	1, 2, 3	01, 04 02, 05 03, 06		70 75 80	mA
V _{CC} current <u>2/</u> during store cycle	I _{CC2}	$\overline{CE} \geq (V_{CC} - 0.2V)$; all other inputs V _{IN} ≤ 0.2 V or ≥ (V _{CC} - 0.2 V)	1, 2, 3	All		50	mA
V _{CC} current (standby, cycling TTL input levels) <u>3/</u>	I _{CC3}	$\overline{CE} \geq V_{IH}$; all others cycling	1, 2, 3	01, 04 02, 05 03, 06		20 23 27	mA
V _{CC} DC current (standby, stable CMOS input levels) <u>2/</u>	I _{CC4}	$\overline{CE} \geq (V_{CC} - 0.2 V)$; all others V _{IN} ≤ 0.2 V or ≥ (V _{CC} - 0.2V)	1, 2, 3	All		2	mA
Input capacitance <u>4/</u>	C _{IN}	V _{IN} = 0 V T _A = 25°C, f = 1.0 MHz See 4.4.1e	4	All		5	pF
Output capacitance <u>4/</u>	C _{OUT}	V _{OUT} = 0 V T _A = 25°C, f = 1.0 MHz See 4.4.1e	4	All		7	pF
Functional test		See 4.4.1c	7, 8A, 8B	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V V _{SS} = 0 V, I _{OUT} = 0 mA unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ CYCLES 1 & 2							
Chip enable access time	t _{ELQV}	See figures 3 and 4	9, 10, 11	01, 04		55	ns
				02, 05		45	
				03, 06		35	
Read cycle time <u>5/</u>	t _{AVAV}		9, 10, 11	01, 04	55		ns
				02, 05	45		
				03, 06	35		
Address access time <u>6/</u>	t _{AVQV}		9, 10, 11	01, 04		55	ns
				02, 05		45	
				03, 06		35	
Output enable to data valid	t _{OLQV}		9, 10, 11	01, 02, 04, 05		25	ns
				03, 06		20	
Output hold after address change	t _{AXQX}		9, 10, 11	All	5		ns
Chip enable to output active	t _{ELQX}		9, 10, 11	All	5		ns
Chip disable to output <u>7/</u> inactive	t _{EHQZ}		9, 10, 11	01, 02, 04, 05		25	ns
		03, 06			20		
Output enable to output active	t _{OLQX}	9, 10, 11	All	0		ns	
Output disable to output <u>7/</u> inactive	t _{OHQZ}	9, 10, 11	01, 02, 04, 05		25	ns	
			03, 06		20		
Chip enable to power <u>4/</u> active	t _{ELPU}	9, 10, 11	All	0		ns	
Chip disable to power <u>3/</u> , <u>4/</u> standby	t _{EHPD}	9, 10, 11	All		25	ns	
Write recovery time	t _{WHQV}	9, 10, 11	01, 04		65	ns	
			02, 05		55		
			03, 06		45		
WRITE CYCLES 1 & 2							
Write cycle time	t _{AVAV}	See figures 3 and 4	9, 10, 11	01, 04	55		ns
				02, 03, 05, 06		45	
Write pulse width	t _{WLWH} t _{WLEH}		9, 10, 11	01, 04	45		ns
				02, 03, 05, 06		35	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V V _{SS} = 0 V, I _{OUT} = 0 mA unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable to end of write	t _{ELWH} t _{ELEH}	See figures 3 and 4	9, 10, 11	01, 04	45		ns
				02, 03, 05, 06	35		
Data set-up to end of write	t _{DVWH} t _{DVEH}		9, 10, 11	All	30		ns
Data hold after end of write	t _{WHDX} t _{EHDX}		9, 10, 11	All	0		ns
Address set-up to end of write	t _{AVWH} t _{AVEH}		9, 10, 11	01, 04	45		ns
				02, 03, 05, 06	35		
Address set-up to start of write	t _{AVWL} t _{AVEL}		9, 10, 11	All	0		ns
Address hold after end of write	t _{WHAX} t _{EHAX}		9, 10, 11	All	0		ns
Write enable to output disable <u>7/</u> , <u>8/</u>	t _{WLQZ}		9, 10, 11	All		35	ns
Output active after end of write	t _{WHQX}	9, 10, 11	All	5		ns	
STORE/RECALL CYCLE							
Store/recall initiation cycle time	t _{AVAV}	See figures 3 and 4	9, 10, 11	01, 04	55		ms
				02, 05	45		
				03, 06	35		
Chip enable to output <u>9/</u> inactive	t _{ELQZ}		9, 10, 11	01, 04		85	ns
				02, 03, 05, 06		75	
Store cycle time <u>10/</u>	t _{STORE}		9, 10, 11	All		12	ms
Recall cycle time <u>11/</u>	t _{RECALL}	9, 10, 11	All		25	μs	
Address set-up to chip <u>12/</u> enable	t _{AVEL}	9, 10, 11	All	0		ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V V _{SS} = 0 V, I _{OUT} = 0 mA unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable pulse <u>12/</u> , <u>13/</u> width	t _{ELEH}	See figures 3 and 4	9, 10, 11	01, 04		45	ns
				02, 05		35	
				03, 06		25	
Chip disable to address <u>12/</u> change	t _{EHAX}		9, 10, 11	All	0		ns

- 1/ I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
- 2/ Bringing $\overline{CE} > V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See Figure 3.
- 3/ I_{CC2} is the current required for the duration of the store cycle (t_{STORE}) once a store has begun.
- 4/ These parameters are tested as part of initial device characterization, and after any design or process change that might affect that parameter. These parameters are not tested as part of lot by lot screening, but are guaranteed to the limits specified in Table I.
- 5/ For Read Cycles 1 and 2, \overline{WE} is high for the entire cycle.
- 6/ The device is continuously selected with \overline{CE} low and \overline{OE} low.
- 7/ Measured ±200 mV from steady state output voltage.
- 8/ If \overline{WE} is low when \overline{CE} goes low, the outputs remain in the high impedance state.
- 9/ Once the software STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.
- 10/ Note that STORE cycles, but not RECALL cycles, are aborted by V_{CC} < 3.8 V (STORE inhibit).
- 11/ A RECALL cycle is initiated automatically at power up when V_{CC} exceeds 3.8 V. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5 V.
- 12/ Noise on the \overline{CE} pin may trigger multiple read cycles from the same address and abort the address sequence.
- 13/ If the \overline{CE} pulse width is less than t_{ELQV}, but greater than or equal to t_{ELEH}, then the data may not be valid at the end of the low pulse. However, the STORE or RECALL will still be initiated.

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Device types	All
Case outlines	X, Y
Terminal number	Terminal symbol
1	NC
2	A ₁₂
3	A ₇
4	A ₆
5	A ₅
6	A ₄
7	A ₃
8	A ₂
9	A ₁
10	A ₀
11	DQ ₀
12	DQ ₁
13	DQ ₂
14	V _{SS}
15	DQ ₃
16	DQ ₄
17	DQ ₅
18	DQ ₆
19	DQ ₇
20	\overline{CE}
21	A ₁₀
22	\overline{OE}
23	A ₁₁
24	A ₉
25	A ₈
26	NC
27	\overline{WE}
28	V _{CC}

FIGURE 1. Terminal connections.

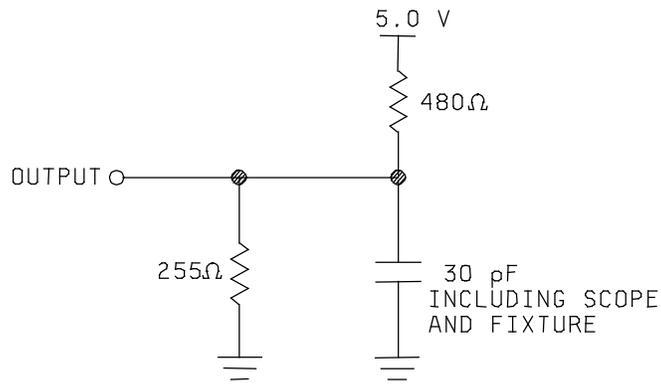
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\overline{CE}	\overline{WE}	A ₁₂ - A ₀ (HEX)	MODE	I/O	POWER
H	X	X	Not Selected	Output high Z	Standby
L	H	X	Read SRAM	Output data <u>2/</u>	Active
L	L	X	Write SRAM	Input data	Active
L	H	0000 <u>1/</u>	Read SRAM	Output data <u>2/</u>	Active
		1555 <u>1/</u>	Read SRAM	Output data <u>2/</u>	
		0AAA <u>1/</u>	Read SRAM	Output data <u>2/</u>	
		1FFF <u>1/</u>	Read SRAM	Output data <u>2/</u>	
		1010 <u>1/</u>	Read SRAM	Output data <u>2/</u>	
		0F0F <u>1/</u>	Nonvolatile store	Output high Z	I _{CC2}
L	H	0000 <u>1/</u>	Read SRAM	Output data <u>2/</u>	Active
		1555 <u>1/</u>	Read SRAM	Output data <u>2/</u>	
		0AAA <u>1/</u>	Read SRAM	Output data <u>2/</u>	
		1FFF <u>1/</u>	Read SRAM	Output data <u>2/</u>	
		1010 <u>1/</u>	Read SRAM	Output data <u>2/</u>	
		0F0E <u>1/</u>	Nonvolatile recall	Output high Z <u>2/</u>	

- 1/ The six consecutive addresses must be in the order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle, or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle. \overline{WE} must be high during all six consecutive cycles. See figure 4.
- 2/ I/O state assumes that \overline{OE} is $\leq V_{IL}$. Initiation and operation of nonvolatile cycles do not depend on the state of \overline{OE} .

FIGURE 2. Truth table.

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AC TEST CONDITIONS ^{1/}

TEST CONDITION	VALUES
Input pulse levels	Gnd to 3 V
Input rise & fall time	≤ 5 ns
Input timing reference levels	1.5V dc
Output reference levels	1.5V dc

^{1/} All voltages are referenced to V_{SS} (ground).

FIGURE 3. Output load circuits.

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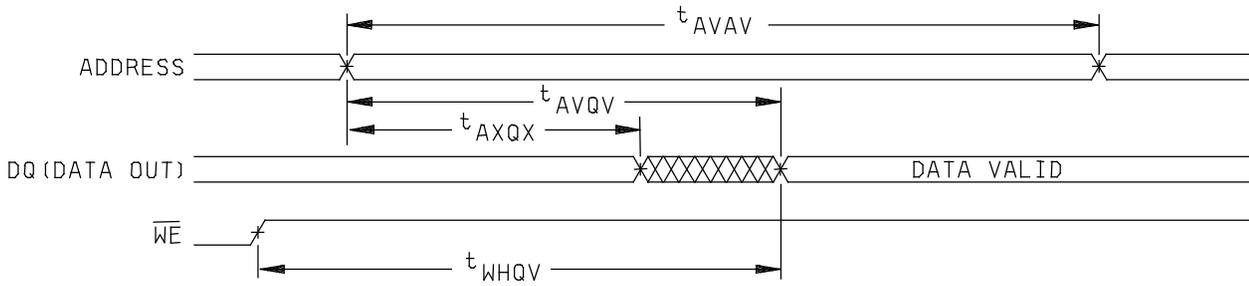
SIZE
A

REVISION LEVEL
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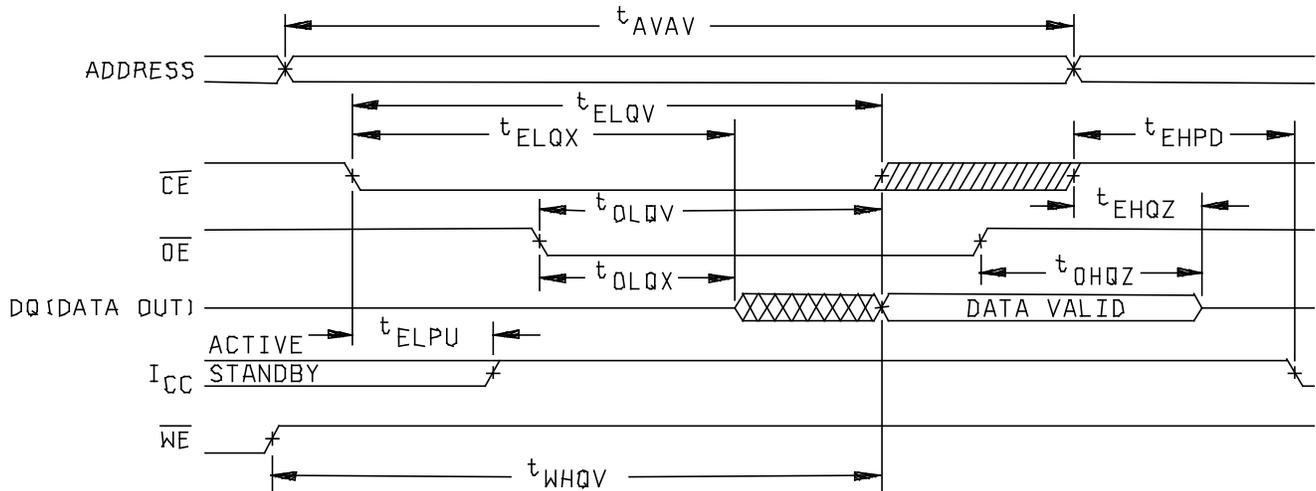
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Read cycle 1 (see notes 1 and 2)



Read cycle 2 (see notes 1 and 2)



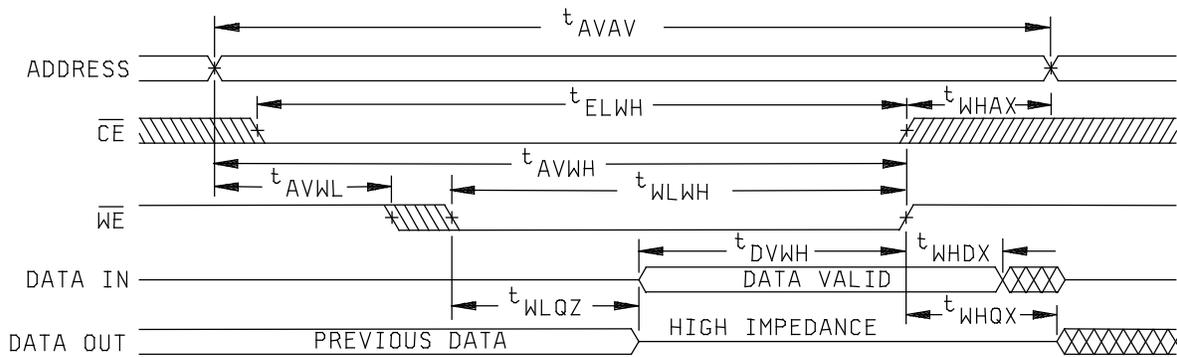
Notes:

1. The device is continuously selected with \overline{CE} low and \overline{OE} low.
2. For READ CYCLE 1 and 2, \overline{WE} must be high for entire cycle.

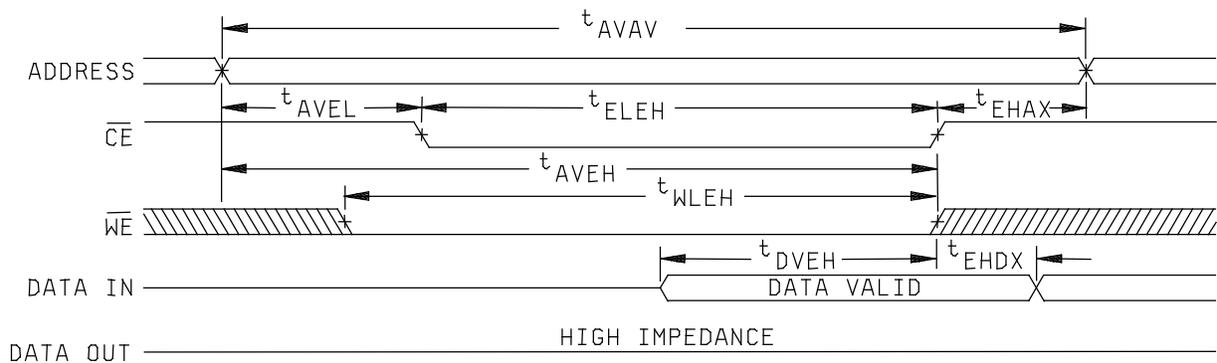
FIGURE 4. Timing waveforms.

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Write cycle 1: \overline{WE} controlled (see note)



Write cycle 2: \overline{CE} controlled (see note)



Note: \overline{CE} or \overline{WE} must be $\geq V_{IH}$ during address transitions.

FIGURE 4. Timing waveforms - continued.

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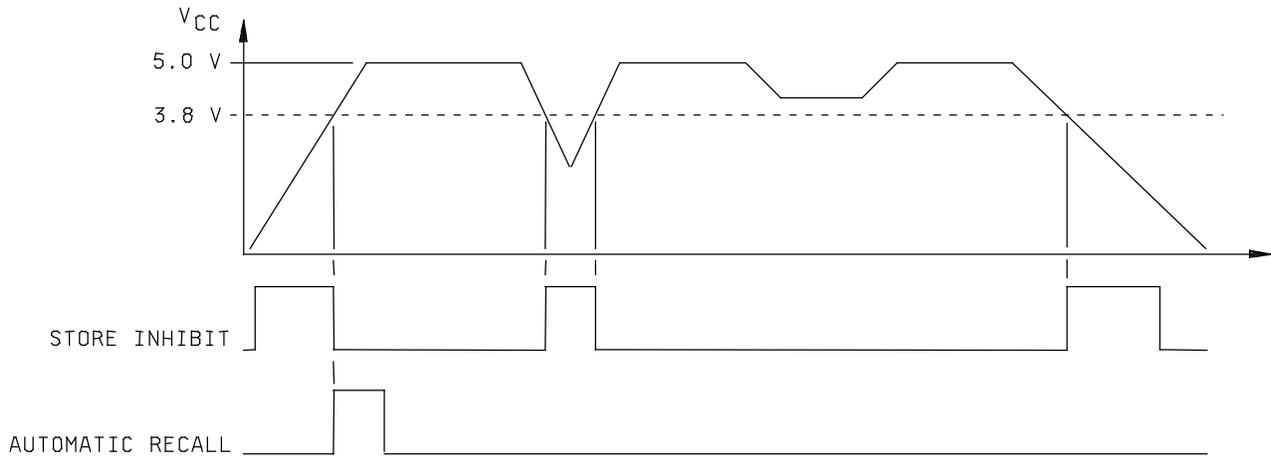
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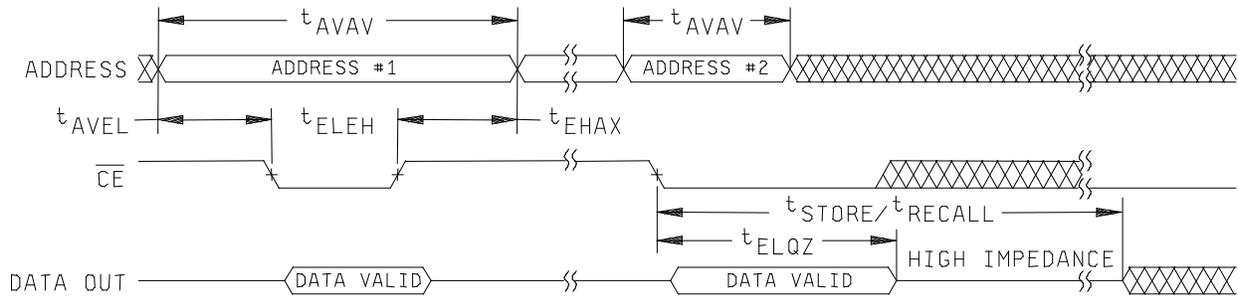
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Store inhibit and automatic power-up recall



Store/recall cycle (see note 3)



Notes:

1. For read cycles 1 and 2, \overline{WE} is high for the entire cycle.
2. The device is continuously selected with \overline{CE} and \overline{OE} low.
3. \overline{WE} must be high when \overline{CE} is low during the address sequence in order to initiate a nonvolatile cycle. \overline{OE} may be either high or low throughout. Addresses A_1 through A_6 are found in the mode selection table. Address A_6 determines whether the device performs a STORE or RECALL.

FIGURE 4. Timing waveforms - continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

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- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

TABLE IIA. Electrical test requirements. 1/, 2/, 3/, 4/, 5/, 6/, 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

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TABLE IIB. Delta limits at +25°C.

Parameter ^{1/}	All Device types
I _{CC4} standby	±10% value in table I
I _{IL} , I _{OL}	±10% value in table I

^{1/} The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. T_A = +125°C, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

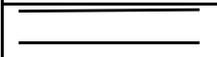
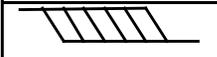
6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331 and as follows:

C _{IN}	Input terminal capacitance.
C _{OUT}	Output terminal capacitance.
GND	Ground zero voltage potential.
I _{CC}	Supply current.
I _{IH}	Input high current.
I _{IL}	Input low current.
T _C	Case temperature.
T _A	Ambient temperature
V _{CC}	Ground zero voltage potential.
O/V	Latch-up over-voltage

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535 and MIL-HDBK-103. The vendors listed in QML-38535 and MIL-HDBK-103 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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APPENDIX A

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

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SRAM APPENDIX A - Continued.

APPENDIX A

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.

A.3.3.1 XY March - Continued.

- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-12-18

Approved sources of supply for SMD 5962-92324 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9232401MXA	<u>3/</u>	STK11C68-C55M
5962-9232401MYA	<u>3/</u>	STK11C68-L55M
5962-9232402MXA	<u>3/</u>	STK11C68-C45M
5962-9232402MYA	<u>3/</u>	STK11C68-L45M
5962-9232403MXA	<u>3/</u>	STK11C68-C35M
5962-9232403MYA	<u>3/</u>	STK11C68-L35M
5962-9232404MXA	65786	STK11C68-5K55M
5962-9232404MXC	65786	STK11C68-5C55M
5962-9232404MYA	<u>3/</u>	STK11C68-5L55M
5962-9232405MXA	<u>3/</u>	STK11C68-5K45M
5962-9232405MXC	<u>3/</u>	STK11C68-5C45M
5962-9232405MYA	<u>3/</u>	STK11C68-5L45M
5962-9232406MXA	<u>3/</u>	STK11C68-5K35M
5962-9232406MXC	<u>3/</u>	STK11C68-5C35M
5962-9232406MYA	<u>3/</u>	STK11C68-5L35M

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE
number

65786

Vendor name
and address

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.