

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add ground bounce criteria and test limits. Changes for device type 01. Editorial changes throughout. - JAK	94-08-19	Monica L. Poelking
B	Add vendor CAGE 27014. Make change to the limits in table I for $I_{OZH}$ , $I_{OZL}$ , $I_{OFF}$ , $I_{CEX}$ , $I_{IH}$ , $I_{IL}$ , $\Delta I_{CC}$ , $V_{OLP}$ , $V_{OHP}$ , $t_{PLH1}$ , $t_{PZH1}$ , $t_{PZL1}$ , $t_{PHZ1}$ , $t_{PLZ1}$ , $t_{PZH2}$ , $t_{PZL2}$ , $t_{PHZ2}$ , $t_{PLZ2}$ , $t_{h1}$ , and $t_{h2}$ for device type 01. Update boilerplate. - JAK	95-08-22	Thomas M. Hess
C	Changes in accordance with NOR 5962-R256-97. - JAK	97-03-31	Monica L. Poelking
D	Update boilerplate to current MIL-PRF-38535 requirements. - MAA	08-10-07	Thomas M. Hess
E	Update output low and high voltage test conditions ( $V_{OL}$ and $V_{OH}$ ) $V_{IH}$ and $V_{IL}$ limits to table I. Update source of supply information. Update boilerplate paragraph to current MIL-PRF-38535 requirements. - JWC	14-10-27	Thomas M. Hess
F	Update devices supplier CAGE 0C7V7 information to bulletin page. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - TTM	21-04-22	Muhammad A. Akbar
G	Add vendor CAGE 3V146 for supplying devices. - TTM	22-10-19	Muhammad A. Akbar



THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

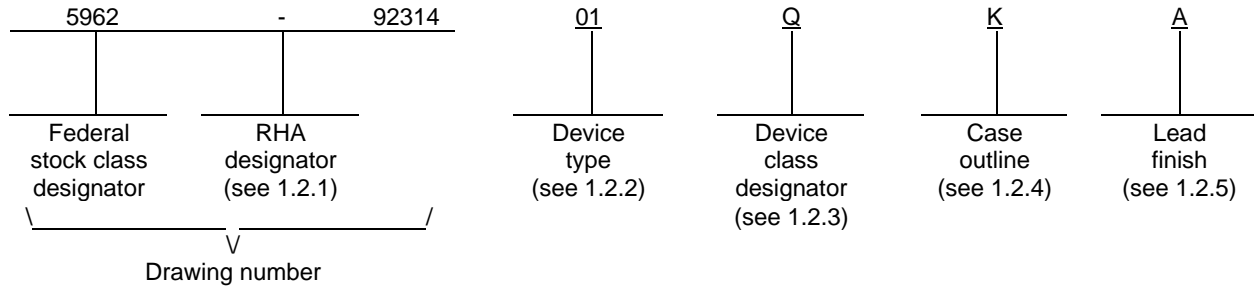
REV																						
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REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

PMIC N/A		PREPARED BY Joseph A. Kerby		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 <a href="https://www.dla.mil/LandandMaritime">https://www.dla.mil/LandandMaritime</a>	
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A		CHECKED BY Thomas J. Ricciuti		MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, OCTAL LATCHED TRANSCEIVER WITH DUAL ENABLE, THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON	
		APPROVED BY Monica L. Poelking			
		DRAWING APPROVAL DATE 93-01-15			
		REVISION LEVEL G		SIZE A	CAGE CODE <b>67268</b>
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ABT543	Octal latched transceiver with dual enable, three-state outputs, TTL compatible inputs
02	54ABT543A	Octal latched transceiver with dual enable, three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V dc to +7.0 V dc
DC input voltage range ( $V_{IN}$ ) (except I/O ports) .....	-0.5 V dc to +7.0 V dc 4/
DC input voltage range ( $V_{IN}$ ) (I/O ports) .....	-0.5 V dc to +5.5 V dc 4/
DC output voltage range ( $V_{OUT}$ ) .....	-0.5 V dc to +5.5 V dc 4/
DC input clamp current ( $I_{IK}$ ) ( $V_{IN} < 0.0$ V) .....	-18 mA
DC output clamp current ( $I_{OK}$ ) ( $V_{OUT} < 0.0$ V or $V_{OUT} > V_{CC}$ ) .....	$\pm 50$ mA
DC output current ( $I_{OL}$ ) (per output):	
Device type 01 .....	+96 mA
Device type 02 .....	+128 mA
Maximum power dissipation ( $P_D$ ) .....	500 mW
Storage temperature range ( $T_{STG}$ ) .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	See MIL-STD-1835
Junction temperature ( $T_J$ ) .....	+150°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range ( $V_{CC}$ ) .....	+4.5 V dc to +5.5 V dc
Input voltage range ( $V_{IN}$ ) .....	+0.0 V dc to $V_{CC}$
Output voltage range ( $V_{OUT}$ ) .....	+0.0 V dc to $V_{CC}$
Minimum high level input voltage ( $V_{IH}$ ) .....	+2.0 V
Maximum low level input voltage ( $V_{IL}$ ) .....	+0.8 V
Maximum high level output current ( $I_{OH}$ ) .....	-24 mA
Maximum low level output current ( $I_{OL}$ ) .....	+48 mA
Maximum input rise or fall rate ( $\Delta t/\Delta V$ ) .....	5 ns/V
Case operating temperature range ( $T_C$ ) .....	-55°C to +125°C

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Unless otherwise noted, all voltages are referenced to GND.
- 3/ The limits of the parameters specified herein shall apply over the full specified  $V_{CC}$  range and case temperature range of -55°C to +125°C. Unused inputs must be held high or low.
- 4/ The input and output voltage ratings may be exceeded provided that the input and output current ratings are observed.

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation. or contract

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification For.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block or Logic diagram. The block or logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

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3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 128 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Device type	V <sub>CC</sub>	Group A subgroups	Limits <u>3/</u>		Unit	
						Min	Max		
High level output voltage 3006	V <sub>OH1</sub>	For all inputs affecting output under test, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.8 V I <sub>OH</sub> = -3 mA	All	4.5 V	1, 2, 3	2.5		V	
	V <sub>OH2</sub>	For all inputs affecting output under test, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.8 V I <sub>OH</sub> = -3 mA	All	5.0 V	1, 2, 3	3.0			
	V <sub>OH3</sub>	For all inputs affecting output under test, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.8 V I <sub>OH</sub> = -24 mA	All	4.5 V	1, 2, 3	2.0			
Low level output voltage 3007	V <sub>OL</sub>	For all inputs affecting output under test, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.8 V I <sub>OL</sub> = +48 mA	All	4.5 V	1, 2, 3		0.55	V	
Three - state output leakage current high 3021	I <sub>OZH</sub> <u>4/ 5/ 6/</u>	For control inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V V <sub>OUT</sub> = 2.7 V	All	5.5 V	1, 2, 3		+10.0	μA	
Three - state output leakage current low 3020	I <sub>OZL</sub> <u>4/ 5/ 6/</u>	For control inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V V <sub>OUT</sub> = 0.5 V	All	5.5 V	1, 2, 3		-10.0	μA	
Input current high 3010	I <sub>IH</sub>	For input under test, V <sub>IN</sub> = V <sub>CC</sub> For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND	Control inputs	01	5.5 V	1, 2, 3		+2.0	μA
				02		1, 2, 3		+1.0	
			An, Bn inputs <u>7/</u>	All		1, 2, 3		+100	
Input current low 3009	I <sub>IL</sub>	For input under test, V <sub>IN</sub> = GND For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND	Control inputs	01	5.5 V	1, 2, 3		-2.0	μA
				02		1, 2, 3		-1.0	
			An, Bn inputs <u>7/</u>	All		1, 2, 3		-100	
Negative input clamp voltage 3022	V <sub>IC</sub>	For input under test, I <sub>IN</sub> = -18 mA	All	4.5 V	1, 2, 3		-1.2	V	
Off-state leakage current	I <sub>OFF</sub>	For input or output under test, V <sub>IN</sub> or V <sub>OUT</sub> ≤ 4.5 V All other pins at 0.0 V		01	0.0 V	1, 2, 3		±100	μA
				02		1		±100	
High-state leakage current	I <sub>CEX</sub>	For output under test, V <sub>OUT</sub> = 5.5 V For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND; outputs at high logic state	All	5.5 V	1, 2, 3		+50	μA	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Device type	V <sub>CC</sub>	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Input capacitance 3012	C <sub>IN</sub>	T <sub>C</sub> = +25°C, See 4.4.1c	01	5.0 V	4		14.0	pF
			02				14.0	
Input capacitance 3012	C <sub>I/O</sub>	T <sub>C</sub> = +25°C, See 4.4.1c	01	5.0 V	4		19.5	pF
			02				19.5	
Short circuit output current 3011	I <sub>OS</sub> <u>8/</u>	For all inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND V <sub>OUT</sub> = 2.5 V	01	5.0 V	1, 2, 3	-50	-180	mA
			02			-50	-200	
Quiescent supply current delta, TTL input levels 3005	ΔI <sub>CC</sub> <u>9/</u>	For input under test, V <sub>IN</sub> = 3.4 V For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND;	01	5.5 V	1, 2, 3		2.5	mA
			02		1, 2, 3		1.5	
Quiescent supply current, output high 3005	I <sub>CC</sub> H	For all inputs V <sub>IN</sub> = V <sub>CC</sub> or GND	01	5.5 V	1, 2, 3		250	μA
			02		1		350	
					2, 3		400	
Quiescent supply current, output low 3005	I <sub>CC</sub> L	For all inputs V <sub>IN</sub> = V <sub>CC</sub> or GND	01	5.5 V	1, 2, 3		30	mA
			02		1, 2, 3		34	
Quiescent supply current, output three-state 3005	I <sub>CC</sub> Z <u>4/</u>	For all inputs V <sub>IN</sub> = V <sub>CC</sub> or GND	01	5.5 V	1, 2, 3		250	μA
			02		1		350	
					2, 3		400	
Low level ground bounce noise	V <sub>OLP</sub> <u>10/</u>	V <sub>IH</sub> = 3.0 V, V <sub>IL</sub> = 0.0 V T <sub>A</sub> = +25°C See 4.4.1d See figure 4	01	5.0 V	4		800	mV
	V <sub>OLV</sub> <u>10/</u>		02				750	
			01		4		-1250	
	02						-1450	
High level V <sub>CC</sub> bounce noise	V <sub>OHP</sub> <u>10/</u>	V <sub>IH</sub> = 3.0 V, V <sub>IL</sub> = 0.0 V T <sub>A</sub> = +25°C See 4.4.1d See figure 4	01	5.0 V	4		1100	mV
	V <sub>OHV</sub> <u>10/</u>		02				1500	
			01		4		-560	
	02						-450	
Functional test 3014	<u>11/</u>	V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.8 V Verify output V <sub>OUT</sub> See 4.4.1b	All	4.5 V	7, 8	L	H	
			All	5.5 V	7, 8	L	H	

See footnotes at end of table.

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**A**

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TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Device type	V <sub>CC</sub>	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Propagation delay time, data to output An to Bn, Bn to An 3003	t <sub>PHL1</sub> <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	All	5.0 V	9	1.6	5.1	ns
			All	4.5 V and 5.5 V	10, 11	1.6	6.2	
Propagation delay time, data to output An to Bn, Bn to An 3003	t <sub>PLH1</sub> <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	1.6	5.1	ns
			02			1.6	4.4	
			01	4.5 V and 5.5 V	10, 11	1.6	6.4	
			02			1.6	5.5	
Propagation delay time, latch enable to output $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn 3003	t <sub>PHL2</sub> <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	All	5.0 V	9	1.6	5.4	ns
			All	4.5 V and 5.5 V	10, 11	1.6	6.4	
Propagation delay time, latch enable to output $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn 3003	t <sub>PLH2</sub> <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	All	5.0 V	9	1.6	5.1	ns
			All	4.5 V and 5.5 V	10, 11	1.6	6.6	
Propagation delay time, output enable, $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn 3003	t <sub>PZH1</sub> <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	1.4	5.1	ns
			02			1.4	4.1	
			01	4.5 V and 5.5 V	10, 11	1.2	6.2	
			02			1.4	5.1	
Propagation delay time, output enable, $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn 3003	t <sub>PZL1</sub> <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	1.8	5.8	ns
			02			2.0	4.9	
			01	4.5 V and 5.5 V	10, 11	1.8	7.2	
			02			2.0	5.8	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T <sub>c</sub> ≤ +125°C +4.5 V ≤ V <sub>cc</sub> ≤ +5.5 V unless otherwise specified	Device type	V <sub>cc</sub>	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Propagation delay time, output disable, $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn 3003	$t_{PHZ1}$ <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	All	5.0 V	9	2.5	5.8	ns
			01	4.5 V	10, 11	2.0	6.7	
			02	and 5.5 V		2.5	6.9	
Propagation delay time, output disable, $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn 3003	$t_{PLZ1}$ <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	1.8	6.1	ns
			02			2.5	6.1	
			01	4.5 V	10, 11	1.8	7.6	
			02	and 5.5 V		2.5	7.6	
Propagation delay time, output enable, $\overline{EBA}$ to An, $\overline{EAB}$ to Bn 3003	$t_{PZH2}$ <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	1.4	5.4	ns
			02			1.4	4.7	
			01	4.5 V	10, 11	1.3	6.4	
			02	and 5.5 V		1.4	5.6	
Propagation delay time, output enable, $\overline{EBA}$ to An, $\overline{EAB}$ to Bn 3003	$t_{PZL2}$ <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	All	5.0 V	9	2.0	5.7	ns
			01	4.5 V	10, 11	1.8	7.4	
			02	and 5.5 V		2.0	6.2	
Propagation delay time, output disable, $\overline{EBA}$ to An, $\overline{EAB}$ to Bn 3003	$t_{PHZ2}$ <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	2.5	6.0	ns
			02			3.2	6.5	
			01	4.5 V	10, 11	2.0	7.2	
			02	and 5.5 V		3.2	7.3	
Propagation delay time, output disable, $\overline{EBA}$ to An, $\overline{EAB}$ to Bn 3003	$t_{PLZ2}$ <u>12/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	1.5	6.2	ns
			02			2.5	6.7	
			01	4.5 V	10, 11	1.5	7.0	
			02	and 5.5 V		2.5	7.8	
Setup time high An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	$t_{S1}$ <u>13/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	3.5		ns
			02			2.5		
			01	4.5 V	10, 11	3.5		
			02	and 5.5 V		2.5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T <sub>c</sub> ≤ +125°C +4.5 V ≤ V <sub>cc</sub> ≤ +5.5 V unless otherwise specified	Device type	V <sub>cc</sub>	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Setup time low An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	$t_{s2}$ <u>13/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	All	5.0 V	9	3.0		ns
			All	4.5 V and 5.5 V	10, 11	3.0		
Setup time high An to $\overline{EAB}$ , Bn to $\overline{EBA}$	$t_{s3}$ <u>13/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	3.0		ns
			02			2.5		
			01	4.5 V and 5.5 V	10, 11	3.3		
			02			2.5		
Setup time low An to $\overline{EAB}$ , Bn to $\overline{EBA}$	$t_{s4}$ <u>13/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	All	5.0 V	9	2.5		ns
			All	4.5 V and 5.5 V	10, 11	2.5		
Hold time high or low An from $\overline{LEAB}$ , Bn from $\overline{LEBA}$	$t_{h1}$ <u>13/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	1.5		ns
			02			1.0		
			01	4.5 V and 5.5 V	10, 11	2.0		
			02			1.0		
Hold time high or low An from $\overline{EAB}$ , Bn from $\overline{EBA}$	$t_{h2}$ <u>13/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	01	5.0 V	9	1.5		ns
			02			1.0		
			01	4.5 V and 5.5 V	10, 11	2.0		
			02			1.0		
Latch enable Pulse width low $\overline{LEAB}$ , $\overline{LEBA}$	$t_w$ <u>13/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500 Ω See figure 5	All	5.0 V	9	3.5		ns
			All	4.5 V and 5.5 V	10, 11	3.5		

- 1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI<sub>cc</sub>), utilize the general test procedure of 883 under the conditions listed herein.
- 2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I<sub>cc</sub> and ΔI<sub>cc</sub> tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

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TABLE I. Electrical performance characteristics - Continued.

- 3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I at  $4.5\text{ V} \leq V_{CC} \leq +5.5\text{ V}$
- 4/ Three-state output conditions are required.
- 5/ This test shall be guaranteed, if not tested, to the limits in table I herein, when performed with control inputs that affect the state of the output under test at  $V_{IN} = V_{IH}$  or  $V_{IL}$ ,  $V_{IH} = 2.0\text{ V}$ ,  $V_{IL} = 0.8\text{ V}$
- 6/ For I/O ports, the limit includes  $I_{IH}$  or  $I_{IL}$  leakage current from the input circuitry.
- 7/ For I/O ports, the limit includes  $I_{OZH}$  or  $I_{OZL}$  leakage current from the output circuitry.
- 8/ Not more than one output should be shorted at a time. The duration of short circuit test should not exceed one second.
- 9/ This test may be performed either one input at a time (preferred method) or with all inputs pins simultaneously at  $V_{IN} = V_{CC} - 2.1\text{ V}$  (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 2.5 mA or 1.5 mA as applicable; and the preferred method and limits are guaranteed.
- 10/ This test is for qualification only. Ground and  $V_{CC}$  bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with  $500\Omega$  of load resistance and a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from  $V_{CC}$  to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and  $V_{CC}$  bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a  $50\Omega$  input impedance.  
  
 The device inputs shall be conditioned such that all outputs are at a high nominal  $V_{OH}$  level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at  $V_{OH}$  as all other outputs possible are switched from  $V_{OH}$  to  $V_{OL}$ .  $V_{OHV}$  and  $V_{OHP}$  are then measured from the nominal  $V_{OH}$  level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from  $V_{OL}$  to  $V_{OH}$ .  
  
 The device inputs shall be conditioned such that all outputs are at a low nominal  $V_{OL}$  level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at  $V_{OL}$  as all other outputs possible are switched from  $V_{OL}$  to  $V_{OH}$ .  $V_{OLP}$  and  $V_{OLV}$  are then measured from the nominal  $V_{OL}$  level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from  $V_{OH}$  to  $V_{OL}$ .
- 11/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883,  $V_{IL} = 0.4\text{ V}$  and  $V_{IH} = 2.4\text{ V}$ . For outputs,  $L \leq 0.8\text{ V}$ ,  $H \geq 2.0\text{ V}$ .
- 12/ For propagation delay tests, all paths must be tested.
- 13/ This parameter is guaranteed, if not tested, to the limit specified in table I, herein.

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Device type	01 and 02	
Case outlines	K and L	3
Terminal number	Terminal symbol	
1	$\overline{LEBA}$	NC
2	$\overline{OEBA}$	$\overline{LEBA}$
3	A0	$\overline{OEBA}$
4	A1	A0
5	A2	A1
6	A3	A2
7	A4	A3
8	A5	NC
9	A6	A4
10	A7	A5
11	$\overline{EAB}$	A6
12	GND	A7
13	$\overline{OEAB}$	$\overline{EAB}$
14	$\overline{LEAB}$	GND
15	B7	NC
16	B6	$\overline{OEAB}$
17	B5	$\overline{LEAB}$
18	B4	B7
19	B3	B6
20	B2	B5
21	B1	B4
22	B0	NC
23	$\overline{EBA}$	B3
24	V <sub>CC</sub>	B2
25		B1
26		B0
27		$\overline{EBA}$
28		V <sub>CC</sub>

NC = No internal connection

Terminal description	
Terminal symbol	Description
$\overline{LEAB} / \overline{LEBA}$	A to B / B to A latch enable control inputs (active low)
$\overline{EAB} / \overline{EBA}$	A to B / B to A enable control inputs (active low)
$\overline{OEAB} / \overline{OEBA}$	A to B / B to A output enable control inputs (active low)
A <sub>n</sub> (n = 0 to 7)	Data inputs/outputs (A port)
B <sub>n</sub> (n = 0 to 7)	Data inputs/outputs (B port)

FIGURE 1. Terminal connections.

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Inputs				Outputs	Internal latch status
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	Data		
H	L	L	H	Z	Transparent
H	L	L	L	Z	Transparent
X	↑	L	h	Z	Latch+hold
X	↑	L	l	Z	Latch+hold
H	L	↑	h	Z	Latch+hold
H	L	↑	l	Z	Latch+hold
H	X	H	X	Z	Hold
X	H	X	X	Z	Hold
L	L	L	H	H	Transparent
L	L	L	L	L	Transparent
L	L	↑	h	H	Latch+hold
L	L	↑	l	L	Latch+hold
L	L	H	X	NC	Hold

H = High voltage level

L = Low voltage level

X = Don't care or Irrelevant

Z = High impedance

NC = No change

h = High voltage level meeting the setup and hold times in table I relative to the low-to high transition of  $\overline{LEXX}$  or  $\overline{EXX}$

l = Low voltage level meeting the setup and hold times in table I relative to the low-to high transition of  $\overline{LEXX}$  or  $\overline{EXX}$

↑ = Low-to high transition of  $\overline{LEXX}$  or  $\overline{EXX}$

XX = AB or BA

FIGURE 2. Truth table

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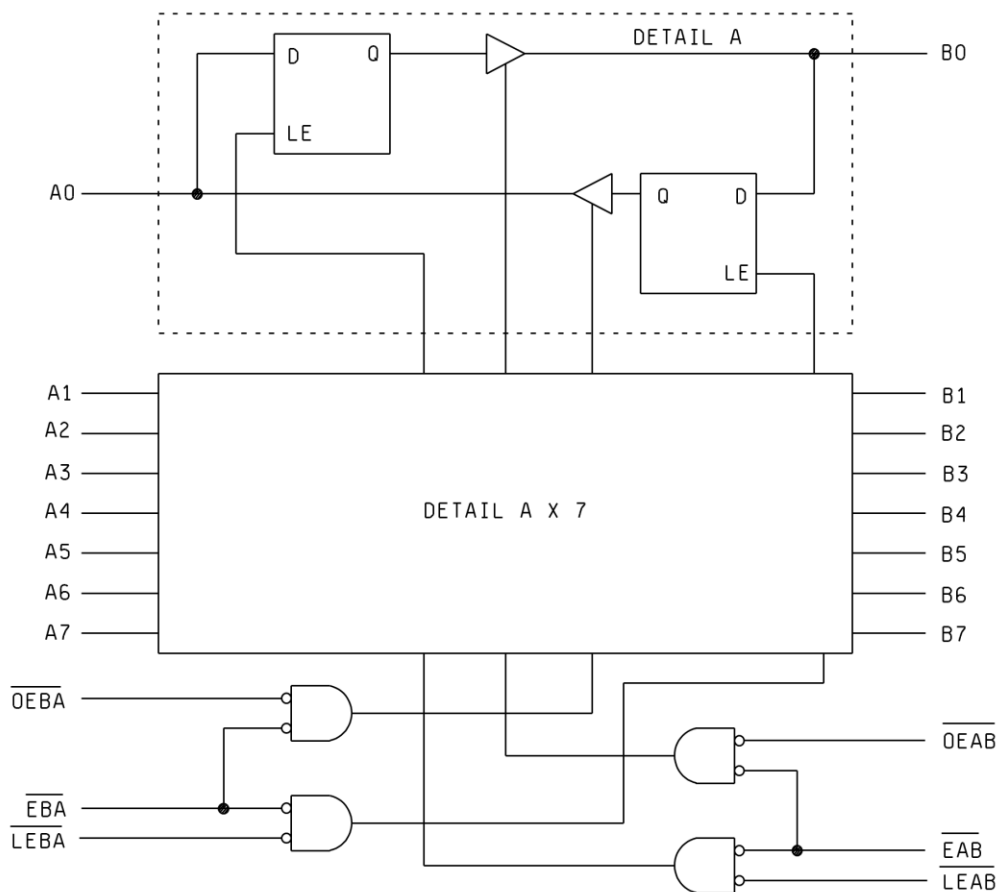
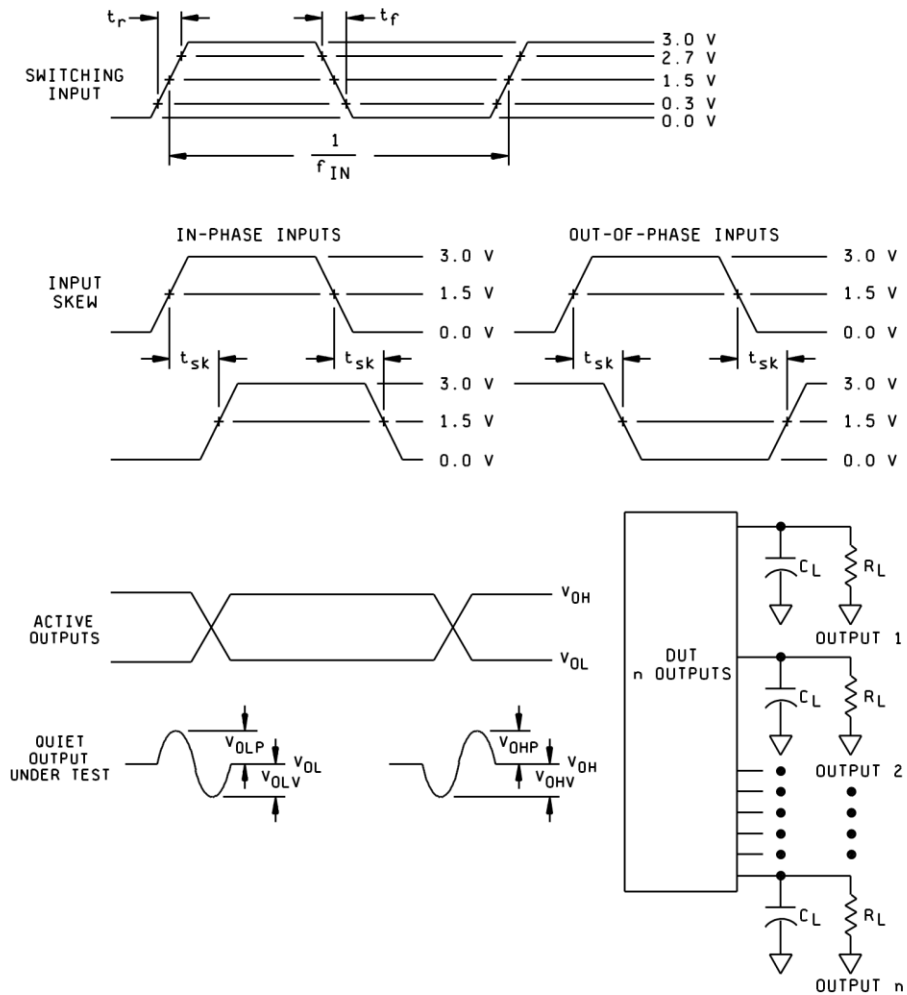


FIGURE 3. Logic diagram

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**NOTES:**

1.  $C_L$  includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2.  $R_L = 450\Omega \pm 1$  percent, chip resistor in series with a  $50\Omega$  termination. For monitored outputs, the  $50\Omega$  termination shall be the  $50\Omega$  characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
  - a.  $V_{IN} = 0.0$  V to 3.0 V; duty cycle = 50 percent;  $f_{IN} \geq 1$  MHz.
  - b.  $t_r, t_f = 3$  ns  $\pm 1.0$  ns. For input signal generators incapable of maintaining these values of  $t_r$  and  $t_f$ , the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the  $\pm 1.0$  ns tolerance and guaranteeing the results at 3.0 ns  $\pm 1.0$  ns; skew between any two switching inputs signals ( $t_{sk}$ ):  $\leq 250$  ps.

FIGURE 4. Ground bounce load circuit and waveforms.

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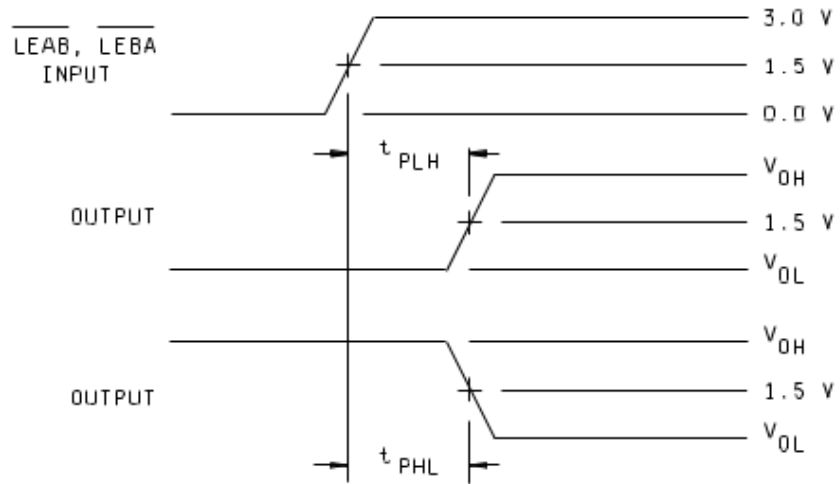
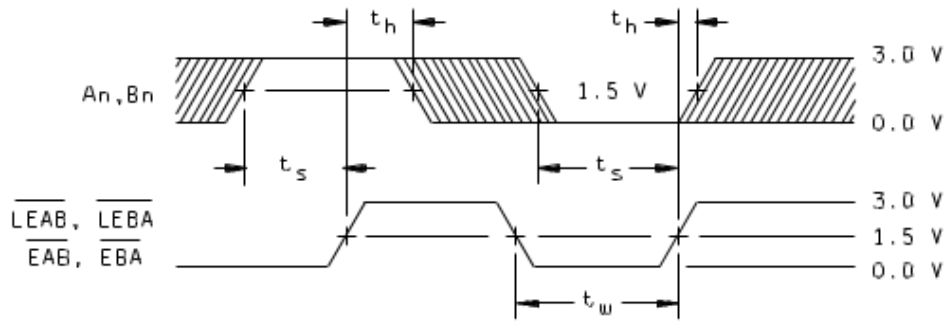


FIGURE 5. Switching waveforms and test circuit.

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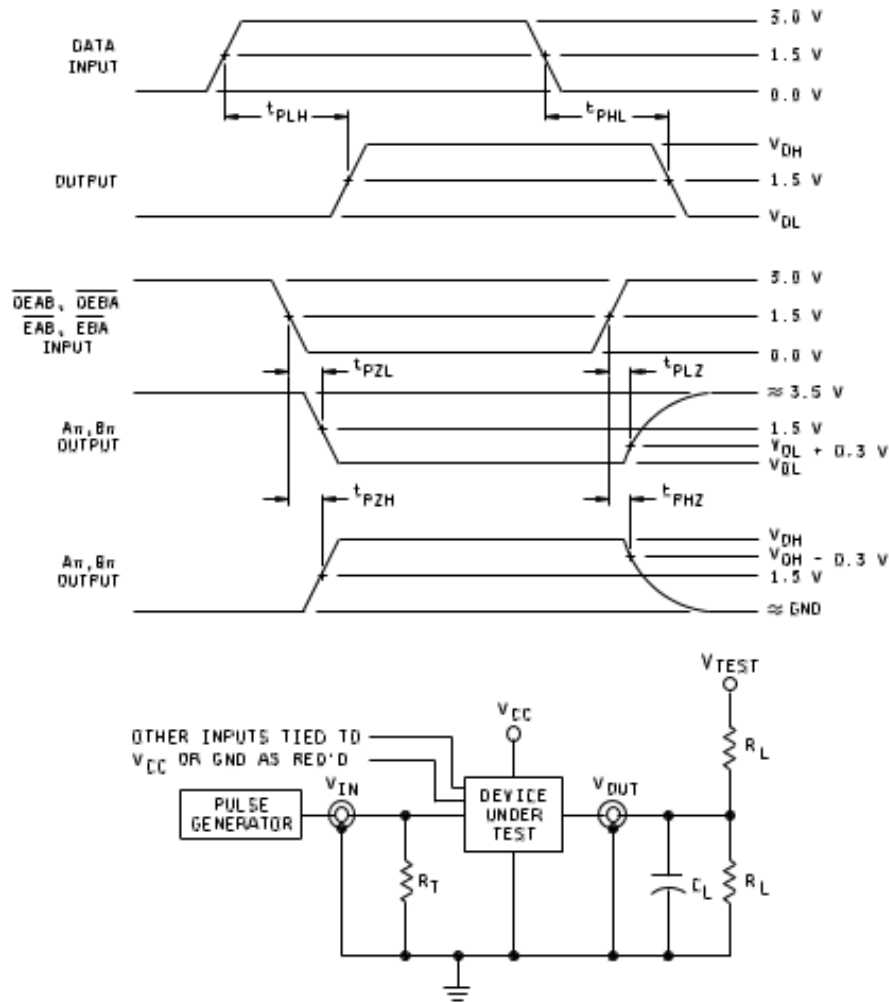
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NOTES:

1. When measuring  $t_{PHZ}$ ,  $t_{PZH}$ ,  $t_{PLH}$ , and  $t_{PHL}$ :  $V_{TEST} = \text{Open}$
2. When measuring  $t_{PLZ}$  and  $t_{PZL}$ :  $V_{TEST} = 7.0 \text{ V}$
3. The  $t_{PZL}$  and  $t_{PLZ}$  reference waveform is for the output under test with internal conditions such that the output is at  $V_{OL}$  except when disabled by the output enable control. The  $t_{PZH}$  and  $t_{PHZ}$  reference waveform is for the output under test with internal conditions such that the output is at  $V_{OH}$  except when disabled by the output enable control.
4.  $C_L = 50 \text{ pF}$  minimum or equivalent (includes test jig and probe capacitance).
5.  $R_L = 500\Omega$  or equivalent
6.  $R_T = 50\Omega$  or equivalent
7. Input signal from pulse generator:  $V_{IN} = 0.0 \text{ V}$  to  $3.0 \text{ V}$ ;  $\text{PRR} \leq 10 \text{ MHz}$ ;  $t_r \leq 2.5 \text{ ns}$ ;  $t_f \leq 2.5 \text{ ns}$ ;  $t_r$  and  $t_f$  shall be measured from  $0.3 \text{ V}$  to  $2.7 \text{ V}$  and from  $2.7 \text{ V}$  to  $0.3 \text{ V}$ , respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of  $1 \text{ MHz}$
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

- (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
- (2)  $T_A = +125^{\circ}\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c.  $C_{IN}$  and  $C_{I/O}$  shall be measured only for initial qualification and after process or design changes which may affect capacitance.  $C_{IN}$  and  $C_{I/O}$  shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test ( $V_{BIAS}$ ) = 2.5 V or 3.0 V. For  $C_{IN}$  and  $C_{I/O}$ , test all applicable pins on five devices with zero failures.

For  $C_{IN}$  and  $C_{I/O}$ , a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the  $C_{IN}$  and  $C_{I/O}$  tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results for each device tested.

- d. Ground and  $V_{CC}$  bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture.  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DLA Land and Maritime-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DLA Land and Maritime-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DLA Land and Maritime-VA data from testing on both fixtures, that shall include all measured peak values for each device tested and detailed oscilloscope plots for each  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For  $V_{OHP}$ ,  $V_{OHV}$ ,  $V_{OLP}$ , and  $V_{OLV}$ , a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the  $V_{OHP}$ ,  $V_{OHV}$ ,  $V_{OLP}$ , and  $V_{OLV}$  tests. The device manufacturer may then test one device function from a functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturers shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and test results, along with the oscilloscope plots, for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance With MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1

2/ PDA applies to subgroups 1 and 7

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table II herein.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218 - 3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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Approved sources of supply for SMD 5962-92314 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9231401MKA	3V146	54ABT543/MKA
	<u>3</u> /	54ABT543/BKA
5962-9231401MLA	3V146	54ABT543/MLA
	<u>3</u> /	54ABT543/BLA
5962-9231401M3A	3V146	54ABT543/M3A
	<u>3</u> /	54ABT543/B3A
5962-9231401QKA	0C7V7	54ABT543W-QML
	3V146	54ABT543/QKA
5962-9231401QLA	0C7V7	54ABT543J-QML
	3V146	54ABT543/QLA
5962-9231401Q3A	0C7V7	54ABT543E-QML
	3V146	54ABT543/Q3A
5962-9231402QKA	<u>3</u> /	SNJ54ABT543AW
5962-9231402QLA	<u>3</u> /	SNJ54ABT543AJT
5962-9231402Q3A	01295	SNJ54ABT543AFK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

DATE: 22-10-19

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>
0C7V7	Teledyne e2v, Inc. 765 Sycamore Drive Milpitas, CA 95035
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln P.O. Box 660199 Dallas, TX 75243
3V146	Rochester Electronics, LLC 16 Malcolm Drive Newburyport, MA 01950

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.