

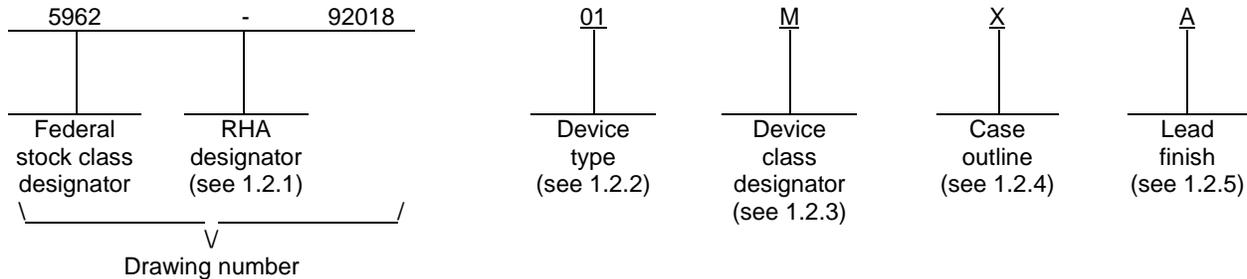
REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. - jak	07-01-22	Thomas M. Hess
B	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	13-08-29	Thomas M. Hess

REV																					
SHEET																					
REV	B	B	B	B	B	B															
SHEET	15	16	17	18	19	20															
REV STATUS	REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
OF SHEETS	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14				
PMIC N/A	PREPARED BY Wanda L. Meadows						DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil														
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas J. Ricciuti																				
	APPROVED BY Monica L. Poelking						MICROCIRCUIT, DIGITAL, ADVANCED CMOS, 16-BIT BUS DRIVERS WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON														
	DRAWING APPROVAL DATE 93-02-08																				
	REVISION LEVEL B						SIZE A	CAGE CODE 67268	5962-92018												
						SHEET		1 OF 20													

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ACT16240	16-bit bus driver with inverting three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	48	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 2

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage range (V_{OUT})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC input clamp current (I_{IK}) ($V_{IN} < 0.0$ V, $V_{IN} > V_{CC}$)	± 20 mA
DC output clamp current (I_{OK}) ($V_{OUT} < 0.0$ V, $V_{OUT} > V_{CC}$).....	± 50 mA
DC output current (I_{OUT}) ($V_{OUT} = 0$ to V_{CC}) (per output)	± 50 mA
DC V_{CC} or GND current (I_{CC} , I_{GND}) (per pin)	± 400 mA 3/
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	9.9 °C/W
Junction temperature (T_J).....	+175°C
Case operating temperature range (T_C).....	-55°C to +125°C

1.4 Recommended operating conditions. 2/ 4/ 5/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT}).....	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL}).....	0.8 V
Minimum high level input voltage (V_{IH}).....	2.0 V
Case operating temperature range (T_C).....	-55°C to +125°C
Maximum input rise and fall rate (t_r , t_f): (10% to 90% of V_{IN} , 90% to 10% of V_{IN})	10 ns/V
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL}).....	24 mA

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
- 2/ Unless otherwise noted, all voltages are referenced to GND.
- 3/ For packages with multiple V_{CC} and GND pins, this value represents the maximum total current flowing into or out of all V_{CC} or GND pins.
- 4/ Unless otherwise specified the limits for the parameters listed herein shall apply over the full specified V_{CC} and T_C recommended operating range.
- 5/ Unused or floating inputs should be held high or low.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 3

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.
 JESD78 - IC Latch-Up Test.

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S Arlington, VA 22201-2107).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 5.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 4

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 5

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Device type and device class <u>3/</u>	V _{CC}	Group A subgroups	Limits <u>4/</u>		Unit
						Min	Max	
High level output voltage 3006	V _{OH1}	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -50 μA	All All	4.5 V	1, 2, 3	4.4		V
	V _{OH2}	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -50 μA	All All	5.5 V	1, 2, 3	5.4		
	V _{OH3}	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -24 mA	All All	4.5 V	1	3.94		
					2, 3	3.70		
	V _{OH4}	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -24 mA	All All	5.5 V	1	4.94		
2, 3					4.70			
V _{OH5} <u>5/</u>	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -50 mA	All All	5.5 V	1, 2, 3	3.85			
Low level output voltage 3007	V _{OL1}	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OL} = +50 μA	4.5 V	All All	1, 2, 3		0.1	V
	V _{OL2}	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OL} = +50 μA	5.5 V	All All	1, 2, 3		0.1	
	V _{OL3}	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OL} = +24 mA	4.5 V	All Q, V	1, 3		0.36	
					2		0.50	
				All M	1		0.36	
					2, 3		0.50	
V _{OL4}	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OL} = +24 mA	5.5 V	All Q, V	1, 3		0.36		
				2		0.50		
			All M	1		0.36		
				2, 3		0.50		
V _{OL5} <u>5/</u>	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OL} = +50 mA	5.5 V	All All	1, 2, 3		1.65		

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 6

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	V _{CC}	Device type and device class <u>3/</u>	Group A subgroups	Limits <u>4/</u>		Unit
						Min	Max	
Three-state output leakage current high 3021	I _{OZH}	$\overline{mG} = V_{IH} = 2.0 \text{ V}$ or $V_{IL} = 0.8 \text{ V}$ For all other inputs $V_{IN} = V_{CC}$ or GND $V_{OUT} = 5.5 \text{ V}$	5.5 V	All Q, V	1		0.5	μA
					2, 3		10.0	
				All M	1		0.5	
					2, 3		10.0	
Three-state output leakage current low 3020	I _{OZL}	$\overline{mG} = V_{IH} = 2.0 \text{ V}$ or $V_{IL} = 0.8 \text{ V}$ For all other inputs $V_{IN} = V_{CC}$ or GND $V_{OUT} = \text{GND}$	5.5 V	All Q, V	1		-0.5	μA
					2, 3		-10.0	
				All M	1		-0.5	
					2, 3		-10.0	
Positive input clamp voltage 3022	V _{IC+}	For input under test, I _{IN} = 1 mA	GND	All Q, V	1	0.4	1.5	V
Negative input clamp voltage 3022	V _{IC-}	For input under test, I _{IN} = -1 mA	Open	All Q, V	1	-0.4	-1.5	V
Input current high 3010	I _{IH}	For input under test $V_{IN} = V_{CC}$ For all other inputs $V_{IN} = V_{CC}$ or GND	5.5 V	All Q, V	1		0.1	μA
					2, 3		1.0	
				All M	1		0.1	μA
					2, 3		1.0	
Input current low 3009	I _{IL}	For input under test $V_{IN} = \text{GND}$ For all other inputs $V_{IN} = V_{CC}$ or GND	5.5 V	All Q, V	1		-0.1	μA
					2, 3		-1.0	
				All M	1		-0.1	μA
					2, 3		-1.0	
Input capacitance 3012	C _{IN}	See 4.4.1c T _C = +25°C	GND	All All	4		9.0	pF
Output capacitance 3012	C _{OUT}	See 4.4.1c T _C = +25°C	GND	All All	4		24.0	pF
Power dissipation capacitance	C _{PD} <u>6/</u>	See 4.4.1c T _C = +25°C C _L = 50 pF f = 1 MHz Any one mA input switching	5.0 V	All All	4		48	pF
							11	
Quiescent supply current delta, TTL input levels 3005	ΔI _{CC} <u>7/</u>	For input under test $V_{IN} = V_{CC} - 2.1 \text{ V}$ For all other inputs $V_{IN} = V_{CC}$ or GND	5.5 V	All Q, V	3		0.9	mA
					1, 2		1.0	
				All M	1		0.9	
					2, 3		1.0	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 7

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	V _{CC}	Device type and device class <u>3/</u>	Group A subgroups	Limits <u>4/</u>		Unit
						Min	Max	
Quiescent supply current, output high 3005	I _{CCH}	$\overline{mG} = \text{GND}$ For all other inputs V _{IN} = V _{CC} or GND	5.5 V	All Q, V	1		2.0	μA
					2, 3		40	
				All M	1		8.0	
					2, 3		160	
Quiescent supply current, output low 3005	I _{CCL}	$\overline{mG} = \text{GND}$ For all other inputs V _{IN} = V _{CC} or GND	5.5 V	All Q, V	1		2.0	μA
					2, 3		40	
				All M	1		8.0	
					2, 3		160	
Quiescent supply current, outputs three-state 3005	I _{CCZ}	$\overline{mG} = V_{CC}$ For all other inputs V _{IN} = V _{CC} or GND	5.5 V	All Q, V	1		2.0	μA
					2, 3		40	
				All M	1		8.0	
					2, 3		160	
Low level ground bounce noise	V _{GBL} <u>8/ 9/</u>	V _{LD} = 2.5 V I _{OL} = +24 mA See figure 5	4.5 V	All Q, V	4		2000	mV
High level V _{CC} bounce noise	V _{GBH} <u>8/ 9/</u>	V _{LD} = 2.5 V I _{OL} = -24 mA See figure 5	4.5 V	All Q, V	4		2000	mV
Latch-up input/output over-voltage	I _{CC} (O/V1) <u>10/</u>	t _w ≥ 100 μs, t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms, 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V V _{over} = 10.5 V	5.5 V	All Q, V	2		200	mA
Latch-up input/output positive over-current	I _{CC} (O/I1+) <u>10/</u>	t _w ≥ 100 μs, t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms, 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V I _{trigger} = +120 mA	5.5 V	All Q, V	2		200	mA
Latch-up input/output negative over-current	I _{CC} (O/I1-) <u>10/</u>	t _w ≥ 100 μs, t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms, 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V I _{trigger} = -120 mA	5.5 V	All Q, V	2		200	mA
Latch-up supply over-voltage	I _{CC} (O/V2) <u>10/</u>	t _w ≥ 100 μs, t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms, 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V V _{over} = 9.0 V	5.5 V	All Q, V	2		100	mA
Truth table test, output voltage 3014	<u>11/</u>	V _{IL} = 0.40 V V _{IH} = 2.40 V Verify output V _{OUT} See 4.4.1e	4.5 V	All All	7, 8	L	H	
			5.5 V	All M	7, 8	L	H	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 8

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	V _{CC}	Device type and device class <u>3/</u>	Group A subgroups	Limits <u>4/</u>		Unit
						Min	Max	
Propagation delay time, <u>mAn</u> to <u>mYn</u> 3003	<u>t_{PLH}</u> <u>12/ 13/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 6	4.5 V	9	All All	2.3	8.5	ns
						10, 11	2.0	
	9			All All	4.1	9.6		
					10, 11	3.0	11.5	
	5.5 V		9	All All	2.3	8.5		
					10, 11	2.0	9.5	
			9	All All	4.1	9.6		
					10, 11	3.0	11.5	
Propagation delay time, <u>output enable</u> , <u>mG</u> to <u>mYn</u> 3003	<u>t_{PZH}</u> <u>12/ 13/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 6	4.5 V	9	All All	2.6	9.0	ns
						10, 11	2.0	
	9			All All	3.3	10.2		
					10, 11	2.5	12.2	
	5.5 V		9	All All	2.6	9.0		
					10, 11	2.0	10.1	
			9	All All	3.3	10.2		
					10, 11	2.5	12.2	
Propagation delay time, <u>output disable</u> , <u>mG</u> to <u>mYn</u> 3003	<u>t_{PHZ}</u> <u>12/ 13/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 6	4.5 V	9	All All	5.9	11.5	ns
						10, 11	4.5	
	9			All All	5.1	11.0		
					10, 11	4.0	12.0	
	5.5 V		9	All All	5.9	11.5		
					10, 11	4.5	12.7	
			9	All All	5.1	11.0		
					10, 11	4.0	12.0	

See footnotes on next sheet.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 9

TABLE I. Electrical performance characteristics – Continued.

- 1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.
- 2/ Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:
 - a. V_{IC} (pos) tests, the GND terminal can be open. $T_C = +25^\circ\text{C}$.
 - b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. $T_C = +25^\circ\text{C}$.
 - c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.
- 3/ The word "All" in the device type and device class column means the test is for all device types and classes.
- 4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. Devices shall meet or exceed the limits specified in table I if tested at $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$.
- 5/ Transmission driving tests are performed at $V_{CC} = 5.5\text{ V}$ dc with a 10 ms duration maximum. Not more than one output should be tested at one time. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN} = 2.0\text{ V}$ or 0.8 V . For device class M, values for subgroup 1 shall be guaranteed, if not tested, to the limits specified in table I.
- 6/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$, and the dynamic current consumption, $I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + (n \times d \times \Delta I_{CC})$. For both P_D and I_S , n is the number of device inputs at TTL levels, f is the frequency of the input signal, and d is the duty cycle of the input signal.
- 7/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} . This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1\text{ V}$ (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.0 mA or 0.9 mA, as applicable, and the preferred method and limits are guaranteed.
- 8/ This test is for qualification only. Ground bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} maximum = $\pm 24\text{ mA}$, for example) and 50 pF of load capacitance (see figure 5). The loads must be located as closely as possible to the device output. Inputs are conditioned with a 1 MHz pulse ($t_r, t_f = 3.5 \pm 1.5\text{ ns}$) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using an F.E.T. oscilloscope probe with at least 1 M Ω impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (see figure 5). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.
- 9/ When used in asynchronous TTL compatible systems, ground bounce (V_{GBL} and V_{GBH}) = 2,000 mV can be a possible problem.
- 10/ See EIA/JEDEC Standard No. 78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and V_{over} are to be accurate within ± 5 percent.
- 11/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. $H \geq 2.5\text{ V}$, $L < 2.5\text{ V}$; high inputs = 2.4 V and low inputs = 0.4 V. The input voltage levels have the allowable tolerances in accordance with MIL-STD-883 already incorporated. For functional testing the outputs shall have, at a minimum, the same loading conditions as the ac tests (see figure 6).
- 12/ Device classes Q and V are tested at $V_{CC} = 4.5\text{ V}$ at $T_C = +125^\circ\text{C}$ for sample testing and at $V_{CC} 4.5\text{ V}$ at $T_C = +25^\circ\text{C}$ for screening. Other V_{CC} levels and temperatures are guaranteed, if not tested; see 4.4.1d.
- 13/ For propagation delay tests, all paths must be tested.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 10

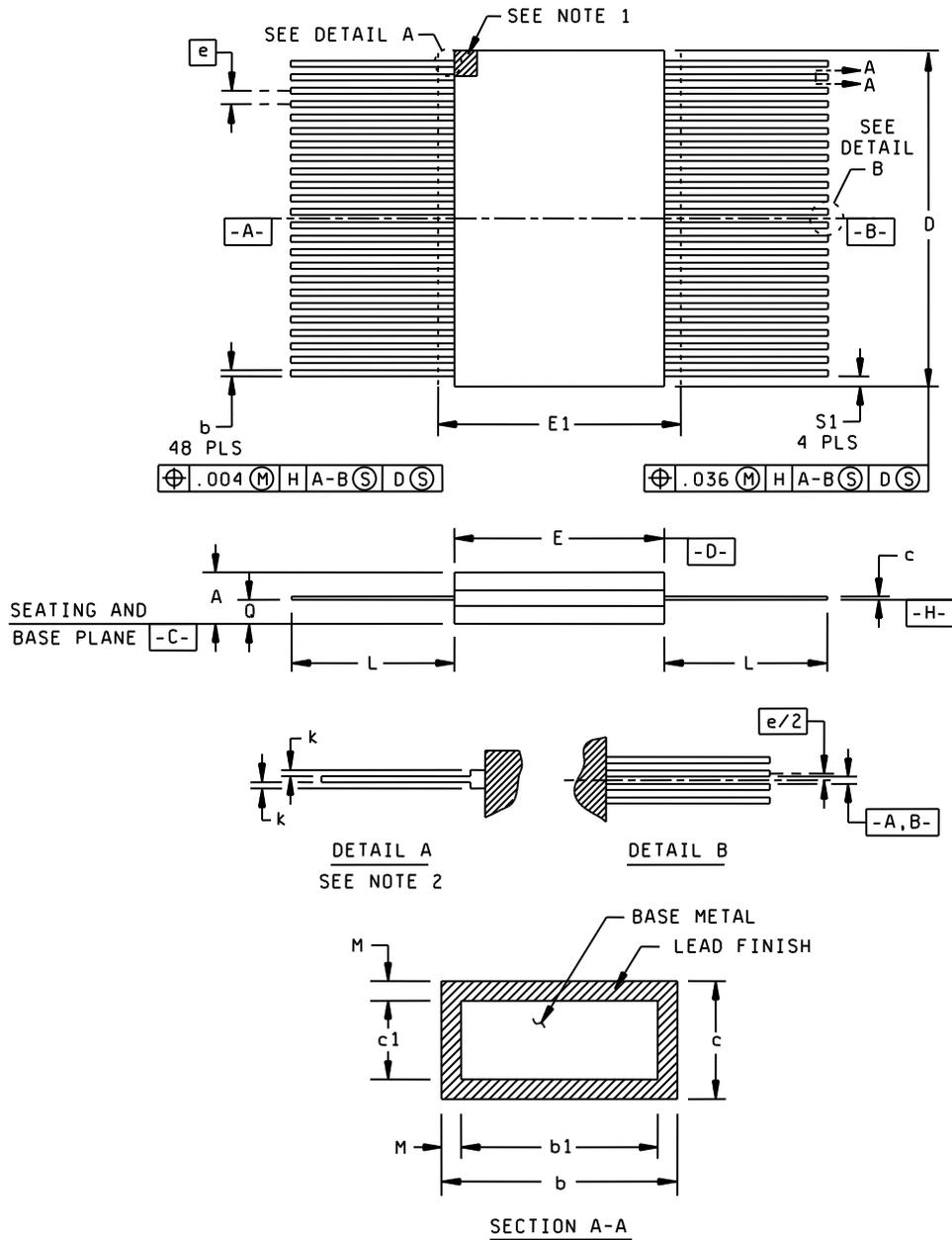


FIGURE 1. Case outline.

**STANDARD
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DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-92018

REVISION LEVEL
B

SHEET
11

Case outline X					
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.075	.120	1.91	3.01	
b	.008	.014	0.20	0.36	
b1	.008	.012	0.20	0.30	3
c	.004	.009	0.10	0.23	
c1	.004	.006	0.10	0.15	3
D	---	.640	---	16.26	4
E	.370	.390	9.40	9.91	
E1	---	.400	---	10.16	4
e	.025 BCS		0.635 BSC		
k	.003	.007	0.08	0.18	2, 5
L	.250	.370	6.35	9.40	
Q	.026	.045	0.66	1.14	6
S1	.005	---	0.13	---	7
M	---	.0015	---	0.04	3
N	48		48		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dimension k) may be used to identify pin one. This tab may be located on either side of terminal one as shown in detail A.
2. Optional, see note 1. If a pin one identification mark in addition to this tab, the minimum limit of dimension k does not apply.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions c and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
6. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by .0015 inch (0.04 mm) maximum when solder dip lead finish is applied.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.

FIGURE 1. Case outline – Continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 12

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{1G}$	25	$\overline{3G}$
2	$\overline{1Y1}$	26	4A4
3	$\overline{1Y2}$	27	4A3
4	GND	28	GND
5	$\overline{1Y3}$	29	4A2
6	$\overline{1Y4}$	30	4A1
7	V _{CC}	31	V _{CC}
8	$\overline{2Y1}$	32	3A4
9	$\overline{2Y2}$	33	3A3
10	GND	34	GND
11	$\overline{2Y3}$	35	3A2
12	$\overline{2Y4}$	36	3A1
13	$\overline{3Y1}$	37	2A4
14	$\overline{3Y2}$	38	2A3
15	GND	39	GND
16	$\overline{3Y3}$	40	2A2
17	$\overline{3Y4}$	41	2A1
18	V _{CC}	42	V _{CC}
19	$\overline{4Y1}$	43	1A4
20	$\overline{4Y2}$	44	1A3
21	GND	45	GND
22	$\overline{4Y3}$	46	1A2
23	$\overline{4Y4}$	47	1A1
24	$\overline{4G}$	48	$\overline{2G}$

Terminal description	
Terminal symbol	Description
mAn (m = 1 to 4, n = 1 to 4)	Data inputs
\overline{mG} (m = 1 to 4)	Output enable control inputs (active low)
\overline{mYn} (m = 1 to 4, n = 1 to 4)	Outputs (inverting)

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 13

inputs		Output
\overline{mG}	mAn	\overline{mYn}
L	H	L
L	L	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance

FIGURE 3. Truth table.

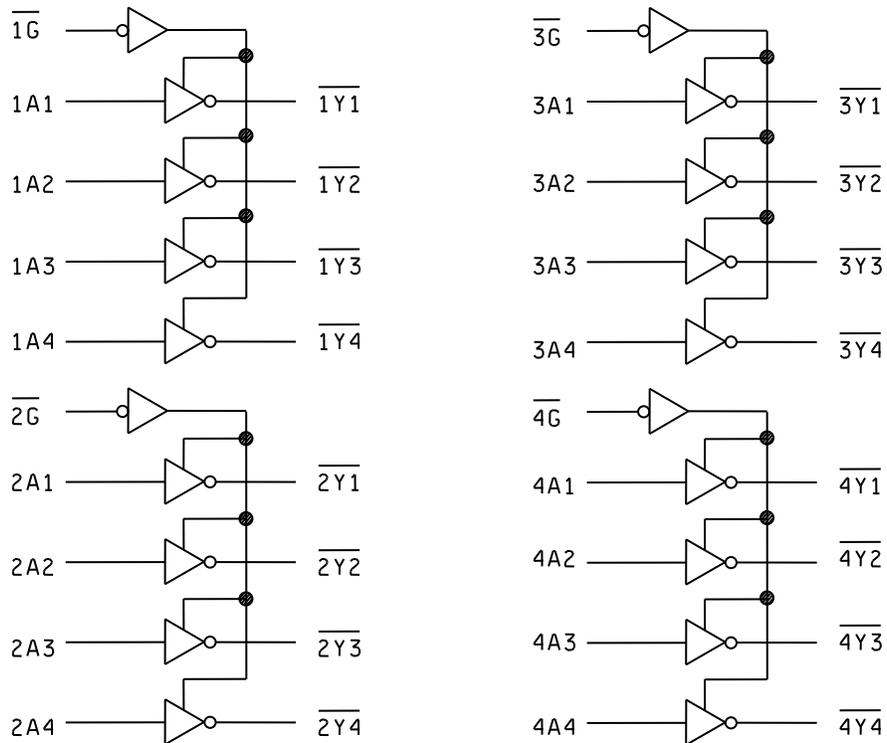
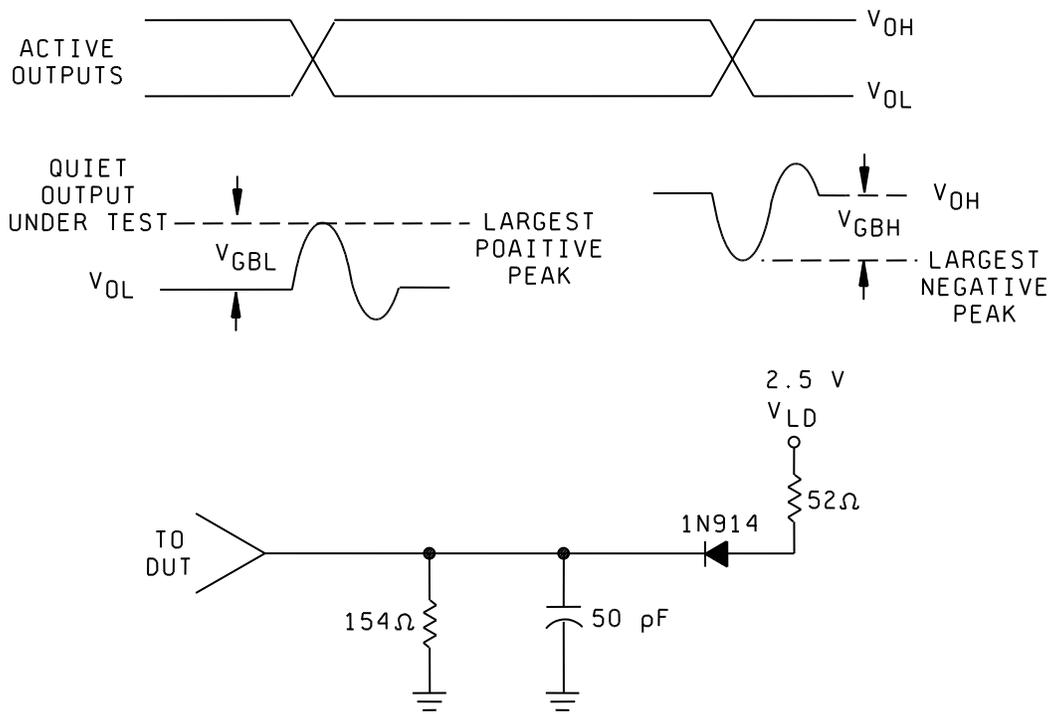


FIGURE 4. Logic diagram.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A	5962-92018
	REVISION LEVEL B	SHEET 14



NOTE: Resistor and capacitor tolerances = $\pm 10\%$.

FIGURE 5. Ground bounce waveforms and test circuit.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 15

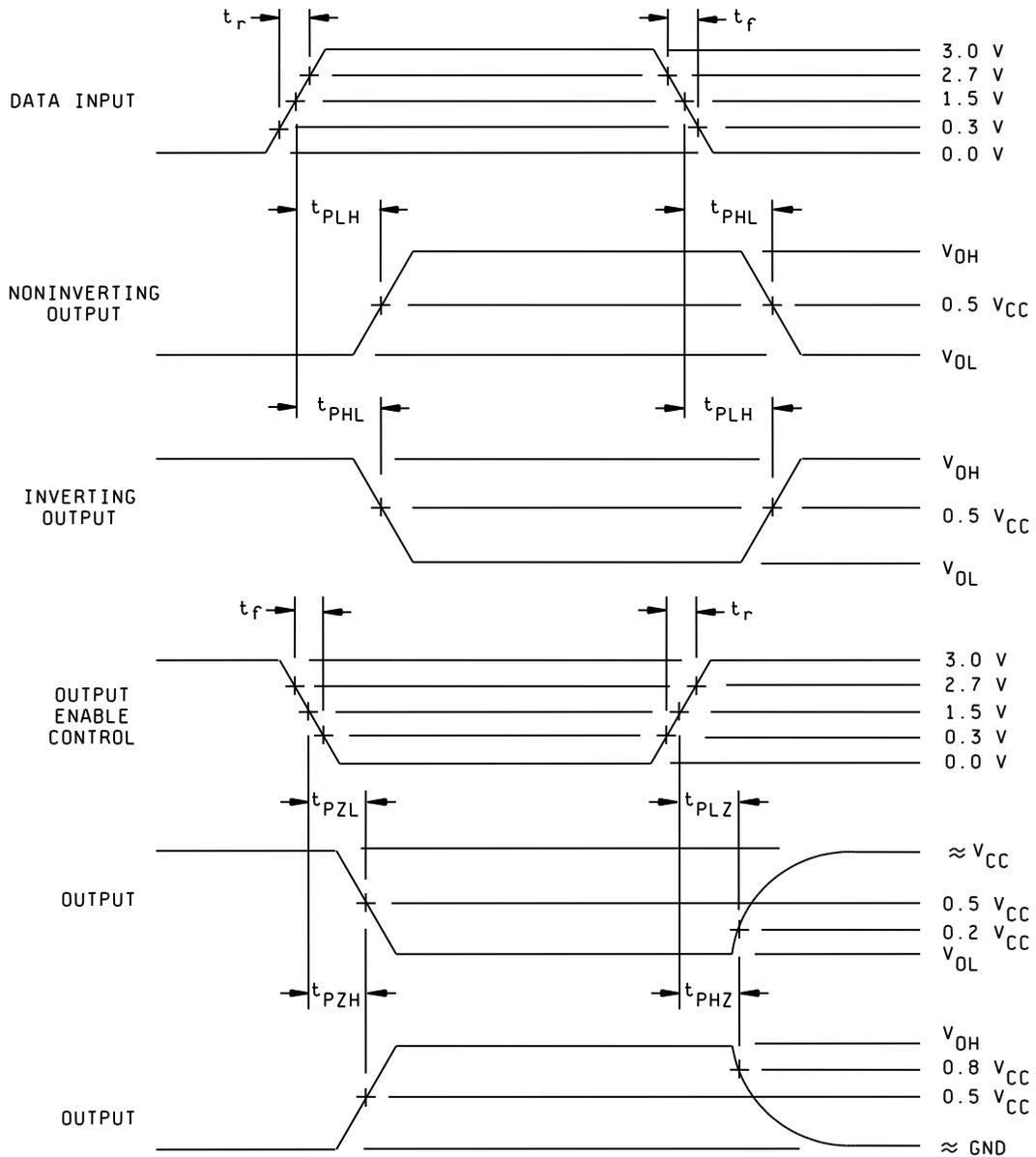
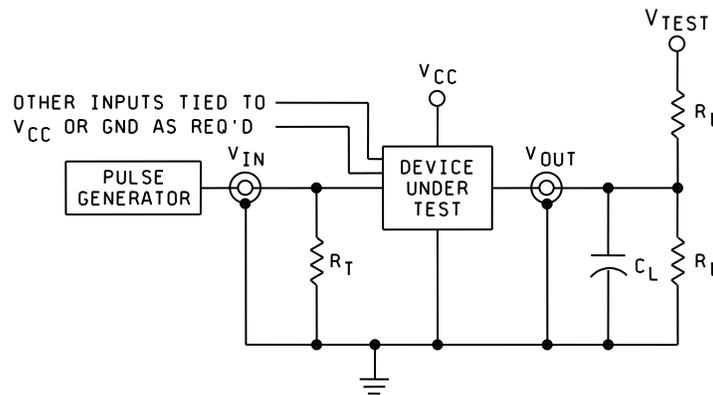


FIGURE 6. Switching waveforms and test circuit.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 16



NOTES:

1. When measuring t_{PHZ} and t_{PZH} : $V_{TEST} = GND$.
2. When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 2 \times V_{CC}$.
3. When measuring t_{PLH} , and t_{PHL} : $V_{TEST} = Open$.
4. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
5. $C_L = 50 \text{ pF}$ minimum or equivalent (includes test jig and probe capacitance).
6. $R_L = 500\Omega$ or equivalent, $R_T = 50\Omega$ or equivalent.
7. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to 3.0 V ; $PRR \leq 10 \text{ MHz}$; $t_r \leq 3.0 \text{ ns}$; $t_f \leq 3.0 \text{ ns}$; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 6. Switching waveforms and test circuit – Continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 17

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Latch-up tests and ground bounce tests are required for device classes Q and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up test, test all applicable pins on five devices with zero failures.
- c. C_{IN} , C_{OUT} , and C_{PD} , shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JESD20 and tale I herein. For C_{IN} , C_{OUT} , and C_{PD} , test all applicable pins on five devices with zero failures.
- d. For device classes Q and V, subgroups 9 and 11 tests shall be measured only for initial qualifications and after process or design changes which may affect dynamic performance.
- e. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 18

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 19

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-92018
		REVISION LEVEL B	SHEET 20

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-08-29

Approved sources of supply for SMD 5962-92018 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9201801MXA	01295	SNJ54ACT16240WD

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments Inc.
Semiconductor Group
8505 Forest Ln.
P.O. Box 660199
Dallas, TX 75243
Point of contact:

U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

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