REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes IAW NOR 5962-R159-94. – tvn	94-05-02	Monica L. Poelking
B	Incorporate NOR, notice of revision into the drawing. Update the boilerplate to the current requirements of MIL-PRF-38535. - phn	08-02-20	Thomas M. Hess
C	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	14-06-25	Thomas M. Hess
D	Delete class M requirement. Update boilerplate to MIL-PRF- 38535 requirements. - DRH	21-03-15	Muhammad A. Akbar

REV																				
SHEET																				
REV	D	D	D	D																
SHEET	15	16	17	18																

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
94-01-04

REVISION LEVEL
D

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL, BIPOLAR CMOS, SCAN TEST DEVICE WITH OCTAL D-TYPE EDGE TRIGGERED FLIP-FLOP, THREE-STATE OUTPUTS, MONOLITHIC SILICON

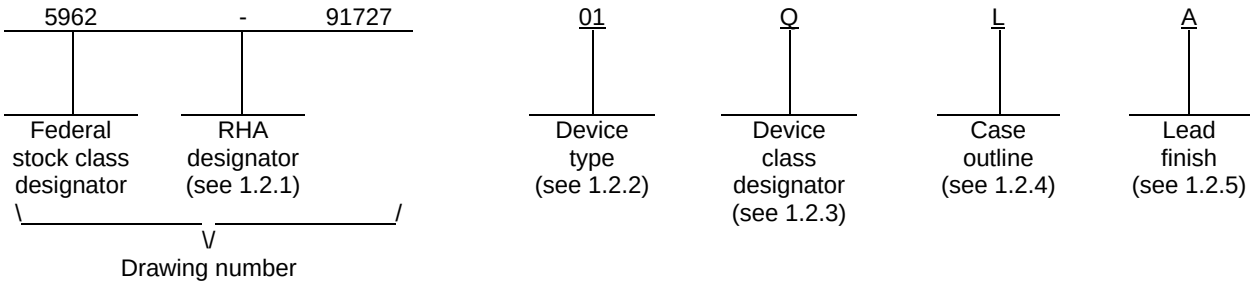
SIZE	CAGE CODE	
A	**67268**	**5962-91727**

SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54BCT8374A	Scan test device with octal D-type edge-triggered flip-flop, three state outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +7.0 V dc
DC input voltage range (except TMS) (V_{IN}) ..... -0.5 V dc to +7.0 V dc 4/
DC input voltage range (TMS) (V_{IN}) ..... -0.5 V dc to +12.0 V dc 4/
DC output voltage range applied to any output in the disabled or power-off state (V_{OUT}) ..... -0.5 V dc to +5.5 V dc
DC output voltage range applied to any output in the high state (V_{OUT}) ..... -0.5 V dc to V_{CC}
DC input clamp current (I_{IK}) ..... -30 mA
DC output current into any output in the low state (I_{OL}) (per output):
TDO ..... +40 mA
Any Q ..... +96 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (Θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C
Maximum power dissipation (P_D) ..... 497 mW 5/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL}) ..... 0.8 V
Minimum high level input voltage (V_{IH}) ..... 2.0 V
Double high level input voltage, TMS (V_{IHH}) ..... +10.0 V dc min to +12.0 V max
Maximum input clamp current (I_{IK}) ..... -18 mA
Maximum high level output current (I_{OH}):
TDO ..... -3 mA
Any Q ..... -12 mA
Maximum low level output current (I_{OL}):
TDO ..... 20 mA
Any Q ..... 48 mA
Minimum setup time (t_s):
Data before CLK↑ ..... 3.0 ns
Any D before TCK↑ ..... 6.0 ns
CLK or before TCK↑ ..... 6.0 ns
TDI before TCK↑ ..... 6.0 ns
TMS before TCK↑ ..... 12.0 ns
Minimum hold time (t_h):
Data after CLK↑ ..... 2.0 ns
Any D after TCK↑ ..... 4.5 ns
CLK or after TCK↑ ..... 4.5 ns
TDI after TCK↑ ..... 4.5 ns
TMS after TCK↑ ..... 0.0 ns
Minimum pulse width (t_w):
CLK high or low ..... 5.0 ns
TCK high or low ..... 25.0 ns
TMS double high ..... 50.0 ns 6/
Minimum delay time, power-up to TCK↑ (t_d) ..... 100.0 ns 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ The input negative voltage rating may be exceeded provided that the input clamp current rating is observed.
5/ Power dissipation values are derived using the formula $P_D = V_{CC}I_{CC} + nV_{OL}I_{OL}$, where V_{CC} and I_{OL} are as specified in 1.4 above, I_{CC} and V_{OL} are as specified in table I herein, and n represents the total number of outputs.
6/ This parameter is not production tested.

1.4 Recommended operating conditions - Continued.

Maximum clock frequency (f_{MAX}):
CLK ..... 70 MHz
TCK ..... 20 MHz
Case operating temperature range (T_C)..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at https://www.ieee.org/).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Test access port controller and scan test registers. The test access port (TAP) controller and scan test registers shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 IEEE 1149.1 compliance. This device shall be compliant with IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$, $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage, TDO 3006	V_{OH1}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$	$I_{OH} = -1.0\ mA$	4.5 V	1, 2, 3	2.5		V
				4.75 V	1, 2, 3	2.7		
			$I_{OH} = -3.0\ mA$	4.5 V	1, 2, 3	2.4		
High level output voltage, any Q 3006	V_{OH2}		$I_{OH} = -3.0\ mA$	4.5 V	1, 2, 3	2.4		
				4.75 V	1, 2, 3	2.7		
			$I_{OH} = -12.0\ mA$	4.5 V	1, 2, 3	2.0		
Low level output voltage, TDO 3007	V_{OL1}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$	$I_{OL} = +20\ mA$	4.5 V	1, 2, 3		0.5	V
Low level output voltage, any Q 3007	V_{OL2}		$I_{OL} = +48\ mA$	4.5 V	1, 2, 3		0.55	
Negative input clamp voltage 3022	V_{IC-}	For input under test, $I_{IN} = -18\ mA$		4.5 V	1, 2, 3		-1.2	V
Input current high 3010	I_{IH1}	For input under test, $V_{IN} = 5.5\ V$		5.5 V	1, 2, 3		100	µA
	I_{IH2}	For input under test, $V_{IN} = 2.7\ V$		5.5 V	1, 2, 3	-1.0	-100	
Double input current high 3010	I_{IHH}	$V_{IN} = 10.0\ V$	TMS	5.5 V	1, 2, 3		1.0	mA
Input current low 3009	I_{IL}	For input under test, $V_{IN} = 0.5\ V$		5.5 V	1, 2, 3		-200	µA
Off-state output leakage current high 3021	I_{OZH}	For control input affecting output under test, $V_{IN} = 2.0\ V$, $V_{OUT} = 2.7\ V$	TDO	5.5 V	1, 2, 3	-1.0	-100	µA
			Any Q		1, 2, 3		50	
Off-state output leakage current low 3020	I_{OZL}	For control input affecting output under test $V_{IN} = 2.0\ V$, $V_{OUT} = 0.5\ V$	TDO	5.5 V	1, 2, 3		-200	µA
			Any Q		1, 2, 3		-50	
Output short circuit current 3011	I_{OS} 4/	$V_{OUT} = 0.0\ V$		5.5 V	1, 2, 3	-100	-225	mA
Supply current outputs high 3005	I_{CCH}	For all inputs, $V_{IN} = V_{CC}$ or GND, V_{OUT} = open		5.5 V	1, 2, 3		7.0	mA
Supply current outputs low 3005	I_{CCL}			5.5 V	1, 2, 3		52.0	
Supply current outputs disabled 3005	I_{CCZ}			5.5 V	1, 2, 3		3.5	
Functional test	5/	$V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$ Verify output V_O See 4.4.1b		4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits		Unit
					Min	Max	
NORMAL MODE							
Propagation delay time CLK to nQ 3003	t_{PLH1} 6/	C_L = 50 pF minimum R_L = 500Ω See figure 5	5.0 V	9	3.0	8.5	ns
			4.5 V and 5.5 V	10, 11	3.0	10.5	
	t_{PHL1} 6/		5.0 V	9	3.0	8.0	
			4.5 V and 5.5 V	10, 11	3.0	10.0	
Propagation delay time, output enable, to nQ 3003	t_{PZH1} 6/		5.0 V	9	3.0	8.5	
			4.5 V and 5.5 V	10, 11	3.0	10.5	
	t_{PZL1} 6/		5.0 V	9	3.5	10.5	
			4.5 V and 5.5 V	10, 11	3.5	12.5	
Propagation delay time, output disable, to nQ 3003	t_{PHZ1} 6/		5.0 V	9	3.0	8.0	
			4.5 V and 5.5 V	10, 11	3.0	10.0	
	t_{PLZ1} 6/		5.0 V	9	2.5	7.5	
			4.5 V and 5.5 V	10, 11	2.5	9.5	
Maximum CLK frequency	f_{MAX1}	C_L = 50 pF minimum R_L = 500Ω See figure 5	5.0 V	9	70		MHz
			4.5 V and 5.5 V	10, 11	70		
TEST MODE							
Propagation delay time, TCK↓ to nQ 3003	t_{PLH2} 6/	C_L = 50 pF minimum R_L = 500Ω See figure 5	5.0 V	9	6.0	15.5	ns
			4.5 V and 5.5 V	10, 11	6.0	21.5	
	t_{PHL2} 6/		5.0 V	9	6.0	15.5	
			4.5 V and 5.5 V	10, 11	6.0	21.5	
Propagation delay time, TCK↓ to TDO 3003	t_{PLH3} 6/		5.0 V	9	3.5	10.5	ns
			4.5 V and 5.5 V	10, 11	3.5	14.0	
	t_{PHL3} 6/		5.0 V	9	3.5	10.5	
			4.5 V and 5.5 V	10, 11	3.5	13.0	
Propagation delay time, TCK↑ to nQ 3003	t_{PLH4} 6/		5.0 V	9	7.5	20.0	ns
			4.5 V and 5.5 V	10, 11	7.5	28.0	
	t_{PHL4} 6/		5.0 V	9	7.5	21.0	
			4.5 V and 5.5 V	10, 11	7.5	29.0	
Propagation delay time, output enable, TCK↓ to nQ 3003	t_{PZH2} 6/		5.0 V	9	6.5	17.0	ns
			4.5 V and 5.5 V	10, 11	6.5	24.0	
	t_{PZL2} 6/		5.0 V	9	7.0	20.0	
			4.5 V and 5.5 V	10, 11	7.0	26.0	
Propagation delay time, output enable, TCK↓ to TDO 3003	t_{PZH3} 6/		5.0 V	9	3.5	10.5	ns
			4.5 V and 5.5 V	10, 11	3.5	11.5	
	t_{PZL3} 6/		5.0 V	9	4.0	11.0	
			4.5 V and 5.5 V	10, 11	4.0	13.5	

See footnotes at end of the table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits		Unit
					Min	Max	
TEST MODE – Continued.							
Propagation delay time, output enable, TCK↑ to nQ 3003	t_{PZH4} 6/	C_L = 50 pF minimum R_L = 500Ω See figure 5	5.0 V	9	8.0	22.0	ns
			4.5 V and 5.5 V	10, 11	8.0	30.0	
	t_{PZL4} 6/		5.0 V	9	8.0	25.0	
			4.5 V and 5.5 V	10, 11	8.0	32.0	
Propagation delay time, output disable, TCK↓ to nQ 3003	t_{PHZ2} 6/		5.0 V	9	6.0	18.0	ns
			4.5 V and 5.5 V	10, 11	6.0	24.0	
	t_{PLZ2} 6/		5.0 V	9	6.0	17.0	
			4.5 V and 5.5 V	10, 11	6.0	23.0	
Propagation delay time, output disable, TCK↓ to TDO 3003	t_{PHZ3} 6/		5.0 V	9	3.0	11.5	ns
			4.5 V and 5.5 V	10, 11	3.0	13.0	
	t_{PLZ3} 6/		5.0 V	9	3.0	10.0	
			4.5 V and 5.5 V	10, 11	3.0	13.0	
Propagation delay time, output disable, TCK↑ to nQ 3003	t_{PHZ4} 6/		5.0 V	9	8.0	22.0	ns
			4.5 V and 5.5 V	10, 11	8.0	31.0	
	t_{PLZ4} 6/		5.0 V	9	8.0	22.0	
			4.5 V and 5.5 V	10, 11	8.0	31.0	
Maximum TCK frequency	f_{MAX2}		5.0 V	9	20		MHz

1/ For tests not listed in the referenced MIL-STD-883, utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V_{IN} = GND or $V_{IN} \ge 3.0$ V.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I at $4.5\ V \le V_{CC} \le 5.5$ V.

4/ Not more than one output should be tested at one time, and the duration of the test condition should not exceed one second.

5/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

6/ For propagation delay tests, all paths must be tested.

Case outlines	L	3	Case outlines	**L**	**3**
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	CLK	NC	15	8D	NC
2	1Q	5D	16	7D	5Q
3	2Q	4D	17	6D	6Q
4	3Q	3D	18	V_{CC}	7Q
5	4Q	2D	19	5D	8Q
6	GND	1D	20	4D	TDO
7	5Q	$\overline{OE}$	21	3D	TMS
8	6Q	NC	22	2D	NC
9	7Q	CLK	23	1D	TCK
10	8Q	1Q	24	$\overline{OE}$	TDI
11	TDO	2Q	25		8D
12	TMS	3Q	26		7D
13	TCK	4Q	27		6D
14	TDI	GND	28		V_{CC}

NC = No internal connection

Terminal description	
Terminal symbol	Description
nD (n = 1 to 8)	Data inputs
nQ (n = 1 to 8)	Outputs
$\overline{OE}$	Output enable control input
CLK	Clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select input
TCK	Test clock input

FIGURE 1. Terminal connections.

Inputs			Outputs
$\overline{OE}$	CLK	nD	nQ
L	↑	H	H
L	↑	L	L
L	L	X	Q_O
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance
↑ = Low-to-high clock transition
Q_0 = The level of Q before the indicated steady-state input conditions were established

FIGURE 2. Truth table.

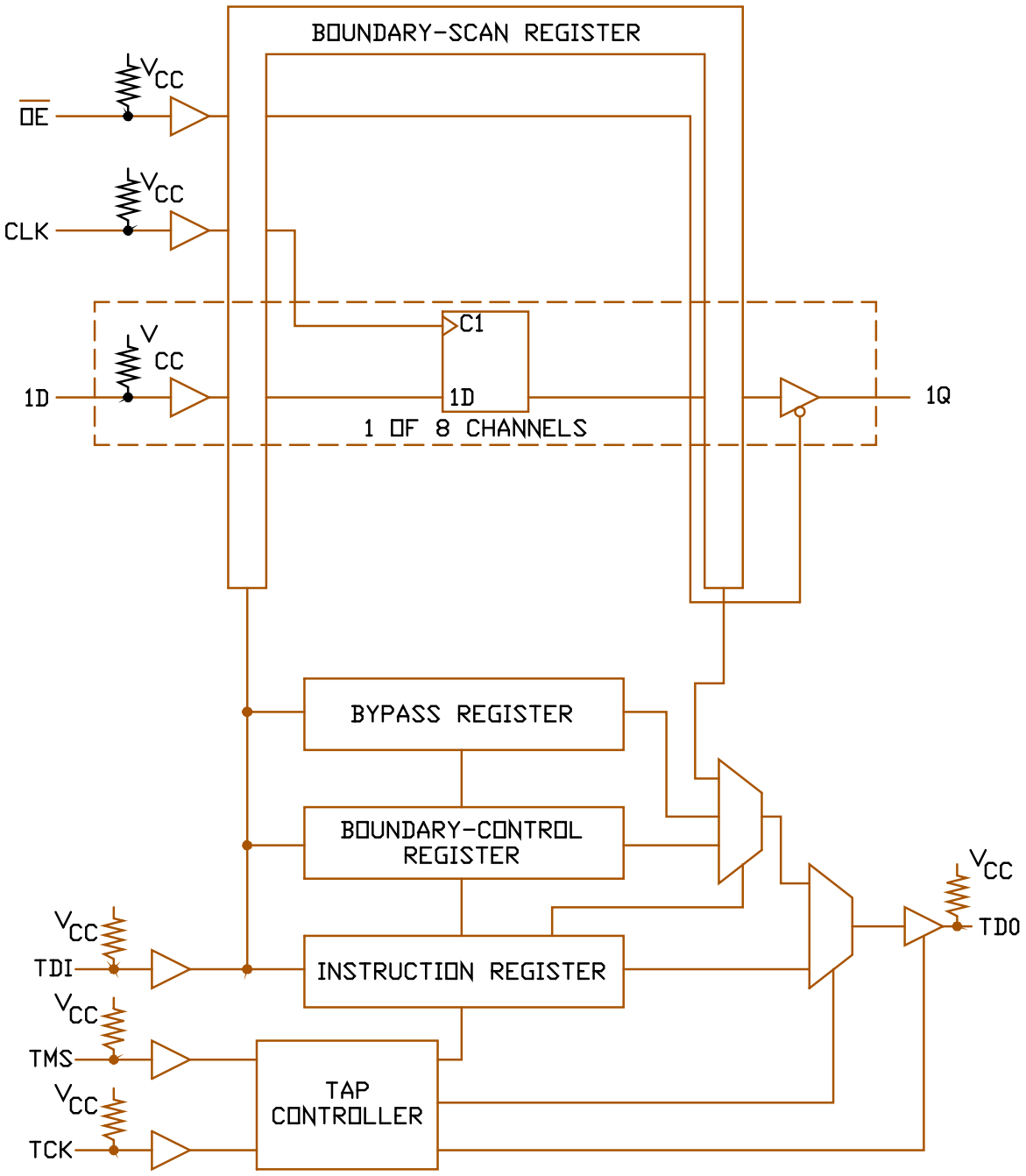


FIGURE 3. Block diagram.

Test access port (TAP) controller state diagram

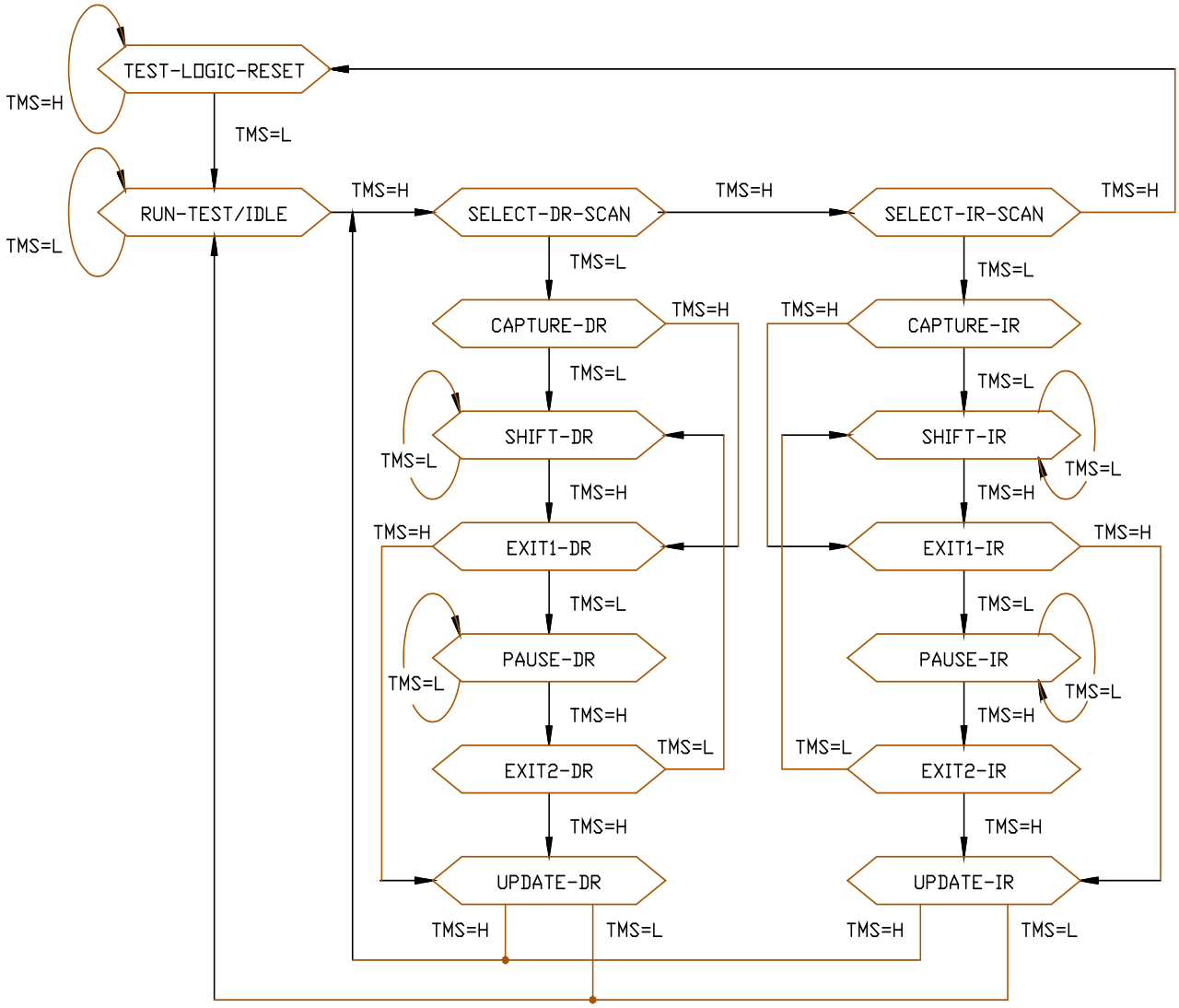
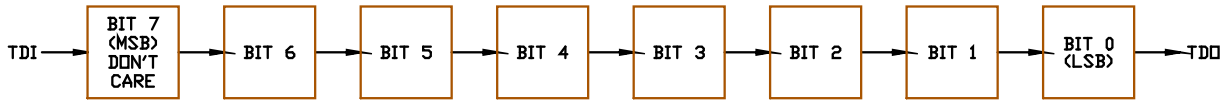


FIGURE 4. Test access port controller and scan test registers.

Instruction register (IR) order of scan



NOTE: During capture-IR, the IR captures the binary value 10000001. At power up or in the test-logic-reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction.

Instruction register opcodes

Binary code 1/ Bit 7 → Bit 0 MSB → LSB	SCOPE™ opcode	Description	Selected data register	Mode
X0000000	EXTEST	Boundary scan	Boundary scan	Test
X0000001	BYPASS 2/	Bypass scan	Bypass	Normal
X0000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
X0000011	INTEST	Boundary scan	Boundary scan	Test
X0000100	BYPASS 2/	Bypass scan	Bypass	Normal
X0000101	BYPASS 2/	Bypass scan	Bypass	Normal
X0000110	HIGHZ (TRIBYP)	Control boundary to high impedance	Bypass	Modified test
X0000111	CLAMP (SETBYP)	Control boundary to 1/0	Bypass	Test
X0001000	BYPASS 2/	Bypass scan	Bypass	Normal
X0001001	RUNT	Boundary run test	Bypass	Test
X0001010	READBN	Boundary read	Boundary scan	Normal
X0001011	READBT	Boundary read	Boundary scan	Test
X0001100	CELLTST	Boundary self test	Boundary scan	Normal
X0001101	TOPHIP	Boundary toggle outputs	Bypass	Test
X0001110	SCANCN	Boundary-control register scan	Boundary control	Normal
X0001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

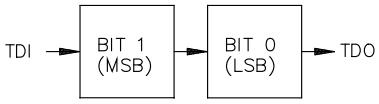
1/ Bit 7 is a don't-care bit; X = don't care.
2/ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in this device.

FIGURE 4. Test access port controller and scan test registers - Continued.

Boundary-scan register (BSR) configuration

BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal
17	CLK	15	1D	7	1Q
16		14	2D	6	2Q
---	---	13	3D	5	3Q
---	---	12	4D	4	4Q
---	---	11	5D	3	5Q
---	---	10	6D	2	6Q
---	---	9	7D	1	7Q
---	---	8	8D	0	8Q

Boundary-control register (BCR) order of scan

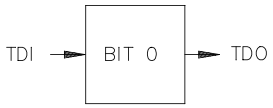


NOTE: During capture-DR (DR stands for data register), the contents of BCR are not changed. At power up or in the test-logic-reset state, the BCR is reset to the binary value 10, which selects the PSA test operation.

Boundary-control register opcodes

Binary code Bit 1 → Bit 0 MSB → LSB	Description
00	Sample inputs/toggle outputs (TOPSIP)
01	Pseudo-random pattern generation/16-bit mode (PRPG)
10	Parallel signature analysis/16-bit mode (PSA)
11	Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG)

Bypass register order of scan



NOTE: During capture-DR, the bypass register captures a logic 0.

FIGURE 4. Test access port controller and scan test registers - Continued.

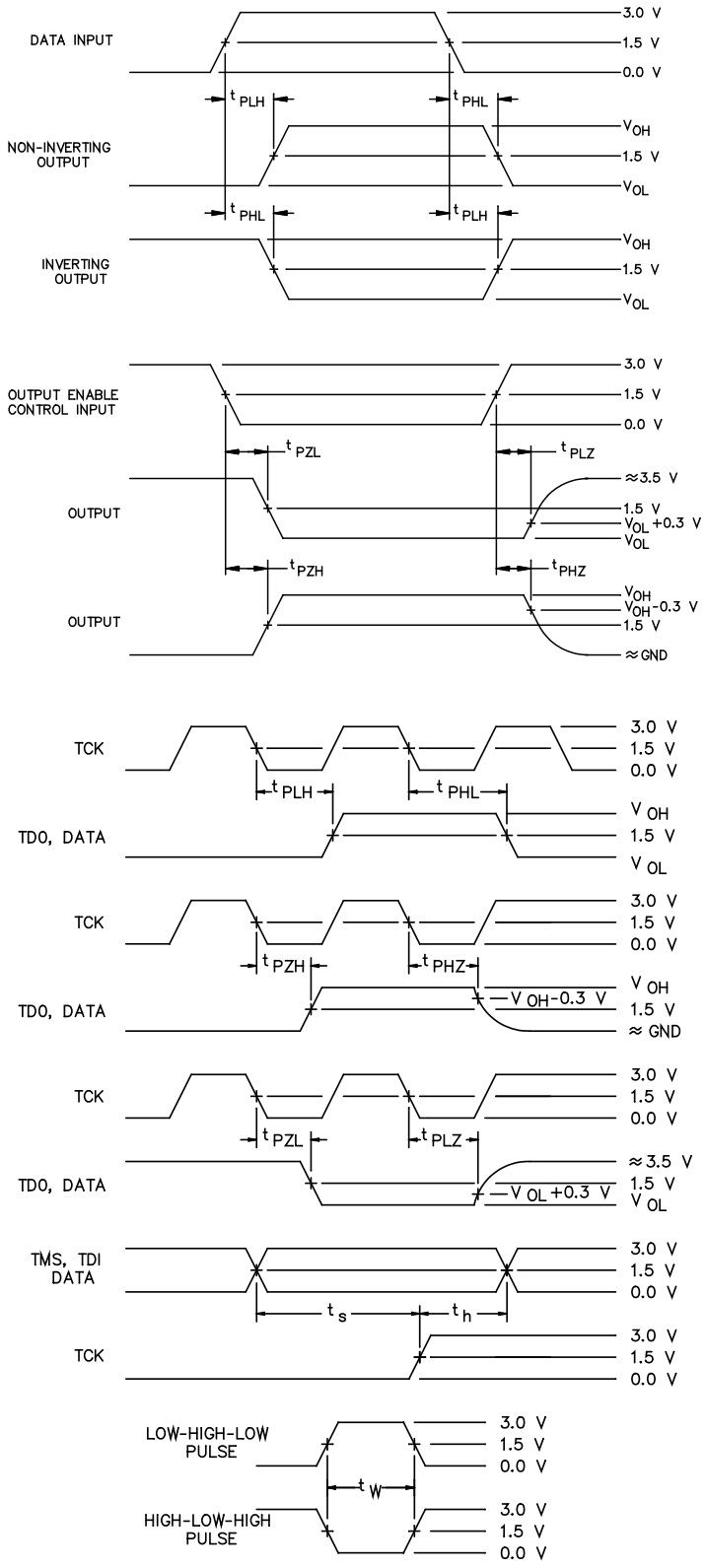
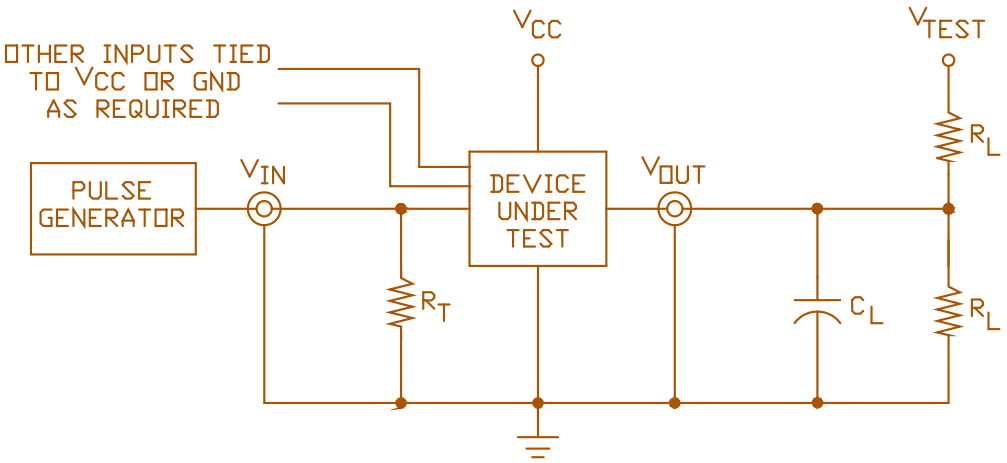


FIGURE 5. Switching waveforms and test circuit.



NOTES:

1. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 7.0 V.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_L = 500Ω or equivalent.
6. R_T = 50Ω or equivalent.
7. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8	1, 2, 3, 7, 8
Group D end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8	1, 2, 3, 7, 8
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{IL} ..... Input current low.
I_{IH} ..... Input current high.
T_C ..... Case temperature.
T_A ..... Ambient temperature.
V_{CC} ..... Positive supply voltage.
V_{IC-} ..... Negative input clamp voltage.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-03-15

Approved sources of supply for SMD 5962-91727 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9172701QLA	01295	SNJ54BCT8374AJT
5962-9172701Q3A	01295	SNJ54BCT8374AFK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243