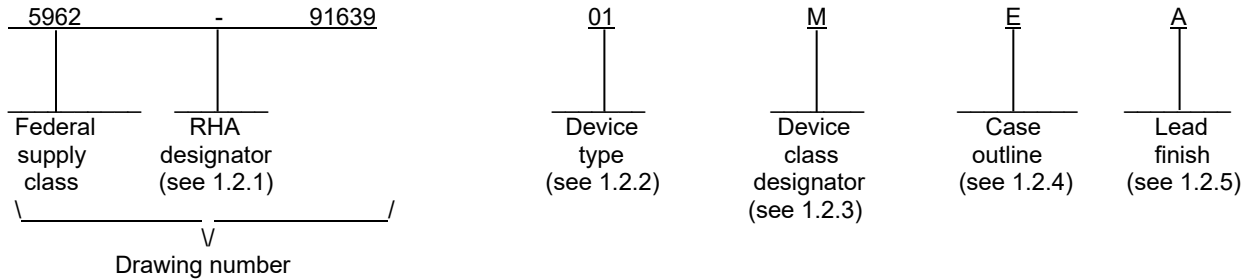


1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	26C31	CMOS quad differential line driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
X	See figure 1	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage range (VCC)	-0.5 V dc to 7.0 V dc
DC input voltage range (VIN)	-0.5 V dc to VCC +0.5 V dc
DC output voltage range (VOUT)	-0.5 V dc to 7.0 V dc
DC output current, per pin (IOUT)	±150 mA
Input, output clamp diode current (I _{IK} , I _{OK})	±20 mA
DC V _{CC} or GND current, per pin (ICC)	±150 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 4 seconds)	260°C
Junction temperature (T _J)	150°C
Thermal resistance, junction-to-case (θ _{JC}):	
Cases E, F, 2	See MIL-STD-1835
Case X	11°C/W
Thermal resistance, junction-to-ambient (θ _{JA}):	
Case E	+100°C/W
Case F	+150°C/W
Case X	+116°C/W
Case 2	+85°C/W
Power dissipation (P _D): (T _A = +25°C)	
Case E	1375 mW
Case F	1000 mW
Case X	1293 mW
Case 2	1375 mW

1.4 Recommended operating conditions.

Supply voltage range (VCC)	4.5 V dc to 5.5 V dc
DC input or output voltage range (VIN, VOUT)	0 V dc to VCC
Ambient operating temperature range (T _A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 AC test circuit. The AC test circuit shall be as specified on figure 6.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ TA ≤ +125°C -4.5 V ≤ VCC ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Logical 1 input voltage	VIH		1, 2, 3	01	2.0		V	
Logical 0 input voltage	VIL		1, 2, 3	01		0.8	V	
Logical 1 output voltage	VOH	VIN = VIH or VIL, ICC = 4.5 V, IOU _T = -20 mA	1	01	2.4		V	
			2, 3		2.2			
Logical 0 output voltage	VOL	VIN = VIH or VIL, VCC = 4.5 V, IOU _T = 20 mA	1, 2, 3	01		0.5	V	
Differential output voltage	VT	VCC = 4.5 V, RL = 100Ω <u>1/</u>	1, 2, 3	01	2.0		V	
Difference in differential output	VT - V̄T	VCC = 4.5 V, RL = 100Ω <u>1/</u>	1, 2, 3	01		0.4	V	
Common mode output voltage	VOS	VCC = 5.5 V, RL = 100Ω <u>1/</u>	1, 2, 3	01		3.0	V	
Difference in common mode output	VOS - V̄OS	VCC = 5.5 V, RL = 100Ω <u>1/</u>	1, 2, 3	01		0.4	V	
Input current	IIN	VIN = VCC, GND, VIH, or VIL, VCC = 5.5 V	1, 2, 3	01	-1.0	+1.0	μA	
Quiescent power supply current	ICC	IOU _T = 0 μA, VCC = 4.5 V, VIN = 5 V or GND <u>2/</u>	1, 2, 3	01		500	μA	
			1			3.0		mA
			2, 3			3.2		
TRI-STATE output leakage current	IOZ	VOUT = 2.5 V or 0.5 V, ENABLE = VIL, VCC = 5.5 V, ENABLĒ = VIH	1, 2, 3	01	-20	+20	μA	
Output short circuit current	ISC	VIN = VCC or GND, <u>1/</u> , <u>3/</u> VCC = 5.5 V	1	01	-150	-30	mA	
			2, 3		-170	-30		
Output leakage current "power off"	IOFF	VCC = 0 V, VOUT = 6 V	1, 2, 3	01		100	μA	
		VCC = 0 V, VOUT = 0 V			-100			
Functional tests to output		See 4.4.1b	7, 8	01				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55°C ≤ TA ≤ +125°C -4.5 V ≤ VCC ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay input to output	tPLH	S1 open <u>4/</u>	9, 10, 11	01		14	ns
	tPHL					14	
Skew		S1 open <u>4/ 5/</u>	9, 10, 11	01		4	ns
Output rise time	tTLH	S1 open <u>4/</u>	9, 10, 11	01		14	ns
Output fall time	tTHL	S1 open <u>4/</u>	9, 10, 11	01		14	ns
Output enable time	tPZH	S1 closed <u>4/</u>	9, 10, 11	01		22	ns
	tPZL					28	
Output disable time	tPHZ	S1 closed <u>4/ 6/</u>	9, 10, 11	01		16	ns
	tPLZ					16	

1/ See EIA specification RS-422 for exact test conditions.

2/ Measure per input. All other inputs at 5 V or GND.

3/ This is a current forced when a high output is shorted to GND. Only one output shall be shorted at a time.

4/ See figures 5 and 6. Rise time (t_r) ≤ 6 ns and fall time (t_f) ≤ 6 ns. VCC = 5.0 V.

5/ Skew is defined as the difference in propagation delay between complementary output at 50 % point.

6/ Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistor turning off.

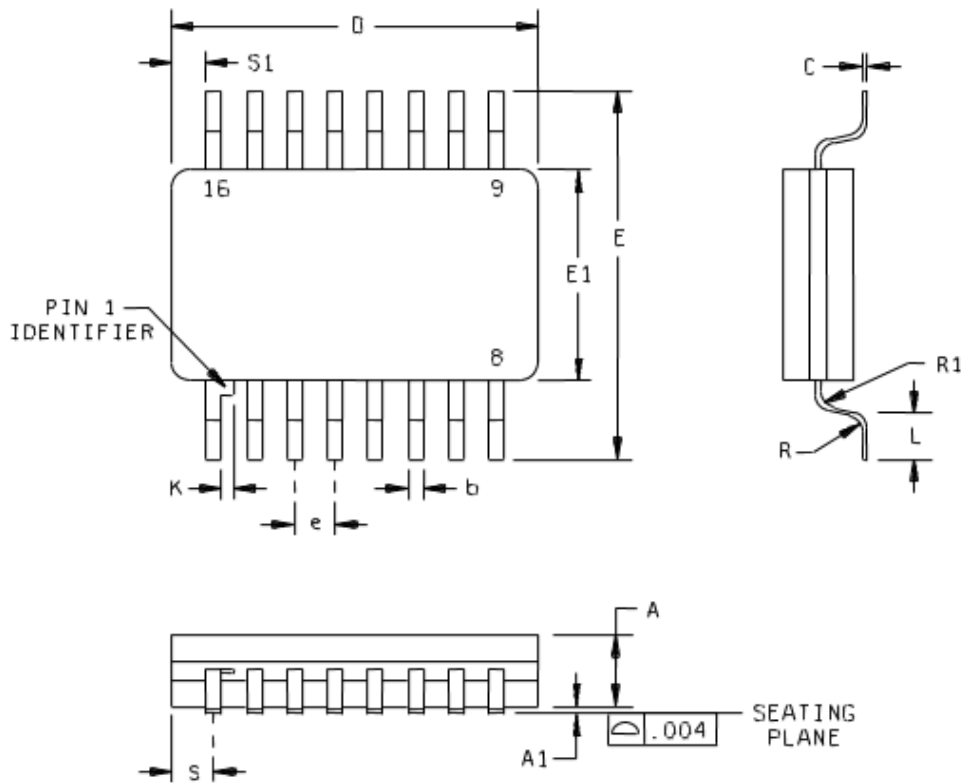
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Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.050	.080	1.27	2.03	
A1	.004	.012	0.10	0.30	
b	.015	.019	0.38	0.48	2
C	.004	.008	0.10	0.20	2
D	---	.390	---	9.91	
E	.400	.420	10.16	10.67	
E1	.245	.270	6.22	6.86	
e	.050 BSC		1.27 BSC		
K	.008	.012	0.20	0.30	
L	.037	.043	0.94	1.09	
R	.013	.017	0.33	0.43	
R1	.013	.017	0.33	0.43	
S	---	.018	---	0.46	
S1	.005	---	0.13	---	

NOTES:

1. The U.S. government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Maximum limits may be increased by .003 inches after lead finish is applied.

FIGURE 1. Case outline X.

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Device type	01	
Case outlines	E, F, and X	2
Terminal number	Terminal symbol	
1	INPUT A	NC
2	CHANNEL A2 OUTPUT	INPUT A
3	CHANNEL A1 OUTPUT	CHANNEL A2 OUTPUT
4	ENABLE	CHANNEL A1 OUTPUT
5	CHANNEL B1 OUTPUT	ENABLE
6	CHANNEL B2 OUTPUT	NC
7	INPUT B	CHANNEL B1 OUTPUT
8	GND	CHANNEL B2 OUTPUT
9	INPUT C	INPUT B
10	CHANNEL C2 OUTPUT	GND
11	CHANNEL C1 OUTPUT	NC
12	$\overline{\text{ENABLE}}$	INPUT C
13	CHANNEL D1 OUTPUT	CHANNEL C2 OUTPUT
14	CHANNEL D2 OUTPUT	CHANNEL C1 OUTPUT
15	INPUT D	$\overline{\text{ENABLE}}$
16	VCC	NC
17	---	CHANNEL D1 OUTPUT
18	---	CHANNEL D2 OUTPUT
19	---	INPUT D
20	---	VCC

NC = No connection

FIGURE 2. Terminal connections.

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Active high ENABLE	Active low <u>ENABLE</u>	Input	Non-inverting output	Inverting output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state
H = High logic state
X = Don't care
Z = TRI-STATE (high impedance)

FIGURE 3. Truth table.

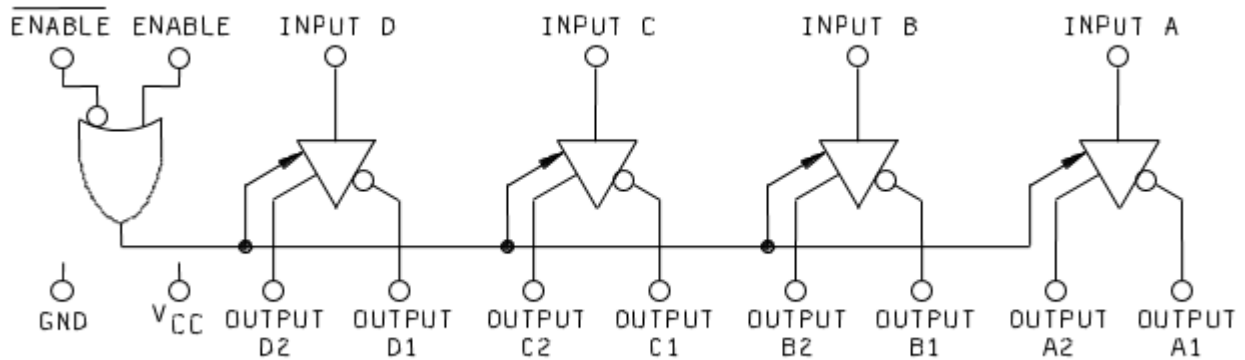


FIGURE 4. Logic diagram.

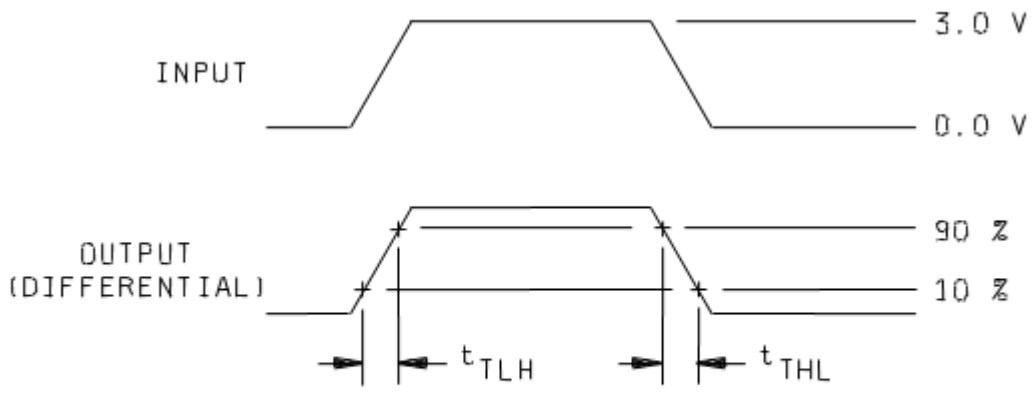
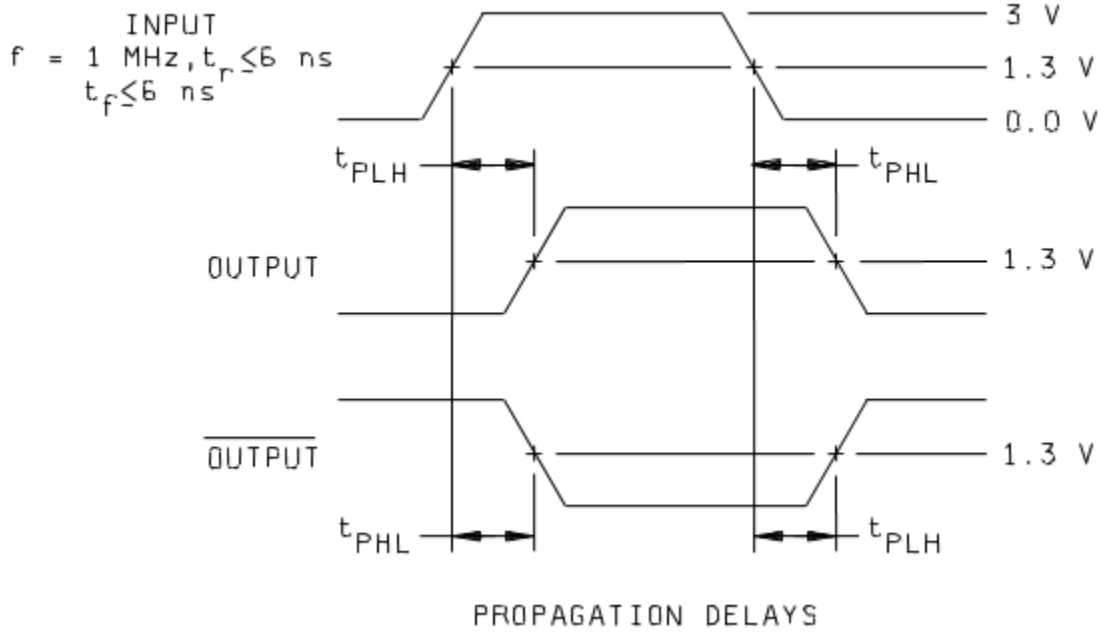
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INPUT PULSE: $f = 1 \text{ MHz}, \text{DUTY CYCLE} \leq 50\%; t_r = t_f \leq 6 \text{ ns}$

FIGURE 5. Timing waveforms.

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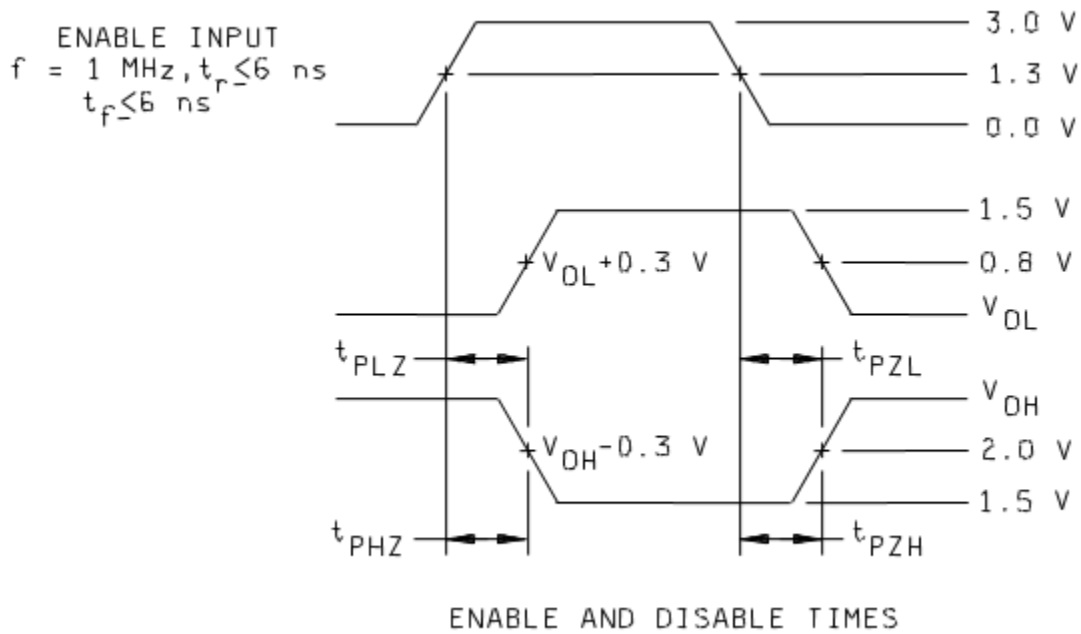
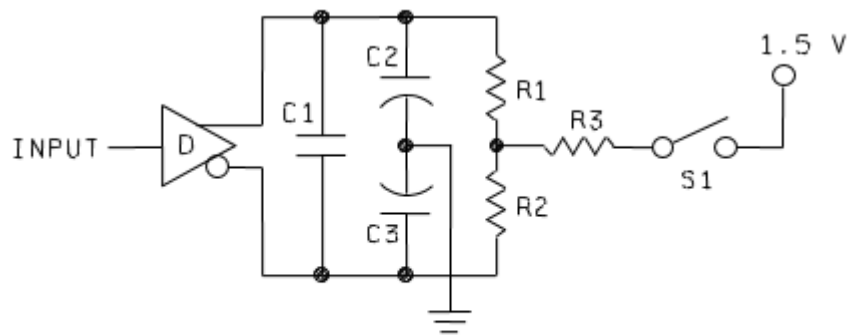


FIGURE 5. Timing waveforms - continued.



NOTE: $C1 = C2 = C3 = 40 \text{ pF}$, $R1 = R2 = 50 \Omega$, $R3 = 500 \Omega$

FIGURE 6. AC test circuit.

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3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 77 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) TA = +125°C, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	---	1
Final electrical parameters (see 4.2)	1, 2, 3, 9 <u>1/</u>	1, 2, 3, 9 <u>1/</u>	1, 2, 3, 9 <u>1/</u>
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device.

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. TA = +125°C, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at TA = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

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6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-01-06

Approved sources of supply for SMD 5962-91639 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9163901MEA	01295	DS26C31MJ/883
5962-9163901MEA	01295	AM26C31
5962-9163901MFA	01295	DS26C31MW/883
5962-9163901MFA	01295	AM26C31
5962-9163901M2A	01295	DS26C31ME/883
5962-9163901M2A	01295	AM26C31
5962-9163901MXA	<u>3/</u>	DS26C31MWG/883
5962-9163901QEA	01295	AM26C31MJB
5962-9163901QFA	01295	AM26C31MWB
5962-9163901Q2A	01295	AM26C31MFKB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
PO Box 660199
Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.