

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R147-92. - LTG	92-03-13	Monica L. Poelking
B	Redraw the switching waveforms in figure 4, switching waveforms and test circuit. Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. - LTG	06-06-23	Thomas M. Hess
C	Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. - jak	12-11-06	Thomas M. Hess

REV																			
SHEET																			
REV	C																		
SHEET	15																		
REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
PMIC N/A	PREPARED BY	<p>Marcia B. Kelleher</p> <p><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a></p>																	
<p><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p>AMSC N/A</p>	CHECKED BY	<p>Thomas J. Ricciuti</p>																	
	APPROVED BY	<p>Michael A. Frye</p>																	
	DRAWING APPROVAL DATE	<p>91-02-28</p>																	
	REVISION LEVEL	SIZE	CAGE CODE	<p><b>5962-91555</b></p>															
	C	A	67268	SHEET 1 OF 15															



1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ).....	-0.5 V dc to +7.0 V dc
DC input voltage range ( $V_{IN}$ ):	
I/O ports .....	-0.5 V dc to +5.5 V dc
Excluding I/O ports.....	-0.5 V dc to +7.0 V dc
Voltage applied to any output in the high state ( $V_{OUT}$ ).....	-0.5 V dc to $V_{CC}$
Voltage applied to any output in the disabled state ( $V_{OUT}$ ) .....	-0.5 V dc to +5.5 V dc
Current into any output in the low state .....	96 mA
Input clamp current ( $I_{IC}$ ) .....	-30 mA
Storage temperature range ( $T_{STG}$ ) .....	-65°C to +150°C
Maximum power dissipation ( $P_D$ ) .....	579.7 mW 2/
Lead temperature (soldering, 10 seconds).....	+300°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	See MIL-STD-1835
Junction temperature ( $T_J$ ) .....	+175°C

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ ).....	+4.5 V dc to +5.5 V dc
Minimum high level input voltage ( $V_{IH}$ ) .....	2.0 V dc
Maximum low level input voltage ( $V_{IL}$ ) .....	0.8 V dc
Maximum input clamp current ( $I_{IC}$ ).....	-18 mA
Maximum high level output current ( $I_{OH}$ ).....	-12 mA
Maximum low level output current ( $I_{OL}$ ).....	+48 mA
Case operating temperature range ( $T_C$ ) .....	-55°C to +125°C
Minimum setup time, Am or Bm before CLKAB or CLKBA going high ( $t_s$ ):	
$T_C = 25^\circ\text{C}$ , $V_{CC} = 5.0$ V.....	6.0 ns
$T_C = -55^\circ\text{C}$ to +125°C, $V_{CC} = 4.5$ V and 5.5 V .....	7.0 ns
Minimum hold time, Am or Bm after CLKAB or CLKBA going high ( $t_h$ ) ..	1.0 ns
Minimum pulse duration, CLKBA or CLKAB high or low ( $t_w$ ) .....	5.5 ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Maximum power dissipation is defined as  $P_D = V_{CC} \times I_{CC} + (\text{number of outputs}) \times V_{OL} \times I_{OL}$  and must be able to withstand the additional  $P_D$  due to the short circuit test, e.g.,  $I_{OS}$ .

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

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3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 126 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V V <sub>IH</sub> = 2.0 V V <sub>IL</sub> = 0.8 V	I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -12 mA	1, 2, 3	All	2.4 2.0		V
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V V <sub>IH</sub> = 2.0 V V <sub>IL</sub> = 0.8 V	I <sub>OL</sub> = 48 mA	1, 2, 3	All		0.55	V
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA		1, 2, 3	All		-1.2	V
High level input current <u>1/</u>	A or B port	I <sub>IH1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V	1, 2, 3	All		1.0	mA
	Control inputs						1.0	
	A or B port	I <sub>IH2</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V	1, 2, 3	All		70	μA
	Control inputs						20	
Low level input current <u>1/</u>	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V		1, 2, 3	All		-1.0	mA
Short-circuit output current <u>2/</u>	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.0 V		1, 2, 3	All	-100	-225	mA
Supply current, outputs high	I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V Outputs open	V <sub>IN</sub> = 4.5 V	1, 2, 3	All		9	mA
Supply current, outputs low	I <sub>CCL</sub>		V <sub>IN</sub> = 0.0 V				67	
Supply current, outputs disabled	I <sub>CCZ</sub>		V <sub>IN</sub> = 0.0 V				16	
Functional tests <u>3/</u>		See 4.4.1b		7, 8	All			
Maximum clock frequency	f <sub>MAX</sub>	C <sub>L</sub> = 50 pF R1 = R2 = 500Ω See figure 4	V <sub>CC</sub> = 5.0 V	9	All	90		MHz
			V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		90		
Propagation delay time, CLKBA to Am or CLKAB to Bm	t <sub>PLH1</sub>	V <sub>CC</sub> = 5.0 V V <sub>CC</sub> = 4.5 V and 5.5 V	V <sub>CC</sub> = 5.0 V	9	All	3.6	9.4	ns
			V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		3.6	12.4	
	t <sub>PHL1</sub>		V <sub>CC</sub> = 5.0 V	9	All	3.9	9.2	
			V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		3.9	11.5	
Propagation delay time, Am to Bm or Bm to Am	t <sub>PLH2</sub>	V <sub>CC</sub> = 5.0 V V <sub>CC</sub> = 4.5 V and 5.5 V	V <sub>CC</sub> = 5.0 V	9	All	3.1	8.1	ns
			V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		3.1	11.1	
	t <sub>PHL2</sub>		V <sub>CC</sub> = 5.0 V	9	All	3.7	8.9	
			V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		3.7	12.1	
Propagation delay time, SAB to Bm or SBA to Am (with Am or Bm high) <u>4/</u>	t <sub>PLH3</sub>	V <sub>CC</sub> = 5.0 V V <sub>CC</sub> = 4.5 V and 5.5 V	V <sub>CC</sub> = 5.0 V	9	All	4.5	11.2	ns
			V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		4.5	15.2	
	t <sub>PHL3</sub>		V <sub>CC</sub> = 5.0 V	9	All	3.3	8.1	
			V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		3.3	9.8	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified		Group A subgroup s	Device type	Limits		Unit
						Min	Max	
Propagation delay time, SBA to Am or SAB to Bm (with Am or Bm low) 4/	t <sub>PLH4</sub>	C <sub>L</sub> = 50 pF R1 = R2 = 500Ω See figure 4	V <sub>CC</sub> = 5.0 V	9	All	3.9	10.2	ns
			V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		3.9	13.3	
	t <sub>PHL4</sub>		V <sub>CC</sub> = 5.0 V	9	All	4.7	10.8	
			V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		4.7	13.7	
Propagation delay time, output enable, $\overline{OE}$ to Am or $\overline{OE}$ to Bm	t <sub>PZH1</sub>	V <sub>CC</sub> = 5.0 V	9	All	4.0	10.7	ns	
		V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		4.0	14.0		
	t <sub>PZL1</sub>	V <sub>CC</sub> = 5.0 V	9	All	4.6	11.8		
		V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		4.6	15.4		
Propagation delay time, output disable, $\overline{OE}$ to Am or $\overline{OE}$ to Bm	t <sub>PHZ1</sub>	V <sub>CC</sub> = 5.0 V	9	All	4.0	9.4	ns	
		V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		4.0	12.0		
	t <sub>PLZ1</sub>	V <sub>CC</sub> = 5.0 V	9	All	3.4	9.3		
		V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		3.4	11.6		
Propagation delay time, output enable, DIR to Am or DIR to Bm	t <sub>PZH2</sub>	V <sub>CC</sub> = 5.0 V	9	All	2.8	10.7	ns	
		V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		2.8	14.0		
	t <sub>PZL2</sub>	V <sub>CC</sub> = 5.0 V	9	All	3.8	11.9		
		V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		3.8	15.6		
Propagation delay time, output disable, DIR to Am or DIR to Bm	t <sub>PHZ2</sub>	V <sub>CC</sub> = 5.0 V	9	All	3.8	10.7	ns	
		V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		3.8	13.2		
	t <sub>PLZ2</sub>	V <sub>CC</sub> = 5.0 V	9	All	3.2	9.9		
		V <sub>CC</sub> = 4.5 V and 5.5 V	10, 11		3.2	12.6		

1/ For I/O ports, the parameters I<sub>IH2</sub> and I<sub>IL</sub> include the off-state output current.

2/ Not more than one output should be shorted at one time and the duration of the test condition should not exceed one second.

3/ Functional tests shall be conducted at input test conditions of 0.4 V ≤ V<sub>IL</sub> ≤ 0.8 V and 2.0 V ≤ V<sub>IH</sub> ≤ 2.4 V for V<sub>CC</sub> = 4.5 V and is repeated for V<sub>CC</sub> = 5.5 V.

4/ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

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Device type	All	
Case outlines	L and K	3
Terminal number	Terminal symbol	Terminal symbol
1	CLKAB	NC
2	SAB	CLKAB
3	DIR	SAB
4	A1	DIR
5	A2	A1
6	A3	A2
7	A4	A3
8	A5	NC
9	A6	A4
10	A7	A5
11	A8	A6
12	GND	A7
13	B8	A8
14	B7	GND
15	B6	NC
16	B5	B8
17	B4	B7
18	B3	B6
19	B2	B5
20	B1	B4
21	$\overline{OE}$	B3
22	SBA	NC
23	CLKBA	B2
24	V <sub>cc</sub>	B1
25	----	$\overline{OE}$
26	----	SBA
27	----	CLKBA
28	----	V <sub>cc</sub>

NC = No connection

FIGURE 1. Terminal connections.

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Inputs						Data I/O		Operation or function
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 through A8	B1 through B8	
X	X	↑	X	X	X	Input	Unspecified <sup>1/</sup>	Store A, B unspecified <sup>1/</sup>
X	X	X	↑	X	X	Unspecified <sup>1/</sup>	Input	Store B, A unspecified <sup>1/</sup>
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

H = High voltage level

L = Low voltage level

X = Irrelevant

↑ = Low-to-high transition

<sup>1/</sup> The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

FIGURE 2. Truth table.

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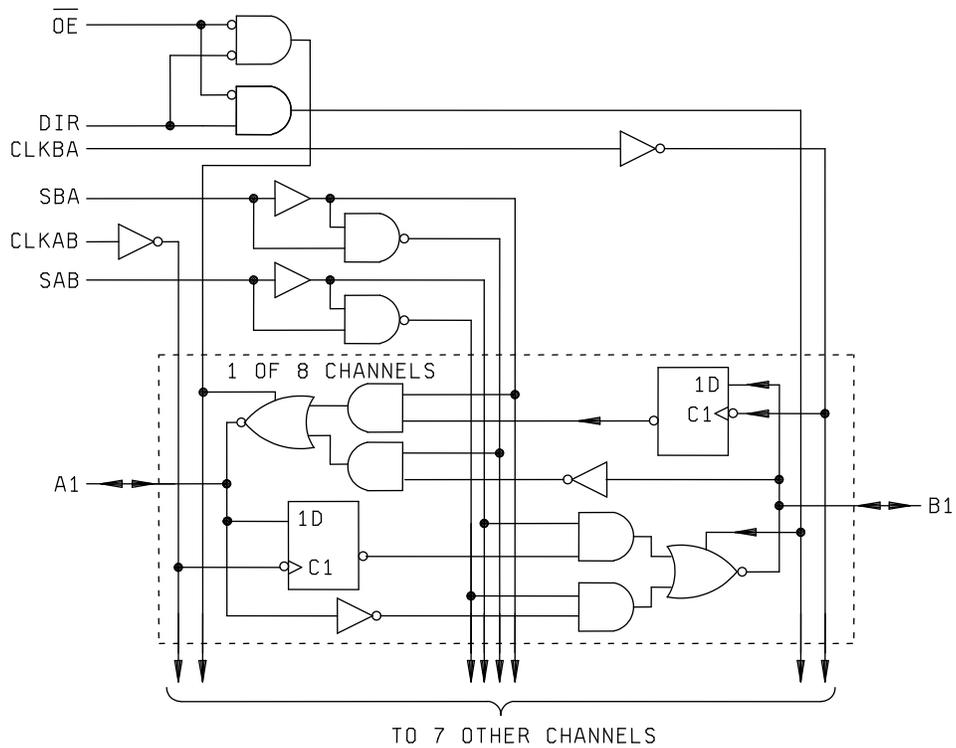


FIGURE 3. Logic diagram.

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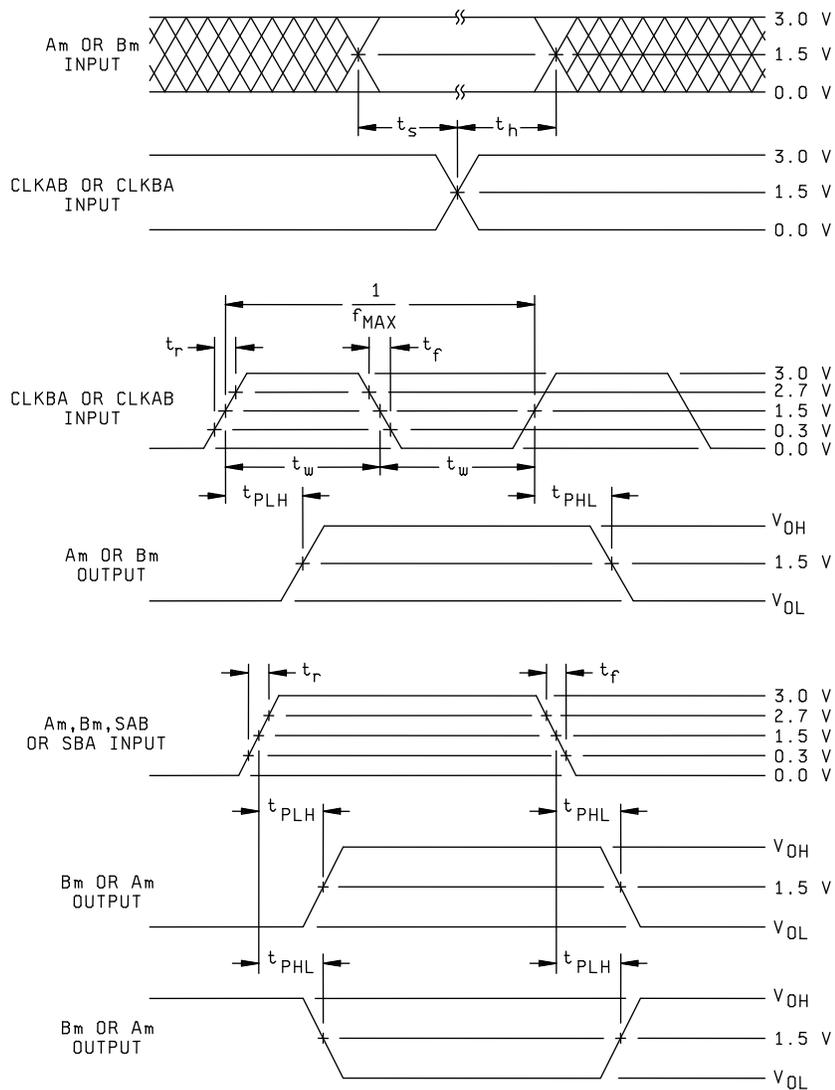


FIGURE 4. Switching waveforms and test circuit.

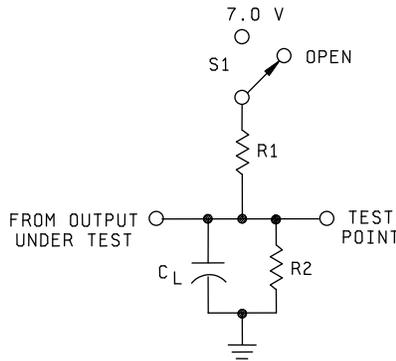
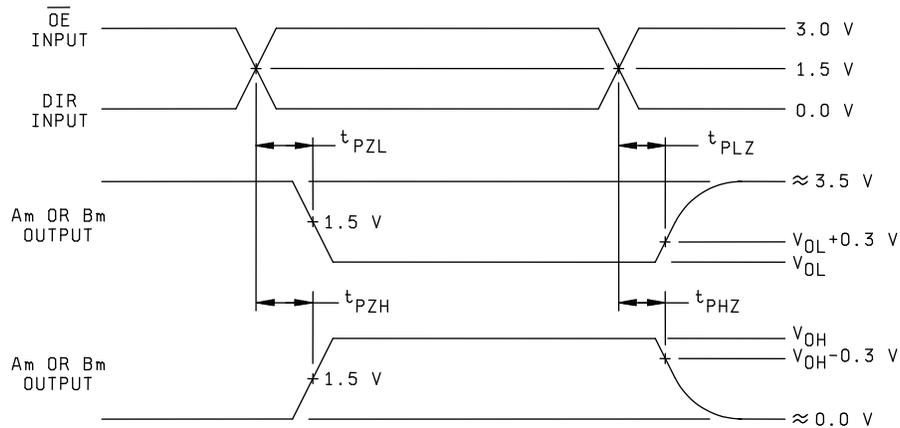
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**NOTES:**

1. When measuring  $t_{PLZ}$  and  $t_{PZL}$ :  $S1 = 7.0 \text{ V}$ . When measuring  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PZH}$ , and  $t_{PHZ}$ :  $S1 = \text{Open}$ .
2. The  $t_{PZL}$  and  $t_{PLZ}$  reference waveform is for the output under test with internal conditions such that the output is at  $V_{OL}$  except when disabled by the output enable control. The  $t_{PZH}$  and  $t_{PHZ}$  reference waveform is for the output under test with internal conditions such that the output is at  $V_{OH}$  except when disabled by the output enable control.
3.  $C_L = 50 \text{ pF}$  minimum or equivalent (includes test jig and probe capacitance).
4.  $R1 = R2 = 500\Omega$  or equivalent.
5. All input pulses are supplied by the generators having the following characteristics:  $V_{IN} = 0.0 \text{ V}$  to  $3.0 \text{ V}$ ;  $\text{PRR} \leq 10 \text{ MHz}$ ;  $Z_O = 50\Omega$ ;  $t_r \leq 2.5 \text{ ns}$ ;  $t_f \leq 2.5 \text{ ns}$ ;  $t_r$  and  $t_f$  shall be measured from  $0.3 \text{ V}$  to  $2.7 \text{ V}$  and from  $2.7 \text{ V}$  to  $0.3 \text{ V}$ , respectively; duty cycle = 50 percent.
6. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit – Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T<sub>A</sub> = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table as specified on figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>2/ 3/</u>
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11 <u>3/</u>
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1, 7, and deltas.

3/ Delta limits shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table II herein.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0540.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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DATE: 12-12-06

Approved sources of supply for SMD 5962-91555 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9155501MLA	01295	SNJ54BCT646JT
5962-9155501MKA	01295	SNJ54BCT646W
5962-9155501M3A	01295	SNJ54BCT646FK

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

01295

Vendor name  
and address

Texas Instruments Incorporated  
Semiconductor Group  
8505 Forest Ln.  
P.O. Box 660199  
Dallas, TX 75243  
Point of contact:

U.S. Highway 75 South  
P.O. Box 84, M/S 853  
Sherman, TX 75090-9493

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