

REVISIONS

| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
|-----|---|-----------------|-------------------|
| A | Updated to current boilerplate for 5 year review. lhl | 12-07-27 | Charles F. Saffle |

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

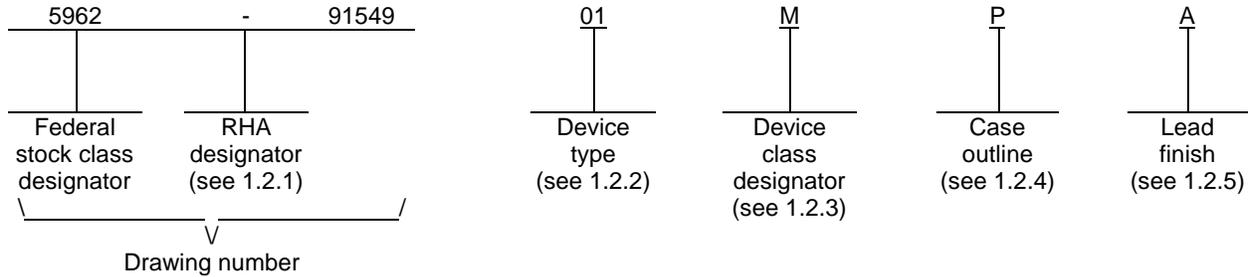
| | | | | | | | | | | | | | | | | | | | | |
|----------------------|-----------|----|----|----|----|---|---|---|---|---|---|---|----|----|----|----|----|---|---|---|
| REV SHEET | | | | | | | | | | | | | | | | | | | | |
| REV SHEET | A | A | A | A | A | | | | | | | | | | | | | | | |
| REV SHEET | 15 | 16 | 17 | 18 | 19 | | | | | | | | | | | | | | | |
| REV STATUS OF SHEETS | REV SHEET | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | | |

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|---|-----------------------------------|---|---|-----------|---------------------------|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| PMIC N/A | PREPARED BY Kenneth Rice | <p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p> | | | | | | | | | | | | | | | | | | |
| <p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p> | CHECKED BY Charles Reusing | | | | | | | | | | | | | | | | | | | |
| | APPROVED BY Michael A. Frye | <p align="center">MICROCIRCUIT, MEMORY, DIGITAL, CMOS EE PROGRAMMABLE READ ONLY MEMORY 256 X 16, MONOLITHIC SILICON</p> | | | | | | | | | | | | | | | | | | |
| | DRAWING APPROVAL DATE 91-08-16 | | | | | | | | | | | | | | | | | | | |
| | REVISION LEVEL A | | <table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-91549</td> </tr> </table> | SIZE A | CAGE CODE 67268 | 5962-91549 | | | | | | | | | | | | | | |
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| | | SHEET | 1 OF 19 | | | | | | | | | | | | | | | | | |

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| <u>Device type</u> | <u>Generic number</u> | <u>Circuit function</u> |
|--------------------|-----------------------|---|
| 01 | 93CS66 | 4096-Bit serial electrically erasable programmable memory |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| <u>Device class</u> | <u>Device requirements documentation</u> |
|---------------------|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| <u>Outline letter</u> | <u>Descriptive designator</u> | <u>Terminals</u> | <u>Package style</u> |
|-----------------------|-------------------------------|------------------|----------------------|
| P | GDIP1-T8 or CDIP2-T8 | 8 | Dual-in-line package |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

| | |
|--|---------------------------------------|
| All input or output voltages with respect to GND | -0.3 V dc to +6.5 V |
| Storage temperature range | -65°C to +150°C |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Junction temperature (T _J) 2/ | +150°C |
| Thermal resistance, junction-to-case (θ _{JC})..... | See MIL-STD-1835 |
| Thermal resistance, junction-to-ambient (θ _{JA}) | +200°C/W |
| Power dissipation (P _D) | 80 mW |
| Endurance | 10,000 program/erase cycles (minimum) |
| Data retention | 10 years (minimum) |

1.4 Recommended operating conditions.

| | |
|---|---------------------------------------|
| Positive power supply | +4.5 V to +5.5 V |
| Ambient operating temperature range (T _A) | -55°C to +125°C |
| Supply voltage (V _{SS}) | 0.0 V dc |
| High level input voltage range (V _{IH}) | 2.0 V dc to V _{CC} +1.0 V dc |
| Low level input voltage range (V _{IL})..... | -0.1 V dc to 0.8 V dc |
| Case operating temperature range (T _C)..... | -55°C to +125°C |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
 2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Instruction set. The instruction set shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number xxx (see MIL-PRF-38535, appendix A).

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3.11 Processing of EEPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Conditions of the supplied devices. Devices will be supplied in cleared state (Logic "0's"). No provision will be made for supplying written devices.

3.11.2 Read-write procedures. Correct red-write procedures shall be as specified 4.6.3.

3.11.3 Verification of state of EEPROMs. When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

3.11.4 Power supply sequence of EEPROMs. In order to reduce the probability of inadvertent writes, the following power supply sequences shall be observed:

- a. A logic low state shall be applied to \overline{CS} at the same time or before the application of V_{CC} .
- b. A logic low state shall be applied to \overline{CS} at the same time or before the removal of V_{CC} .

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TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---------------------------------------|------------------|---|----------------------|----------------|--------|-----------------------|------|
| | | | | | Min | Max | |
| Supply current active CMOS level | I _{CC1} | V _{CC} = 5.5 V, V _{SK} = 0, f _{SK} = .5 MHz, V _{CS} = 5 V, V _I = 0 or 5 V | 1, 2, 3 | 01 | | 2 | mA |
| Supply current active TTL level | I _{CC2} | V _{CC} = 5.5 V, V _{SK} = .8 to 2 V f _{SK} = .5 MHz, V _{CS} = V _{IH} V _I = V _{IH/L} | 1, 2, 3 | 01 | | 4 | |
| Supply current CMOS standby | I _{CC3} | V _{CC} = 5.5 V, V _{SK} = 0 to 5 V f _{SK} = 0 MHz, V _{CS} = 0 V, other V _I = V _{IH/L} | 1, 2, 3 | 01 | | 100 | μA |
| Logical "0" input leakage current | I _{IL} | V _{CC} = 5.5 V, V _I = 0 V | 1, 2, 3 | 01 | -10 | | |
| Logical "1" input leakage current | I _{IH} | V _{CC} = 5.5 V, V _I = 5.5 V | 1, 2, 3 | 01 | | 10 | |
| Logical "0" input leakage current | I _{OLZ} | V _{CC} = 5.5 V, DO TRI-STATE, V _{DO} = 0 V | 1, 2, 3 | 01 | -10 | | |
| Logical "1" output leakage current | I _{OHZ} | V _{CC} = 5.5 V, DO TRI-STATE, V _{DO} = 5.3 V | 1, 2, 3 | 01 | | 10 | |
| Logical "0" input voltage | V _{IL} | V _{CC} = 4.5 V | 1, 2, 3 | 01 | -.1 | .8 | V |
| Logical "1" input voltage | V _{IH} | V _{CC} = 5.5 V | 1, 2, 3 | 01 | 2 | V _{CC} +1 | |
| Logical "0" output voltage | V _{OL1} | V _{CC} = 4.5 V, I _{OL} = 1.8 mA | 1, 2, 3 | 01 | | .4 | |
| | V _{OL2} | V _{CC} = 4.5 V, I _{OL} = 10 μA | | | | .2 | |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|----------------------------|-------------------|---|---|----------------|--------|-------------------------|------|
| | | | | | Min | Max | |
| Logical "1" output voltage | V _{OH1} | V _{CC} = 4.5 V, I _{OH} = -400 μA | 1, 2, 3 | 01 | | 2.4 | V |
| | | V _{CC} = 4.5 V, I _{OH} = -10 μA | | | | V _{CC} -0.2 | |
| Input capacitance | C _I | V _{CC} = 5.5 V, V _{IN} = 2 V, f = 1 MHz <u>1/</u> | 4 | 01 | | 8 | pF |
| Output capacitance | C _O | V _{CC} = 5.5 V, V _O = 2 V, f = 1 MHz <u>1/</u> | 4 | 01 | | 10 | |
| AC Testing <u>2/</u> | | | | | | | |
| SK clock frequency | f _{SK} | V _{CC} = 4.5 V <u>3/</u> | 9, 10, 11 | 01 | 0 | 0.5 | MHz |
| SK high time | t _{SKH} | V _{CC} = 4.5 V <u>3/</u> | 9, 10, 11 | 01 | 500 | | ns |
| SK low time | t _{SKL} | V _{CC} = 4.5 V <u>3/</u> | 9, 10, 11 | 01 | 500 | | |
| CS low time | t _{CS} | V _{CC} = 4.5 V <u>4/</u> | 9, 10, 11 | 01 | 500 | | |
| CS setup time | t _{CSS} | V _{CC} = 4.5 V, Relative to SK rising See figure 3 | 9, 10, 11 | 01 | 100 | | |
| DI setup time | t _{DIS} | | 9, 10, 11 | 01 | 200 | | |
| PRE setup time | t _{PRES} | | 9, 10, 11 | 01 | 100 | | |
| PE setup time | t _{PES} | | 9, 10, 11 | 01 | 100 | | |
| CS hold time | t _{CSH} | | V _{CC} = 4.5 V Relative to SK falling | 9, 10, 11 | 01 | 0 | |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|-----------------------|-------------------|---|----------------------|-----------------|--------|------|------|
| | | | | | Min | Max | |
| DI hold time | t _{DIH} | V _{CC} = 4.5 V, Relative to SK rising See figure 3 | 9, 10, 11 | 01 | 200 | | ns |
| PE hold time | t _{PEH} | V _{CC} = 4.5 V, Relative to CS falling See figure 3 | 9, 10, 11 | 01 | 500 | | |
| PRE hold time | t _{PREH} | | 9, 10, 11 | 01 | 0 | | |
| Output delay to "1" | t _{PD1} | V _{CC} = 4.5 V, Relative to SK rising See figure 3 | 9, 10, 11 | 01 | | 1000 | |
| Output delay to "0" | t _{PDO} | | 9, 10, 11 | 01 | | 1000 | |
| CS to status valid | t _{SV} | | 9, 10, 11 | 01 | | 1000 | |
| CS to DO in tri-state | t _{DF} | V _{CC} = 5.5 V, Relative to CS falling See figure 4 | 9, 10, 11 | 01 | | 1000 | |
| Write cycle time | t _{WP} | | 9, 10, 11 | 01 | | 10 | ms |

- 1/ Tested initially and after any design or process changes which may affect this parameter, and therefore guaranteed to the limits specified in table I.
- 2/ Tested by application of specified timing signals and conditions.
Equivalent A.C. test conditions:
Output load: See figure 5.
Input rise and fall times ≤ 10 ns.
Input pulse levels: 0.4 and 2.4 V.
Timing measurement reference levels:
Inputs 1 V and 2 V.
Outputs 0.8 V and 2 V.
- 3/ The SK frequency specification is for a minimum 5K clock period of 2 us, therefore in a 5K clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 us.
- 4/ CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

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| | |
|-----------------|-----------------|
| Device type | 01 |
| Case outlines | P |
| Terminal number | Terminal symbol |
| 1 | CS |
| 2 | SK |
| 3 | DI |
| 4 | DO |
| 5 | GND |
| 6 | PE |
| 7 | PRE |
| 8 | V _{CC} |

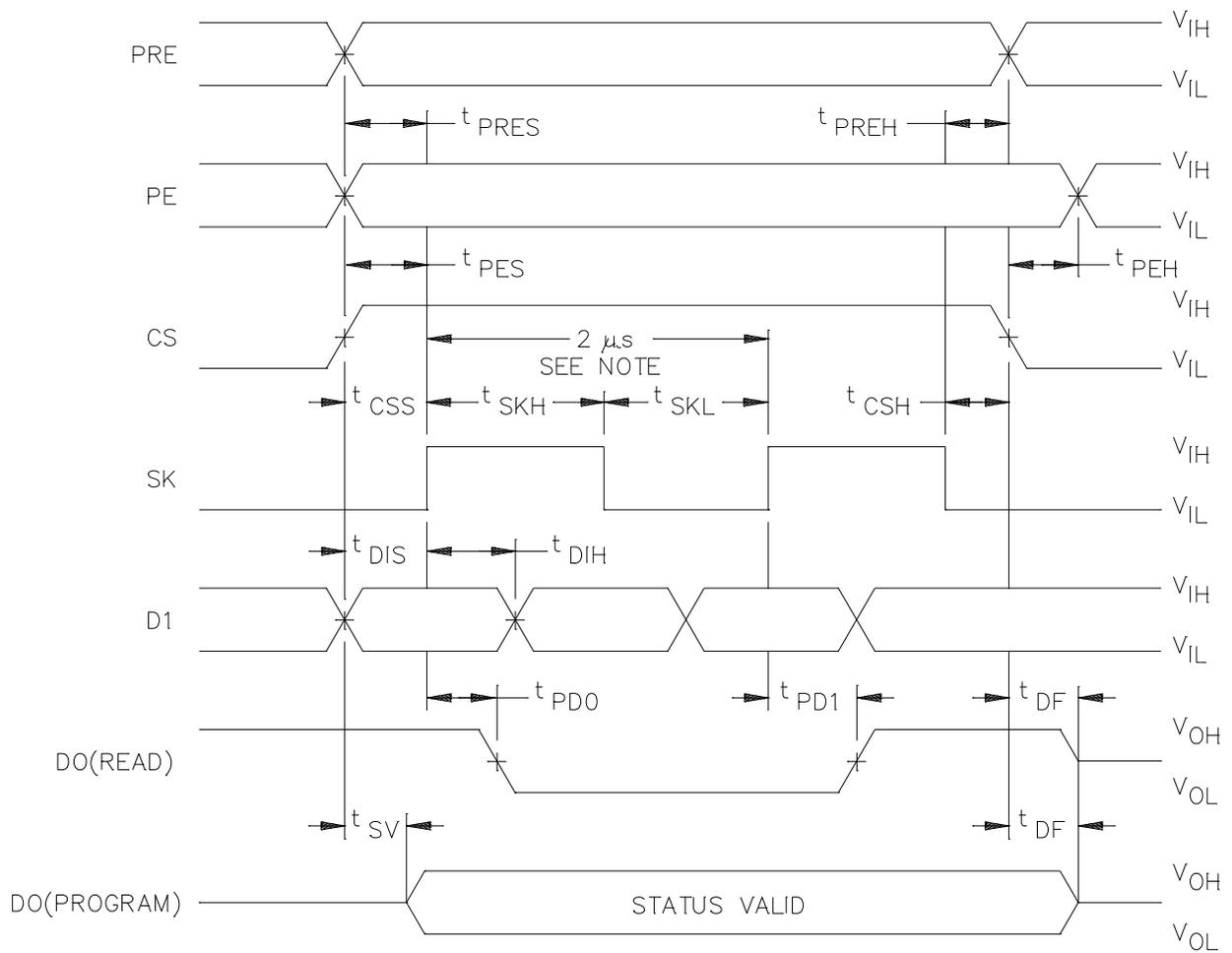
FIGURE 1. Terminal connections.

| Instruction | SB | Op Code | Address | Data | PRE | PE | Comments |
|-------------|----|---------|----------|--------|-----|----|---|
| READ | 1 | 10 | A7-A0 | | 0 | X | Reads data stored in memory, starting at specified address. |
| WEN | 1 | 00 | 11XXXXXX | | 0 | 1 | Write enable must precede all programming modes |
| WRITE | 1 | 01 | A7-A0 | D15-D0 | 0 | 1 | Write register if address is unprotected. |
| WRALL | 1 | 00 | 01XXXXXX | D15-D0 | 0 | 1 | Writes all registers. Valid only when Protect Register is cleared. |
| WDS | 1 | 00 | 00XXXXXX | | 0 | X | Disables all programming instructions. |
| PRREAD | 1 | 10 | XXXXXXXX | | 1 | X | Reads address stored in Protect Register. |
| PREN | 1 | 00 | 11XXXXXX | | 1 | 1 | Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions. |
| PRCLEAR | 1 | 11 | 11111111 | | 1 | 1 | Clears the "protect register" so that no registers are protected from WRITE |
| PRWRITE | 1 | 01 | A7-A0 | | 1 | 1 | Programs address into Protect Register. Thereafter, memory addresses \geq the address in Protect Register are protected from WRITE. |
| PRDS | 1 | 00 | 00000000 | | 1 | 1 | Only time only instruction after which the address in the Protect Register cannot be altered. |

FIGURE 2. Instruction set

| | | | |
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SYNCHRONOUS DATA TIMING



NOTE: This is the minimum SK period.

FIGURE 3. Timing waveform.

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SIZE
A

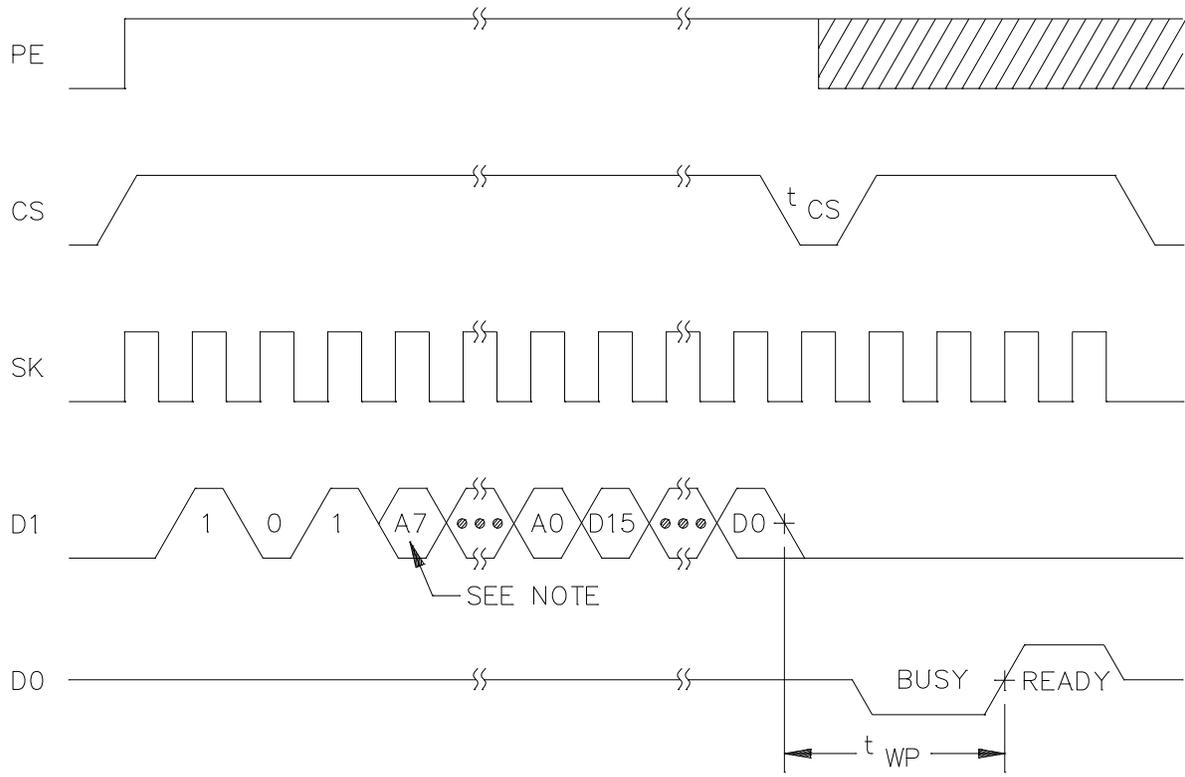
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SHEET

10

WRITE: PRE=0
(SEE NOTE)

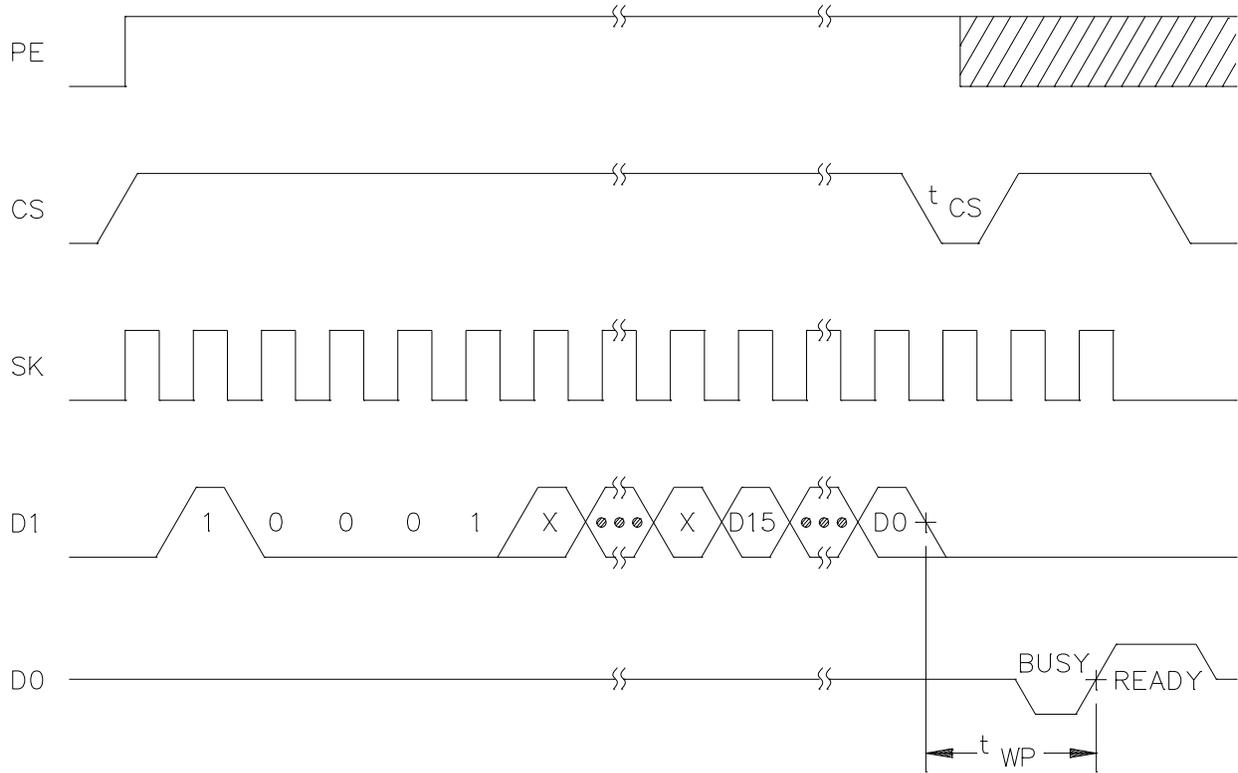


NOTE: Address bit A7 becomes a "don't care" for NMC93CS56.

FIGURE 4. Timing diagrams.

| | | | |
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WRALL: PRE=0
(SEE NOTE)

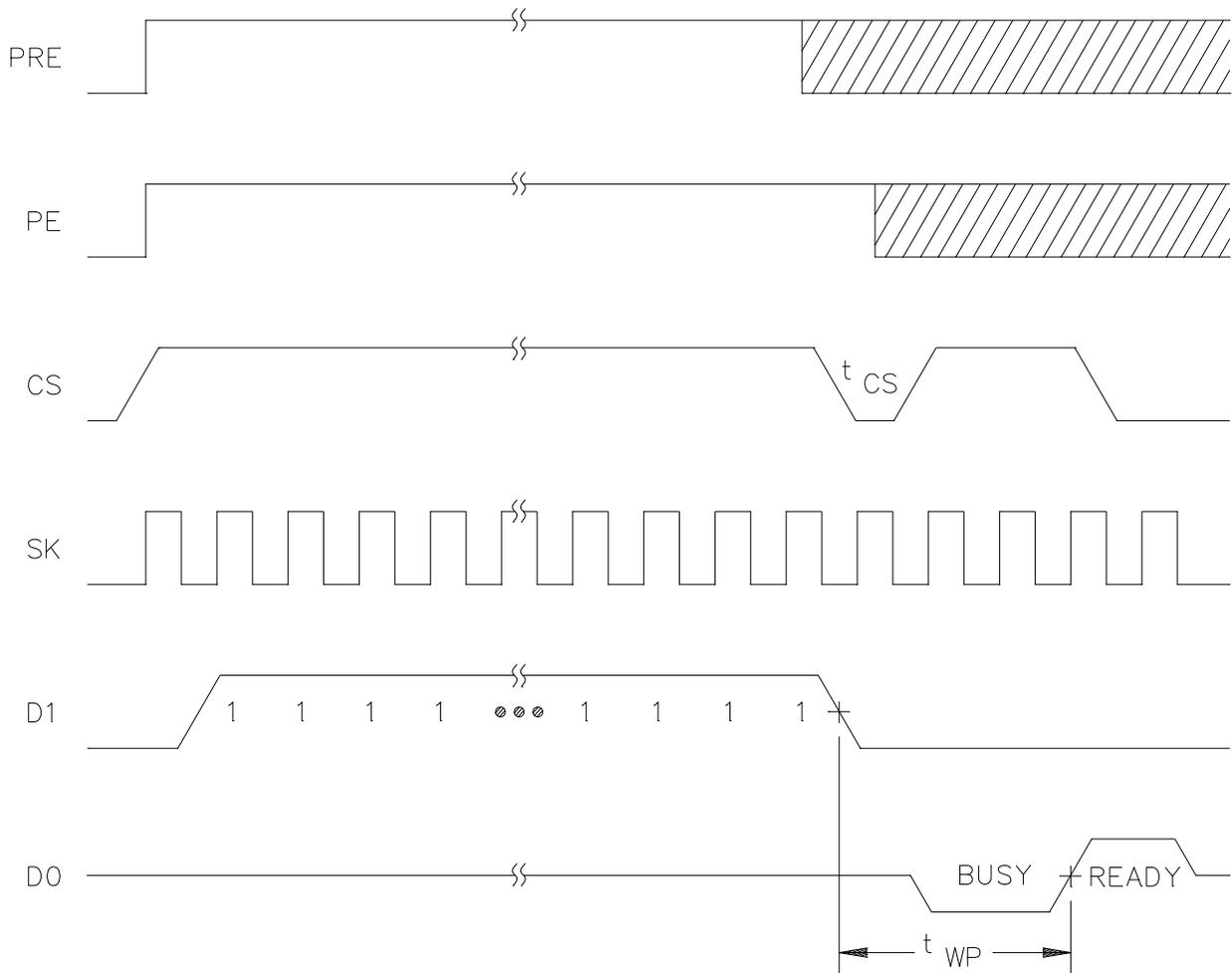


NOTE: Protect Register must be cleared.

FIGURE 4. Timing diagrams – Continued.

| | | | |
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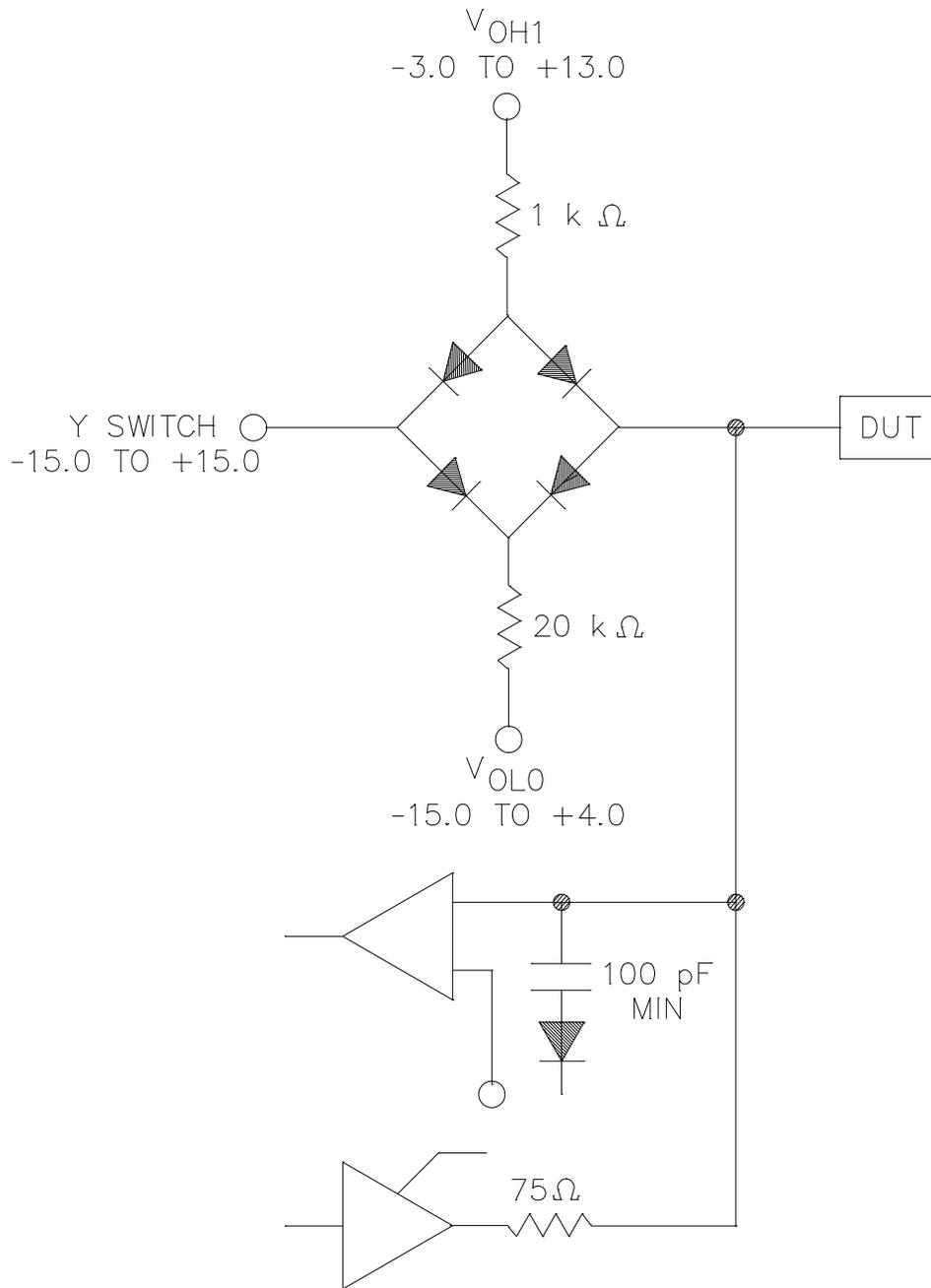
PRECLEAR: (SEE NOTE)



NOTE: A PREN cycle must immediately precede a PRECLEAR cycle.

FIGURE 4. Timing diagrams – Continued.

| | | | |
|--|------------------|----------------|-------------------|
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NOTE: V_{OH1} and V_{OL0} will be adjusted to meet load conditions of table I.

FIGURE 5. Switching load circuit.

| | | | |
|--|------------------|----------------|-------------------|
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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|------------------------------------|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | | 1, 7, 9 or 2, 8A, 10 | 1, 7, 9 or 1, 2, 8A, 10 |
| Static burn-in I & II method 1015 | Not required | Not required | Required |
| Same as line 1 | | | 1*, 7* Δ |
| Dynamic burn-in (method 1015) | Required | Required | Required |
| Same as line 1 | | | 1*, 7* Δ |
| Final electrical parameters (see 4.2) | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 7/ | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 7/ | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 8/ |
| Group A test requirements (see 4.4) | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 2, 3, 7, 8A, 8B | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ 9/ | |
| Group D end-point electrical parameters (see 4.4) | 2, 3, 7, 8A, 8B | 2, 3, 7, 8A, 8B | 2, 3, 7, 8A, 8B |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9, 8A, 8B | 1, 7, 9, 8A, 8B | 1, 7, 9, 8A, 8B |

- 1/ Blank spaces indicate tests are not applicable.
 2/ Any or all subgroups may be combined when using high-speed testers.
 3/ Subgroups 7 and 8 functional tests shall verify the truth table.
 4/ * indicates PDA applies to subgroup 1 and 7.
 5/ see 4.4.1e.
 6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see table IIB).
 7/ PDA applies to subgroup 1.
 8/ PDA applies to subgroups 1 and 7.
 9/ Delta limits required for initial qualification and after any design or process changes.

TABLE IIB. Delta limits at +25°C.

| Test 1/ | Device types |
|-------------------------------------|------------------------------------|
| | All |
| I _{CC3} standby | ±10% of specified value in table I |
| I _{OHZ} , I _{OLZ} | ±10% of specified value in table I |

- 1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device classes Q and V measurements for device classes Q and. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB.

4.6 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.6.1 Voltages and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6.2 Life test, burn-in, cool down and electrical test procedure. When devices are measured at $+25^{\circ}\text{C}$ following application of the steady state life or burn-in test condition, all devices shall be cooled to $+35^{\circ}\text{C}$ or within 10°C of the power stable condition prior to removal of bias voltages/signals. Any electrical tests required shall first be performed at -55°C or $+25^{\circ}\text{C}$ prior to any required tests at $+125^{\circ}\text{C}$.

4.6.3 Writing procedure.

4.6.3.1 Read (READ). The Read (READ) instructions outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit logical 0 precedes the 16-bit output string. Output data changes are initiated by a low to high transition of the SK clock. In the NOVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressing in this mode and a continuous string of data is obtained.

4.6.3.2 Write Enable (WNE). When VCC is applied to the part, it powers up in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or VCC is removed from the part.

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4.6.3.3 Write (WRITE). The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The PE pin MUST be held "high" while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (CS). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

4.6.3.4 Write All (WRALL). The Write All (WRALL) instruction is valid only when the "protect register" has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin MUST be held "high" while loading the WRALL instruction, however, after loading the WIRTE instruction the PE pin becomes a "don't care". As in the WRITE mode the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

4.6.3.5 Write Disable (WDS). To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

4.6.3.6 Protect Register Read (PRREAD). The Protect Register Read (PRREAD) instruction outputs the address stored in the "protect register" on the DO pin. The PRE pin MUST be held "high" while loading the instruction. Following the PRREAD instruction the 8-bit address stored in the Protect Register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 8-bit address string.

4.6.3.7 Protect Register Enable (PREN). The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins MUST be held "high" while loading the instruction. Note that a PREN instruction must IMMEDIATELY precede a PRCLEAR, PRWRITE, or PRDS instruction.

4.6.3.8 Protect Register Clear (PRCLEAR). The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables ALL registers for the WRITE and WRALL instruction. The PRE and PE pins MUST be held "high" while loading the instruction; however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must IMMEDIATELY precede a PRCLEAR instruction.

4.6.3.9 Protect Register Write (PRWRITE). The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register are protected from the WIRTE operation. Note htat before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins MUST be held "high" while loading the instruction, however, after loading the PRWRITE instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must IMMEDIATELY precede a PRWRITE instruction.

4.6.3.10 Protect Register Disable (PRDS). The Protect Register Disable (PRDS) instruction is a ONE TIME ONLY instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become PERMANENTLY protected against data changes. As in the PRWRITE instruction the PRE and PE pins MUST be held "high" while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care". Note that a PREN instruction must IMMEDIATELY precede a PRDS instruction.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0547.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-07-27

Approved sources of supply for SMD 5962-91549 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

| Standard microcircuit drawing PIN <u>1/</u> | Vendor CAGE number <u>3/</u> | Vendor similar PIN <u>2/</u> |
|---|------------------------------|------------------------------|
| 5962-9154901MPA | <u>3/</u> | NM93CS66J/883 |

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply. The last known sources are listed below.

Vendor CAGE
number

27014

Vendor name
and address

National Semiconductor
2900 Semiconductor Drive
PO Box 58090
Santa Clara, CA 95052-8090

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.