REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add notes to figure 5, switching waveforms and test circuit. Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. – LTG	06-02-23	Thomas M. Hess
B	Update test condition of high and low level output voltage (V_{OH} and V_{OL}) to table I. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	12-07-25	Thomas M. Hess
C	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	17-02-23	Thomas M. Hess
D	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - JWC	23-05-31	Muhammad Akbar

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV																						
SHEET																						
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D								
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14								

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
Marcia B. Kelleher

CHECKED BY
Thomas J. Riccuiti

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
91-11-26

REVISION LEVEL
D

SIZE
A

CAGE CODE
67268

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL, HIGH SPEED CMOS, PRESETTABLE SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER, TTL COMPATIBLE INPUTS,MONOLITHIC SILICON

AMSC N/A

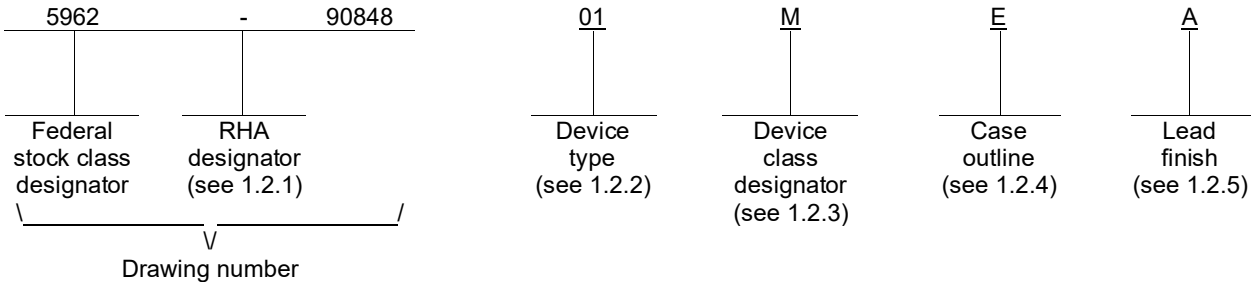
5962-90848

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HCT193	Presettable synchronous 4-bit binary up/down counter, asynchronous reset, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current	±20 mA
DC output current (per pin)	±25 mA
DC V_{CC} or GND current (per pin)	±50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW 4/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time (t_r, t_f):	
V_{CC} = 4.5 V, 5.5 V	0 to 500 ns
Minimum setup time, Pn to $\overline{PL}$ (ts):	
T_C = +25°C, VCC = 4.5 V	15ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V	22 ns
Minimum CPU, CPD pulse width (t_{w1}):	
T_C = +25°C, V_{CC} = 4.5 V	23 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V	35 ns
Minimum $\overline{PL}$ pulse width (t_{w2}):	
T_C = +25°C, V_{CC} = 4.5 V	16 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V	24 ns
Minimum MR pulse width (t_{w3}):	
T_C = +25°C, V_{CC} = 4.5 V	20 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V	30 ns
Minimum hold time, Pn to $\overline{PL}$ (t_{h1}):	
T_C = +25°C, V_{CC} = 4.5 V	0 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V	0 ns
Minimum hold time, CPD to CPU, CPU to CPD (t_{h2}):	
T_C = +25°C, V_{CC} = 4.5 V	16 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V	24 ns
Minimum recovery time, $\overline{PL}$ to CPU, $\overline{PL}$ to CPD (t_{REC1}):	
T_C = +25°C, V_{CC} = 4.5 V	15 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V	22 ns
Minimum recovery time, MR to CPU, MR to CPD (t_{REC2}):	
T_C = +25°C, V_{CC} = 4.5 V	5 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V	5 ns
Maximum CPU, CPD frequency (f_{MAX}):	
T_C = +25°C, V_{CC} = 4.5 V	22 MHz
T_C = -55°C to +125°C, V_{CC} = 4.5 V	15 MHz

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltages are referenced to ground.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ For T_C = +100°C to +125°C, derate linearly at 8 mW/°C to 300 mW.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD7 - Standard for Description of 54/74HCXXXXX and 54/74HCTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at https://www.jedec.org).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Counting sequence diagram. The counting sequence diagram shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 40 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V $V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V	I_{OH} = -20 µA	1, 2, 3	All	4.4		V
			I_{OH} = -4.0 mA			3.7		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V $V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V	I_{OL} = +20 µA	1, 2, 3	All		0.1	V
			I_{OL} = +4.0 mA				0.4	
High level input voltage	V_{IH}	V_{CC} = 4.5 V 2/		1, 2, 3	All	2.0		V
Low level input voltage	V_{IL}	V_{CC} = 4.5 V 2/		1, 2, 3	All		0.8	V
Quiescent supply current	I_{CC}	V_{CC} = 5.5 V, $V_{IN} = V_{CC}$ or GND I_{OUT} = 0.0 A		1, 2, 3	All		160	µA
Input leakage current	I_{IN}	V_{CC} = 5.5 V, $V_{IN} = V_{CC}$ or GND		1, 2, 3	All		±1.0	µA
Additional quiescent supply current, TTL inputs	ΔI_{CC}	Any one input V_{IN} = 2.4 V or 0.5 V Other inputs $V_{IN} = V_{CC}$ or GND V_{CC} = 5.5 V		1, 2, 3	All		3.0	mA
Input capacitance	C_{IN}	V_{IN} = 0 V, see 4.4.1c		4	All		10	pF
Power dissipation capacitance 3/	C_{PD}	See 4.4.1c		4	All		63	pF
Functional tests		See 4.4.1b		7, 8	All			
Propagation delay time, CPU to $\overline{TCU}$	t_{PHL1}, t_{PLH1}	V_{CC} = 4.5 V C_L = 50 pF See figure 5		9	All		27	ns
				10, 11			41	
Propagation delay time, CPD to $\overline{TCD}$	t_{PHL2}, t_{PLH2}			9	All		27	ns
				10, 11			41	
Propagation delay time, CPU to Qn	t_{PHL3}, t_{PLH3}			9	All		40	ns
				10, 11			60	
Propagation delay time, CPD to Qn	t_{PHL4}, t_{PLH4}			9	All		40	ns
				10, 11			60	
Propagation delay time, $\overline{PL}$ to Qn	t_{PHL5}, t_{PLH5}			9	All		47	ns
				10, 11			71	
Propagation delay time, MR to Qn	t_{PHL6}			9	All		43	ns
				10, 11			65	
Transition time 4/	t_{THL}, t_{TLH}			9	All		15	ns
				10, 11			22	

1/ For a power supply of 5.0 V ±10%, the worst case output voltages (V_{OH} and V_{OL}) occur for HCT at V_{CC} = 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst cases V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively.

2/ Tests are not required if applied as a forcing function for V_{OH} or V_{OL} tests.

3/ Power dissipation capacitance (C_{PD}) determines the dynamic power consumption (P_D) and the dynamic current consumption (I_S):
P_D (total) = $(C_{PD} + C_L) V_{CC}^2 f + (V_{CC} \times I_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$
$I_S = (C_{PD} + C_L) V_{CC} f + I_{CC} + (n \times d \times \Delta I_{CC})$
f is input switching frequency; n is number of inputs switching; d is duty cycle; C_L is load capacitance on each output.

4/ This parameter, if not tested, shall be guaranteed to the limits specified in table I.

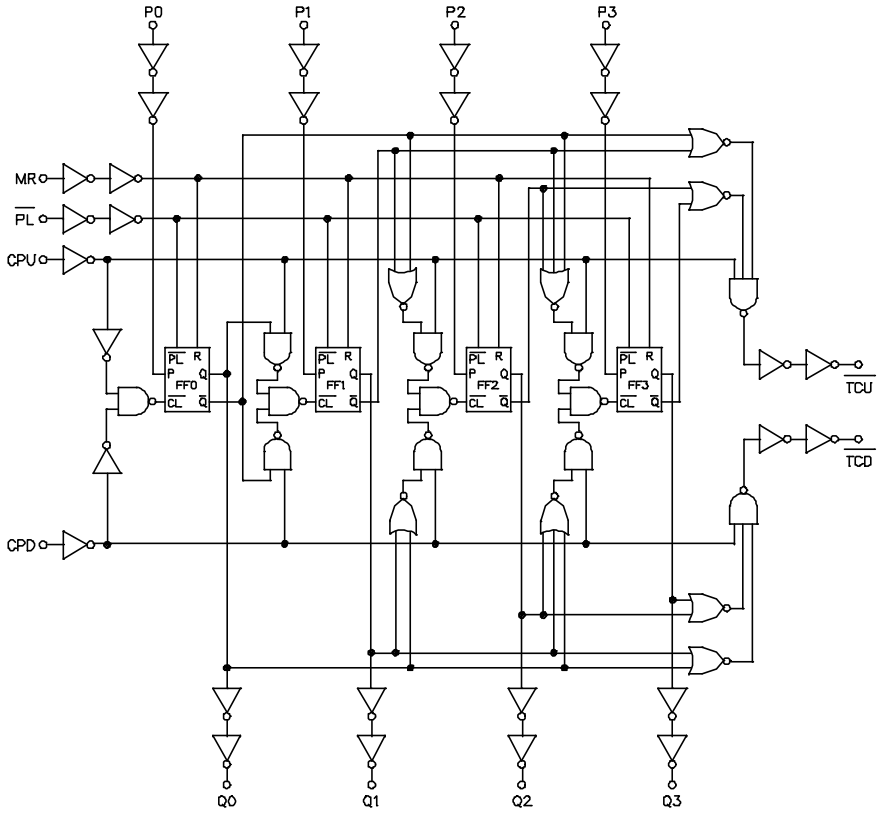
Device type	All
Case outline	E
Terminal number	Terminal symbol
1	P1
2	Q1
3	Q0
4	CPD
5	CPU
6	Q2
7	Q3
8	GND
9	P3
10	P2
11	$\overline{PL}$
12	$\overline{TCU}$
13	$\overline{TCD}$
14	MR
15	P0
16	V_{CC}

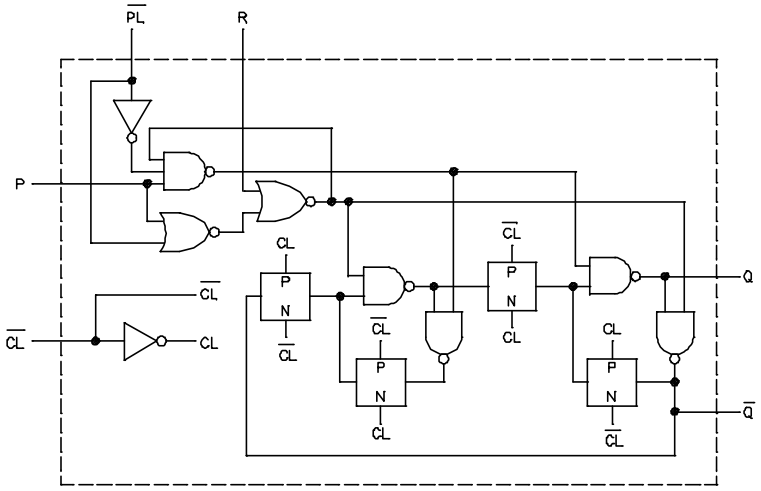
FIGURE 1. Terminal connections.

CPU	CPD	MR	$\overline{PL}$	Function
↑	H	L	H	Count up
H	↑	L	H	Count down
X	X	H	X	Reset all outputs
X	X	L	L	Load preset inputs P0 – P3

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low-to-high clock transition

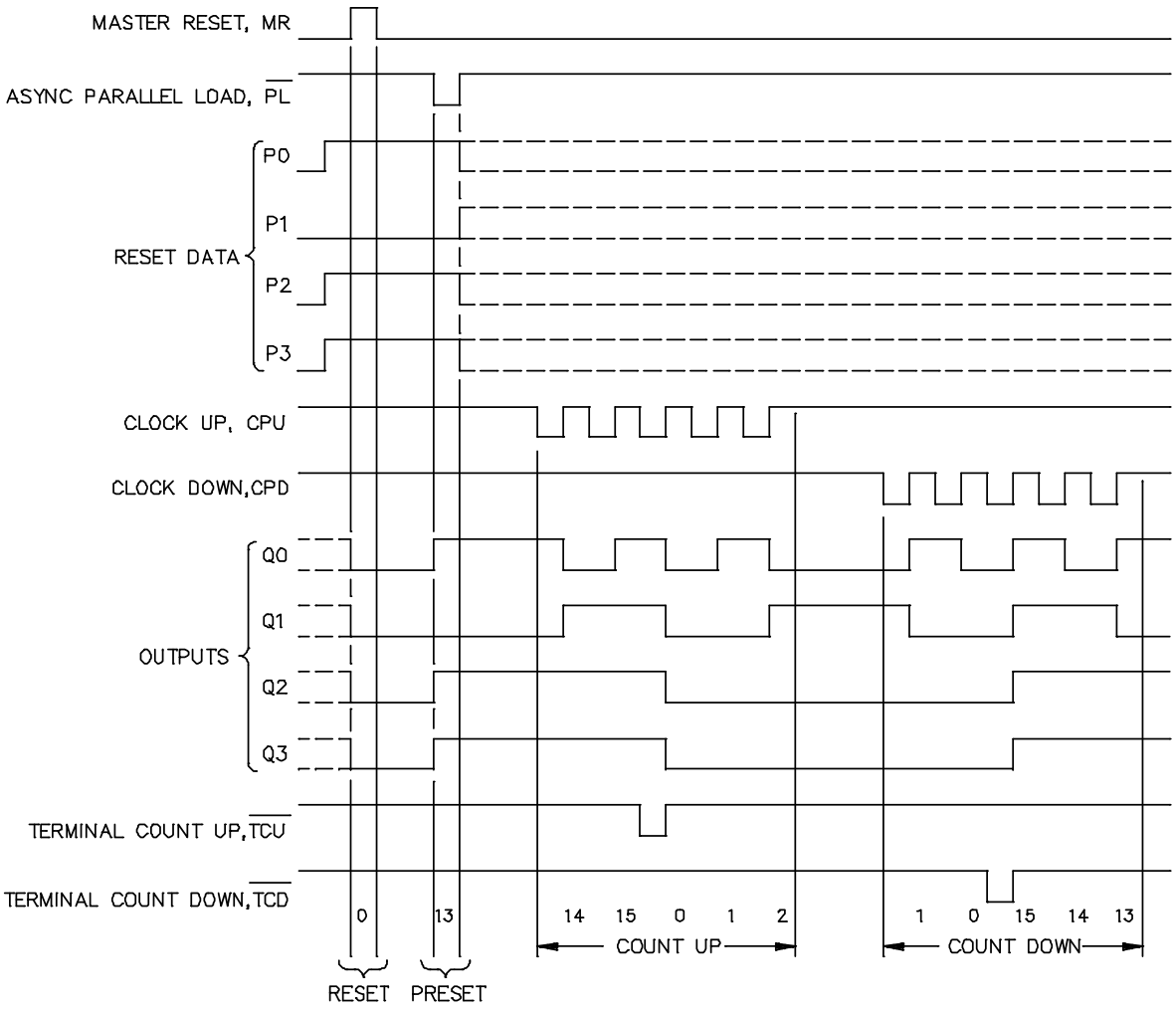
FIGURE 2. Truth table.





LOGIC DIAGRAM OF FLIP-FLOPS

FIGURE 3. Logic diagram.



Sequences:
(1) Reset outputs Q0 through Q3 to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, terminal count up, zero, one, and two.
(4) Count down to one, zero, terminal count down, fifteen, fourteen, and thirteen.

NOTES:
1. Master reset overrides load data and clock inputs.
2. When counting up, clock-down input must be high; when counting down, clock-up input must be high.
3. Terminal count up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count.
4. The terminal count down (borrow) in the count down mode likewise goes low half a clock period before the maximum count and returns to high at the maximum count.

FIGURE 4. Counting sequence diagram.

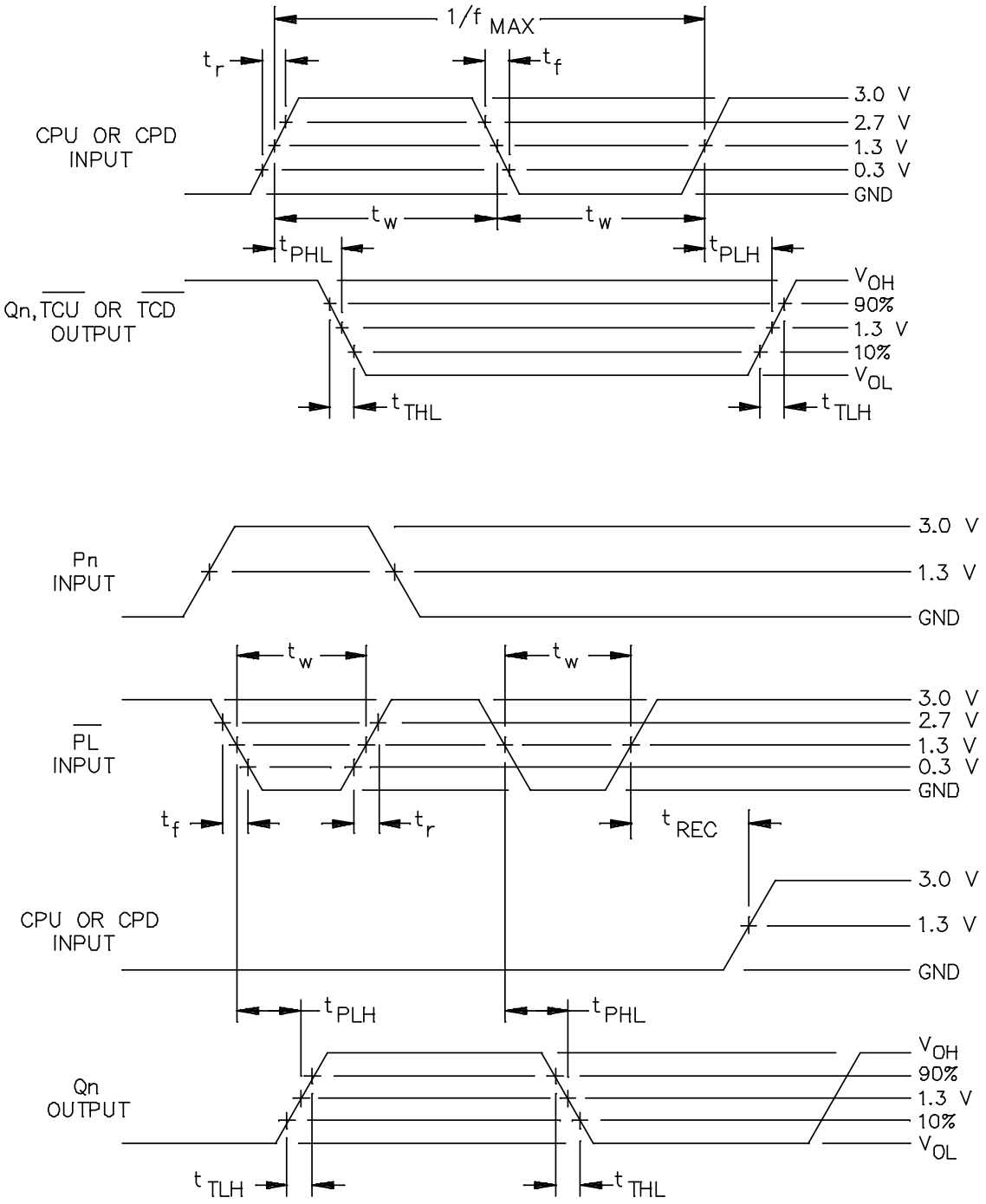
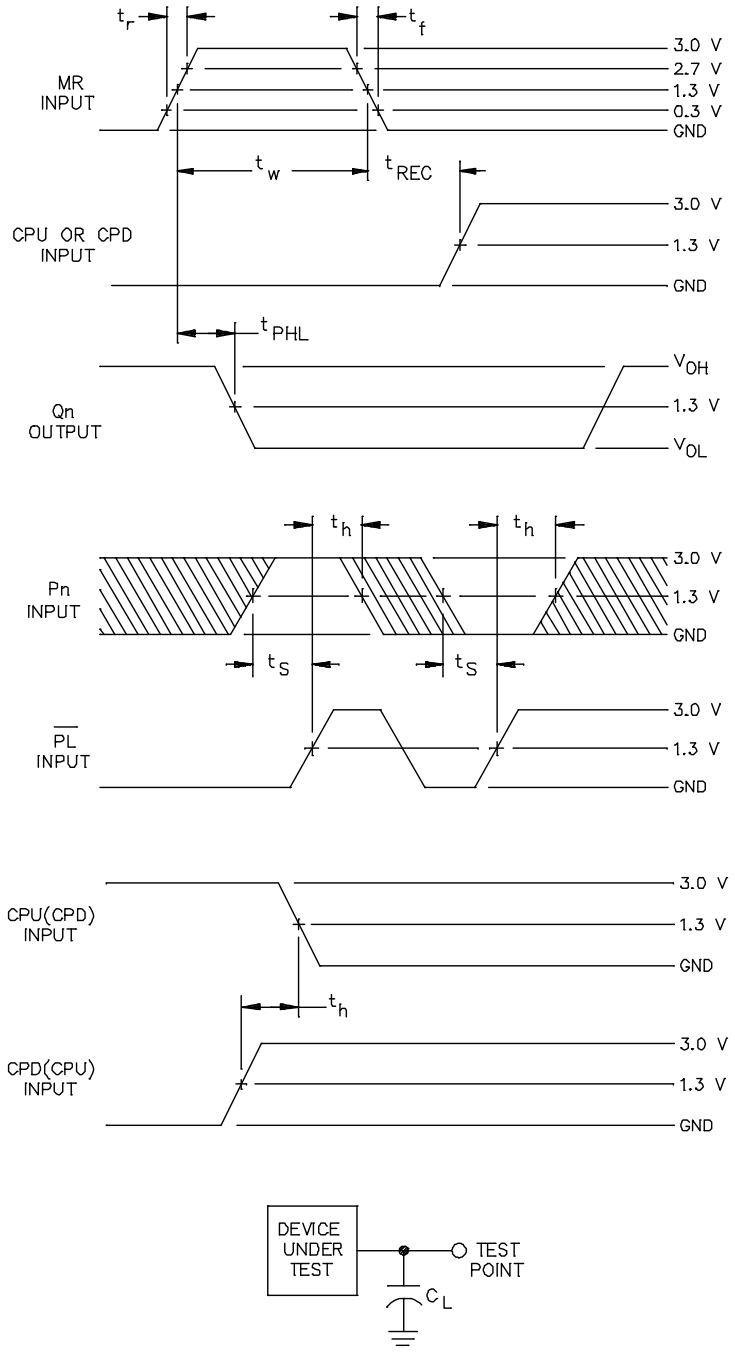


FIGURE 5. Switching waveforms and test circuit.



NOTES:
1. C_L = 50 pF minimum (includes test jig and probe capacitance).
2. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 1 MHz; Z_O = 50Ω; t_r = 6.0 ns; t_f = 6.0 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
3. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.
   (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
   (2) TA = +125°C, minimum.
b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
b. Interim and final electrical test parameters shall be as specified in table II herein.
c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.
b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table as specified on figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
c. Subgroup 4 (C_{IN} and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on 5 devices with zero failures.
d. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-05-31

Approved sources of supply for SMD 5962-90848 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply a https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9084801MEA	01295	CD54HCT193F3A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243