

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R010-96. --ltg	95-12-04	Monica L. Poelking
B	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	04-09-07	Raymond Monnin
C	Update drawing as part of 5 year review. --jt	12-10-15	C. SAFFLE

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
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REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13						
PMIC N/A	PREPARED BY Larry T. Gauder				<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p> <p>MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY, TTL, 10-BIT BUS INTERFACE FLIP-FLOPS WITH NON-INVERTING AND INVERTING INPUTS, MONOLITHIC SILICON</p>															
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY Tim H. Noh																			
	APPROVED BY William K. Heckman																			
	DRAWING APPROVAL DATE 91-02-06																			
AMSC N/A	REVISION LEVEL C				SIZE A	CAGE CODE 67268		5962-90780												
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1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage	-1.2 V dc at -18 mA to +7.0 V dc
Voltage applied to a disabled 3-state output	+5.5 V dc
Storage temperature range	-65°C to +150°C
Continuous power dissipation (P_D)	621.5 mW 2/
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH}):	2.0 V dc
Maximum low level input voltage (V_{IL}):	
01, 02, 04	0.8 V dc
03	0.7 V dc
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+32 mA
Case operating temperature range (T_C)	-55°C to +125°C
Minimum setup time, (t_s) before CLK \uparrow :	
from data, 01, 02	7 ns
from \overline{CLR} inactive, 03, 04	8 ns
from data, 03, 04	7 ns
from CLKEN high or low:	
03	10.5 ns
04	7 ns
Minimum hold time, (t_h) CLKEN or data, after CLK \uparrow	0 ns
Minimum pulse duration, (t_w):	
CLK high or low:	
01, 02, 04	9 ns
03	9.5 ns
\overline{CLR} low:	
03	7 ns
04	5 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
 2/ Continuous power dissipation is defined as $V_{CC} \times I_{CC}$, and must withstand the added P_D due to short circuit test e.g., I_{OS}

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DEPARTMENT OF DEFENSE STANDARDS

- MIL-STD-883 - Test Method Standard Microcircuits.
- MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

- MIL-HDBK-103 - List of Standard Microcircuit Drawings.
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

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3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 10 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V, V _{IN} = 2.0 V, V _{IL} = Max 2/	I _{OH} = -2 mA/	1, 2, 3	All	2.5		V
			I _{OH} = -15 mA			2.4		
			I _{OH} = -24 mA			2.0		
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, V _{IN} = 2.0 V, V _{IL} = Max 2/	I _{OL} = 32 mA	1, 2, 3	All		0.5	V
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V	I _{IN} = -18 mA	1, 2, 3	All		-1.2	V
High level input current	I _{IH1}	V _{CC} = 5.5 V	V _{IN} = 7.0 V	1, 2, 3	All		100	μA
	I _{IH2}		V _{IN} = 2.7 V			20		
Low level input current	I _{IL}	V _{CC} = 5.5 V	V _{IN} = 0.4 V	1, 2, 3	All		-0.5	mA
Output current	I _O	V _{CC} = 5.5 V 3/	V _{OUT} = 2.25 V	1, 2, 3	All	-30	-112	mA
Supply current	I _{CCH}	V _{CC} = 5.5 V	Outputs high	1, 2, 3	01, 02		88	mA
						Outputs low	03, 04	
	Outputs disabled		01, 02				109	
			03, 04			90		
			01, 02			113		
			03, 04			95		
I _{CCL}	I _{CCZ}	V _{CC} = 5.5 V	Outputs disabled	1, 2, 3	All		50	μA
							-50	
Off-state output leakage current	I _{OZH}	V _{CC} = 5.5 V	V _{OUT} = 2.4 V	1, 2, 3	All		50	μA
	I _{OZL}		V _{OUT} = 0.4 V				-50	
Functional tests		See 4.3.1c V _{CC} = 4.5 and 5.5 V		7, 8	All			

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C ^{1/} unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, CLK to any Q	t _{PLH1}	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = R ₂ = 500Ω, See figure 3 ^{4/}	9, 10, 11	All	3.5	9	ns
	t _{PHL1}			01	3.5	14	ns
				02, 04	3.5	11.5	
				03	3.5	13.5	
Propagation delay time, $\overline{\text{CLR}}$ to any Q	t _{PHL2}		9, 10, 11	03	3.5	16.5	ns
				04	3.5	14	
Output enable time, $\overline{\text{OC}}$ to any Q	t _{PZH}		9, 10, 11	All	4	12	ns
	t _{PZL}			All	4	13	ns
Output disable time, $\overline{\text{OC}}$ to any Q	t _{PHZ}	9, 10, 11	01, 03	1	10	ns	
			02, 04	2	10		
	t _{PLZ}		All	2	10	ns	

- ^{1/} Unused inputs that do not directly control the pin under test must be put at ≥ 2.5 V or ≤ 0.4 V. No unused inputs shall exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.
- ^{2/} All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper state, the test must be performed with each input being selected as the V_{IL} maximum or V_{IH} minimum input.
- ^{3/} The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and duration of the test condition shall not exceed one second.
- ^{4/} Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V.

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Device type	01		02		03		04	
Case outlines	K, L	3	K, L	3	K, L	3	K, L	3
Terminal number	Terminal symbol		Terminal symbol		Terminal symbol		Terminal symbol	
1	\overline{OC}	NC	\overline{OC}	NC	$\overline{OC} 1$	NC	$\overline{OC} 1$	NC
2	1D	\overline{OC}	1 \overline{D}	\overline{OC}	$\overline{OC} 2$	$\overline{OC} 1$	$\overline{OC} 2$	$\overline{OC} 1$
3	2D	1D	2 \overline{D}	1 \overline{D}	1D	$\overline{OC} 2$	1 \overline{D}	$\overline{OC} 2$
4	3D	2D	3 \overline{D}	2 \overline{D}	2D	1 \overline{D}	2 \overline{D}	1 \overline{D}
5	4D	3D	4 \overline{D}	3 \overline{D}	3D	2 \overline{D}	3 \overline{D}	2 \overline{D}
6	5D	4D	5 \overline{D}	4 \overline{D}	4D	3 \overline{D}	4 \overline{D}	3 \overline{D}
7	6D	5D	6 \overline{D}	5 \overline{D}	5D	4 \overline{D}	5 \overline{D}	4 \overline{D}
8	7D	NC	7 \overline{D}	NC	6D	5 \overline{D}	6 \overline{D}	NC
9	8D	6D	8 \overline{D}	6 \overline{D}	7D	NC	7 \overline{D}	5 \overline{D}
10	9D	7D	9 \overline{D}	7 \overline{D}	8D	6 \overline{D}	8 \overline{D}	6 \overline{D}
11	10D	8D	10 \overline{D}	8 \overline{D}	\overline{CLR}	7 \overline{D}	\overline{CLR}	7 \overline{D}
12	GND	9D	GND	9 \overline{D}	GND	8 \overline{D}	GND	8 \overline{D}
13	CLK	10D	CLK	10 \overline{D}	CLK	\overline{CLR}	CLK	\overline{CLR}
14	10Q	GND	10Q	GND	\overline{CLKEN}	GND	\overline{CLKEN}	GND
15	9Q	NC	9Q	NC	8Q	NC	8Q	NC
16	8Q	CLK	8Q	CLK	7Q	\overline{CLK}	7Q	\overline{CLK}
17	7Q	10Q	7Q	10Q	6Q	\overline{CLKEN}	6Q	\overline{CLKEN}
18	6Q	9Q	6Q	9Q	5Q	8Q	5Q	8Q
19	5Q	8Q	5Q	8Q	4Q	7Q	4Q	7Q
20	4Q	7Q	4Q	7Q	3Q	6Q	3Q	6Q
21	3Q	6Q	3Q	6Q	2Q	5Q	2Q	5Q
22	2Q	NC	2Q	NC	1Q	NC	1Q	NC
23	1Q	5Q	1Q	5Q	$\overline{OC} 3$	4Q	$\overline{OC} 3$	4Q
24	V _{CC}	4Q	V _{CC}	4Q	V _{CC}	3Q	V _{CC}	3Q
25	---	3Q	---	3Q	---	2Q	---	2Q
26	---	2Q	---	2Q	---	1Q	---	1Q
27	---	1Q	---	1Q	---	$\overline{OC} 3$	---	$\overline{OC} 3$
28	---	V _{CC}	---	V _{CC}	---	V _{CC}	---	V _{CC}

NC = No connection

FIGURE 1. Terminal connections.

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Inputs			Output	
\overline{OC}	CLK	D	Device 01	Device 02
			Q	Q
L	↑	H	H	L
L	↑	L	L	H
L	L	X	Q ₀	Q ₀
H	X	X	Z	Z

Inputs					Output	
\overline{OC} 1/	\overline{CLR}	\overline{CLKEN}	CLK	D	Device 03	Device 04
					Q	Q
L	L	X	X	X	L	L
L	H	L	↑	H	H	L
L	H	L	↑	L	L	H
L	H	H	X	X	Q ₀	Q ₀
H	X	X	X	X	Z	Z

H = High voltage level.
 L = Low voltage level.
 X = Irrelevant.
 Z = Disabled.
 ↑ = Low to high transition of clock.
 Q₀ = The level of Q before the indicated steady-state input conditions were established.

1/ \overline{OC} = H if any \overline{OC} 1, \overline{OC} 2, or \overline{OC} 3 are high.
 \overline{OC} = L if all of \overline{OC} 1, \overline{OC} 2, or \overline{OC} 3 are low.

FIGURE 2. Truth tables.

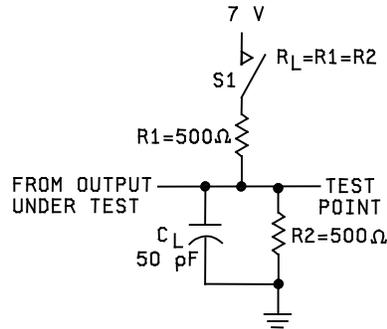
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SIZE
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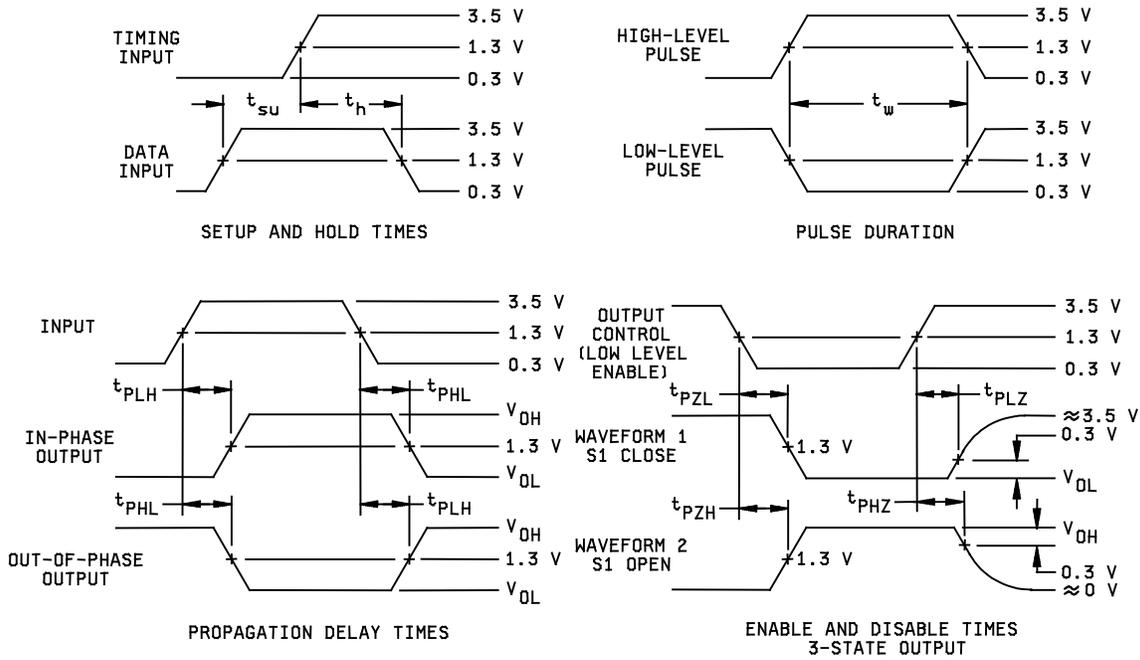
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LOAD CIRCUIT FOR THREE-STATE OUTPUTS



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses have the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f = 3$ ns + 1 ns, duty cycle = 50%.
4. When measuring propagation delay items of 3-state outputs, switch S1 is open.
5. The outputs are measured one at a time with one input transition per measurement.

FIGURE 3. Test circuit and switching waveforms.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A or D The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) T_A = +125°C, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0547.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-90780
		REVISION LEVEL C	SHEET 13

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-10-15

Approved sources of supply for SMD 5962-90780 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9078001MKA	01295	SNJ54AS821AW
5962-9078001MLA	01295	SNJ54AS821AJT
5962-9078001M3A	01295	SNJ54AS821AFK
5962-9078002MKA	<u>3</u> / 3V146	SNJ54AS822W 54AS822/BKA
5962-9078002MLA	<u>3</u> / 3V146	SNJ54AS822JT 54AS822/BLA
5962-9078002M3A	<u>3</u> / 3V146	SNJ54AS822FK 54AS822/B3A
5962-9078003MKA	01295	SNJ54AS825AW
5962-9078003MLA	01295	SNJ54AS825AJT
5962-9078003M3A	01295	SNJ54AS825AFK
5962-9078004MKA	<u>3</u> / 3V146	SNJ54AS826W 54AS826/BKA
5962-9078004MLA	<u>3</u> / 3V146	SNJ54AS826JT 54AS826/BLA
5962-9078004M3A	<u>3</u> / 3V146	SNJ54AS826FK 54AS826/B3A

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ No current source.

Vendor CAGE
number

Vendor name
and address

01295

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
PO Box 660199
Dallas, TX 75243

POC U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

3V146

Rochester Electronics
16 Malcolm Hoyt Drive
Newburyport, MA 01950

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.