REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R270-92	92-08-07	Monica L. Poelking
B	Redrawn with changes. Add device type 02. Editorial changes throughout.	94-02-22	Monica L. Poelking
C	Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. – LTG	03-08-22	Thomas M. Hess
D	Correct the condition I_O for V_{OH} and V_{OL} test in table I. Update boilerplate paragraphs to the latest MIL-PRF-38535 requirements. – jak	10-04-26	Thomas M. Hess
E	Update boilerplate paragraphs to MIL-PRF-38535 requirement. - LTG	16-05-25	Thomas M. Hess

CURRENT CAGE CODE 67268

REV																				
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REV STATUS				REV			E	E	E	E	E	E	E	E	E	E	E	E	E	
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A	PREPARED BY Marcia B. Kelleher	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas J. Ricciuti APPROVED BY Michael A. Frye DRAWING APPROVAL DATE 90-10-15	MICROCIRCUIT, DIGITAL, CMOS, QUAD BILATERAL SWITCH, MONOLITHIC SILICON
	REVISION LEVEL E	SIZE A / CAGE CODE **14933** / **5962-90640**
		SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-90640	01	C	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4016B	Quad bilateral switch
02	14016B	Quad bilateral switch

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range, device type 01 ..... -0.5 V dc to +20 V dc
Supply voltage range, device type 02 ..... -0.5 V dc to +18 V dc
Input voltage range (V_{IN}) ..... -0.5 V dc to V_{DD} + 0.5 V dc
DC input current ..... ±10 mA
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW 3/
Lead temperature (soldering, 10 seconds)..... +300°C-
Thermal resistance, junction-to-case (θ_{JC}): ..... See MIL-STD-1835
Junction temperature (T_J)..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}), device type 01 ..... +3.0 V dc to +18 V dc
Supply voltage range (V_{DD}), device type 02 ..... +3.0 V dc to +15 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltages are referenced to ground.

3/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C to 200 mW.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figures 4 and 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Quiescent supply current	I_{DD}	V_{DD} = 5.0 V V_{IN} = 0.0 V or V_{DD} 1/		All	1, 3		0.25	µA
					2		7.5	
		V_{DD} = 10 V V_{IN} = 0.0 V or V_{DD} 1/		All	1, 3		0.5	
					2		15	
		V_{DD} = 15 V V_{IN} = 0.0 V or V_{DD} 1/		All	1, 3		1	
					2		30	
		V_{DD} = 20 V V_{IN} = 0.0 V or V_{DD} 2/		01	1, 3		5	
					2		150	
Low level output voltage	V_{OL}	V_{IN} = 0.0 V or V_{DD} I_{OL} < 1 µA	V_{DD} = 5 V 1/	02	1, 2, 3		0.05	V
			V_{DD} = 10 V 1/	02	1, 2, 3		0.05	
			V_{DD} = 15 V	02	1, 2, 3		0.05	
High level output voltage	V_{OH}	V_{IN} = 0.0 V or V_{DD} I_{OH} < 1 µA	V_{DD} = 5 V 1/	02	1, 2, 3	4.95		
			V_{DD} = 10 V 1/	02	1, 2, 3	9.95		
			V_{DD} = 15 V	02	1, 2, 3	14.95		
Low level input voltage, control inputs	V_{IL}	V_{DD} = 5.0 V I_{IL} < 10 µA	V_{IN} = GND V_{OUT} = V_{DD} and V_{IN} = V_{DD} V_{OUT} = GND	01	1		0.7	V
					2		0.4	
					3		0.9	
				02	1, 2, 3		0.9	
		V_{DD} = 10 V I_{IL} < 10 µA 1/	V_{IN} = GND V_{OUT} = V_{DD} and V_{IN} = V_{DD} V_{OUT} = GND	01	1		0.7	
					2		0.4	
					3		0.9	
				02	1, 2, 3		0.9	
		V_{DD} = 15 V I_{IL} < 10 µA	V_{IN} = GND V_{OUT} = V_{DD} and V_{IN} = V_{DD} V_{OUT} = GND	01	1		0.7	
					2		0.4	
					3		0.9	
				02	1, 2, 3		0.9	
High level input voltage, control	V_{IH}	V_{DD} = 5.0 V		01	1, 2, 3	3.5		V
				02		3.0		
		V_{DD} = 10 V 1/		01	1, 2, 3	7.0		
				02		8.0		
		V_{DD} = 15 V		01	1, 2, 3	11.0		
				02		13.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Low level output current	I_{OL}	V_{DD} = 5.0 V 3/ V_{OUT} = 0.4 V V_{IN} = 0.0 V or V_{DD}	02	1	0.51		mA
				2	0.36		
				3	0.64		
		V_{DD} = 10 V 1/ V_{OUT} = 0.5 V V_{IN} = 0.0 V or V_{DD}	02	1	1.3		
				2	0.9		
				3	1.6		
		V_{DD} = 15 V 1/ V_{OUT} = 1.5 V V_{IN} = 0.0 V or V_{DD}	02	1	3.4		
				2	2.4		
				3	4.2		
High level output current	I_{OH}	V_{DD} = 5.0 V 3/ V_{OUT} = 4.6 V V_{IN} = 0.0 V or V_{DD}	02	1	-0.51		mA
				2	-0.36		
				3	-0.64		
		V_{DD} = 5.0 V 3/ V_{OUT} = 2.5 V V_{IN} = 0.0 V or V_{DD}	02	1	-1.6		mA
				2	-1.15		
				3	-2.0		
		V_{DD} = 10 V 1/ V_{OUT} = 9.5 V V_{IN} = 0.0 V or V_{DD}	02	1	-1.3		mA
				2	-0.9		
				3	-1.60		
		V_{DD} = 15 V 1/ V_{OUT} = 13.5 V V_{IN} = 0.0 V or V_{DD}	02	1	-3.4		mA
				2	-2.4		
				3	-4.2		
Input current	I_{IN}	V_{DD} = 20 V 2/ V_{IN} = 0.0 V or V_{DD}	01	1, 3		±0.1	µA
				2		±1.0	
		V_{DD} = 15 V V_{IN} = 0.0 V or V_{DD}	02	1, 3		±0.1	
				2		±1.0	
Input/output leakage current (Switch off)	I_{IS}	$V_{CONTROL}$ = 0 V V_{IN} = 18 V V_{OUT} = 0.0 V	All	1, 3		±0.1	µA
				2		±1.0	
		$V_{CONTROL}$ = 0 V V_{IN} = 0.0 V V_{OUT} = 18 V	All	1, 3		±0.1	µA
				2		±1.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits Min	Limits Max	Unit
On-state resistance	R_{ON}	$V_{CONTROL} = V_{DD}$ $R_L = 10\ k\Omega$ Returned to $V_{DD} - GND/2$	$V_{DD} = 10\ V$ $V_{IN} = V_{DD}$ or GND	All	1		660	Ω
					2		960	
					3		600	
			$V_{DD} = 10\ V$ $V_{IN} = 4.75\ V$ to $5.75\ V$		1		2000	
					2		2600	
					3		1870	
			$V_{DD} = 15\ V$ $V_{IN} = V_{DD}$ or GND		1		400	
					2		600	
					3		360	
			$V_{DD} = 15\ V$ $V_{IN} = 7.25\ V$ to $7.75\ V$		1		850	
					2		1230	
					3		775	
Delta on-state resistance between any two switches	ΔR_{ON}	$V_{CONTROL} = V_{DD}$ $R_L = 10\ k\Omega$ 1/ $V_{SS} = 0.0\ V$	$V_{DD} = 5\ V$	01	1		15	Ω
			$V_{DD} = 10\ V$	01	1		15	
				02	1		15	
			$V_{DD} = 15\ V$	01	1		10	
				02	1		10	
Input capacitance	C_{IN}	V_{DD} = GND See 4.3.1c		All	4		7.5	pF
Functional test		See 4.3.1d		All	7, 8			
Propagation delay time, input to output	t_{PHL}, t_{PLH}	$R_L = 200\ k\Omega$ device 01 $R_L = 10\ k\Omega$ device 02 $C_L = 50\ pF$ $t_r, t_f = 20\ ns$ $V_{CONTROL} = V_{DD}$ $V_{IN} = V_{DD}$ (square wave centered on $V_{DD}/2$) See figure 4	$V_{DD} = 5\ V$	All	9	1.5 4/	100	ns
					10, 11	1.5 4/	160	
			$V_{DD} = 10\ V$ 1/		9	1.5 4/	40	
					10, 11	1.5 4/	64	
			$V_{DD} = 15\ V$ 1/		9	1.5 4/	30	
					10, 11	1.5 4/	48	
Propagation delay time, control input to switch output (turn on)	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	$R_L = 1\ k\Omega$ $C_L = 50\ pF$ $t_r, t_f = 20\ ns$ See figure 5	$V_{DD} = 5\ V$	All	9	1.5 4/	70	ns
					10, 11	1.5 4/	112	
			$V_{DD} = 10\ V$ 1/		9	1.5 4/	40	
					10, 11	1.5 4/	64	
			$V_{DD} = 15\ V$ 1/		9	1.5 4/	30	
					10, 11	1.5 4/	48	

1/ For device type 01, this parameter is guaranteed, if not tested, to the limits specified in table I.

2/ At -55°C, this test is performed with $V_{DD} = 18\ V$ dc.

3/ The I_{OL} and I_{OH} tests are tested 100 percent at $T_C = +25°C$, and are guaranteed, if not tested, for $T_C = -55°C$ and $T_C = +125°C$.

4/ The minimum limit for device type 01 only = 1.5 ns.

Device types	01 and 02
Case outline	C
Terminal number	Terminal symbol
1	INPUT/OUPUT SIG A
2	OUTPUT/INPUT SIG A
3	OUTPUT/INPUT SIG B
4	INPUT/OUTPUT SIG B
5	CONTROL B
6	CONTROL C
7	GND
8	INPUT/OUTPUT SIG C
9	OUTPUT/INPUT SIG C
10	OUTPUT/INPUT SIG D
11	INPUT/OUTPUT SIG D
12	CONTROL D
13	CONTROL A
14	V_{DD}

FIGURE 1. Terminal connections.

Each switch		
Inputs		Output
$V_{CONTROL}$	V_{IN}	V_{OUT}
H	L	L
H	H	H
L	L	OPEN
L	H	OPEN

H = High voltage level (steady-state)
L = Low voltage level (steady-state)

Positive logic: Switch on $V_{CONTROL}$ = High
Switch off $V_{CONTROL}$ = Low

FIGURE 2. Truth table.

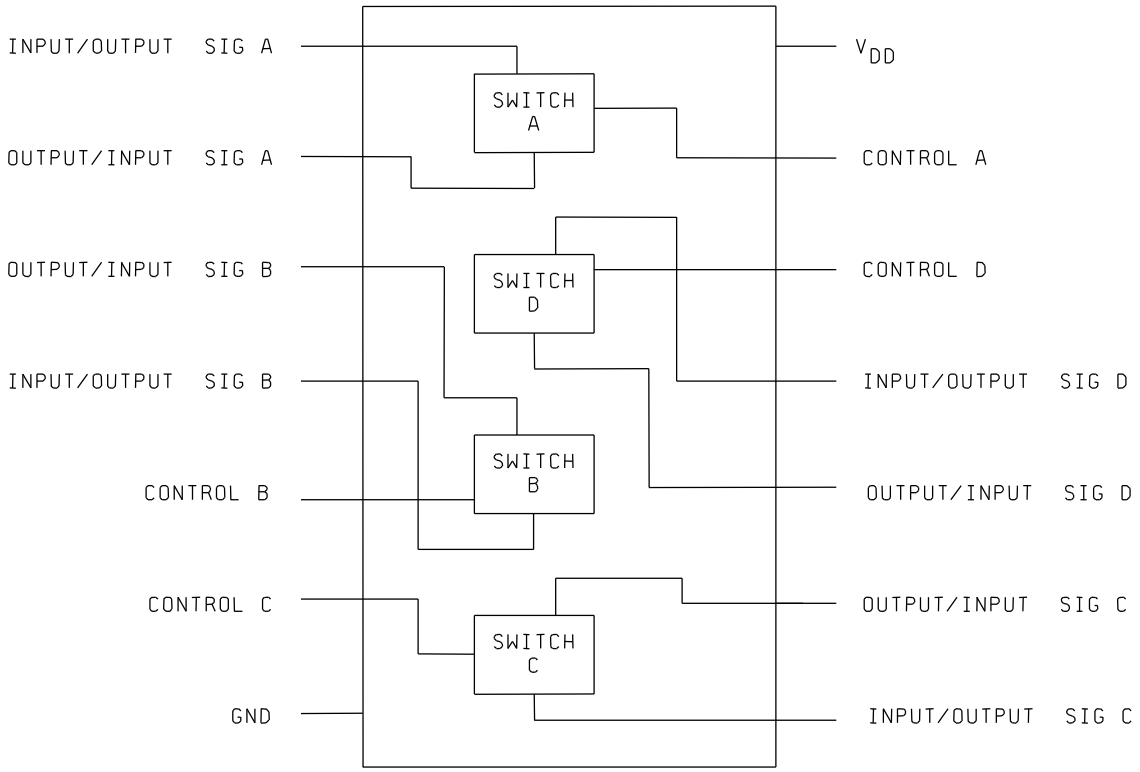
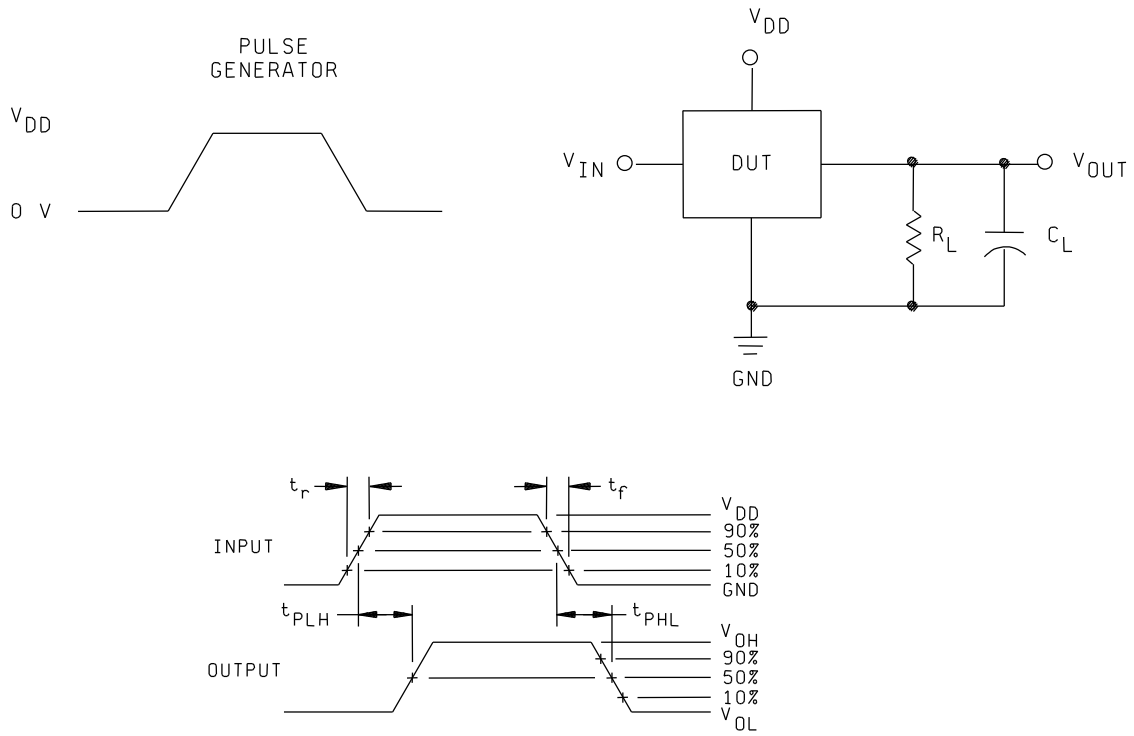
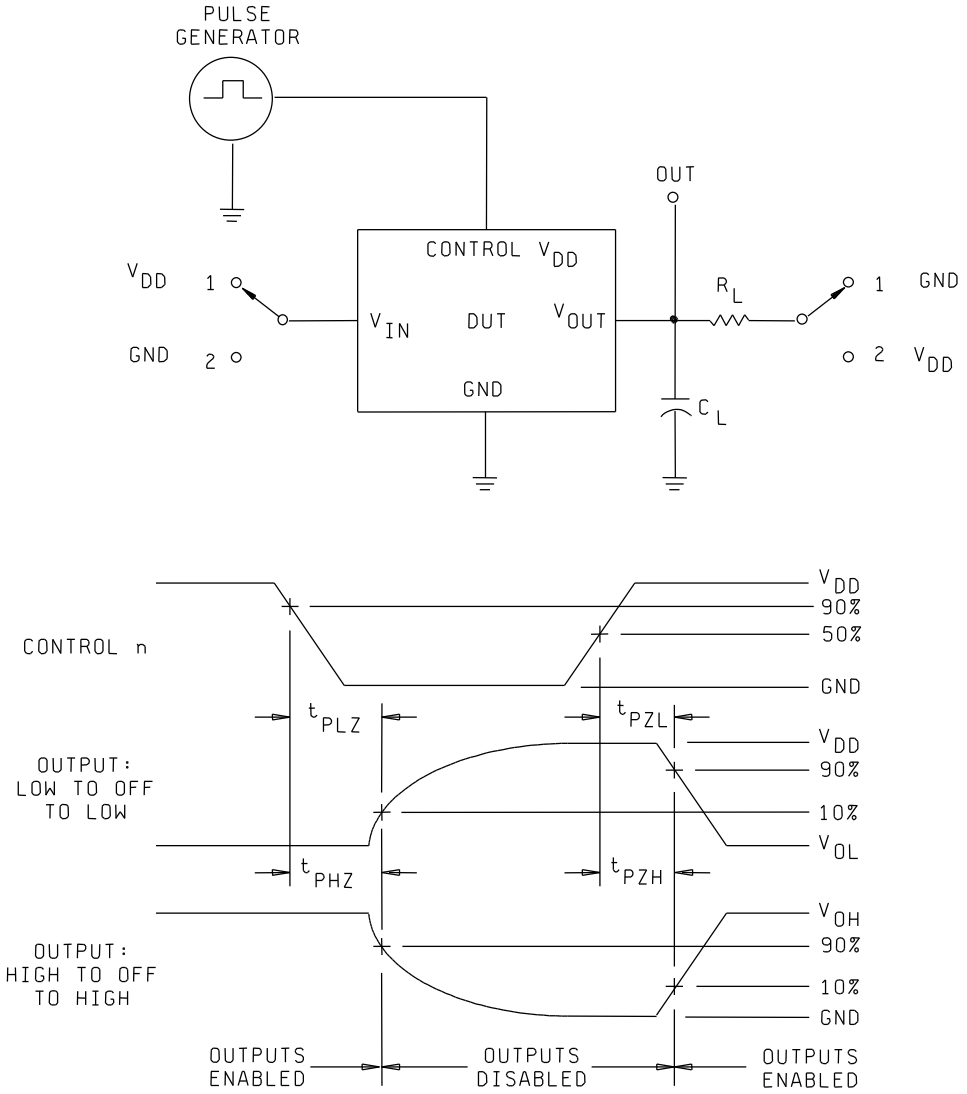


FIGURE 3. Logic diagram.



NOTES:
1. Pulse generator characteristics: $V_{GEN} = V_{DD} \pm 1$ percent, duty cycle = 50 percent, t_r and t_f = 20 ns ±2.0 ns.
2. R_L = 200 kΩ for device type 01 and R_L = 10 kΩ for device type 02.
3. C_L = 50 pF includes probe and jig capacitance.
4. Identical switching measurements are obtained from switch A, switch B, switch C, and switch D.

FIGURE 4. Switching waveforms and test circuit, switch input to switch output.



NOTES:

1. Pulse generator characteristics: $V_{GEN} = V_{DD} \pm 1$ percent, duty cycle = 50 percent, t_r and t_f = 20 ns ±2.0 ns.
2. R_L = 1 kΩ.
3. C_L = 50 pF includes probe and jig capacitance.
4. Identical switching measurements are obtained from switch A, switch B, switch C, and switch D.
5. Switch position 1 for t_{PZH} and t_{PHZ} tests; switch position 2 for t_{PLZ} and t_{PZL} tests.

FIGURE 5. Switching waveforms and test circuit, switch control to switch output.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	----
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, are guaranteed to the limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on five devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-05-25

Approved sources of supply for SMD 5962-90640 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9064001CA	01295	CD4016BF3A
5962-9064002CA	3/	14016B/BEAJC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.