REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add delta limits for class V devices. Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. – jak	06-11-13	Thomas M. Hess
B	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	13-03-25	Thomas M. Hess
C	Remove class M references. Update boilerplate paragraphs and drawing to current MIL-PRF-38535 requirements. –RDC	21-03-01	Muhammad A. Akbar

REV																				
SHEET																				
REV	C	C																		
SHEET	15	16																		

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
94-12-15

REVISION LEVEL
B

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL, HIGH-SPEED CMOS, 8-BIT SERIAL/PARALLEL-IN, SERIAL-OUT SHIFT REGISTER, MONOLITHIC SILICON

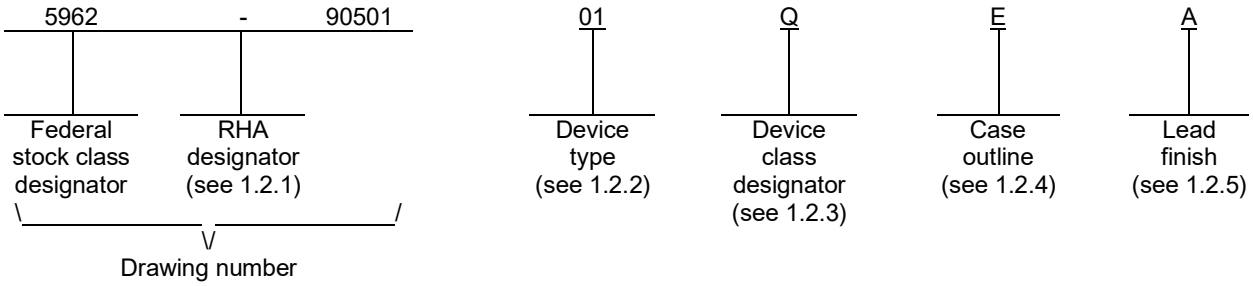
SIZE	CAGE CODE	
A	**67268**	**5962-90501**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC166	Eight-bit serial/parallel-in, serial-out shift register

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V
.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input clamp current (I_{IK})	±20 mA
DC output clamp current (I_{OK})	±20 mA
DC output current (I_{OUT}) (per pin)	±25 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) (per pin)	±50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW 3/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 4/

Supply voltage range (V_{CC})	+2.0 V dc to +6.0 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum low level input voltage (V_{IL}):	
V_{CC} = 2.0 V	0.3 V dc
V_{CC} = 4.5 V	0.9 V dc
V_{CC} = 6.0 V	1.2 V dc
Minimum high level input voltage (V_{IH}):	
V_{CC} = 2.0 V	1.5 V dc
V_{CC} = 4.5 V	3.15 V dc
V_{CC} = 6.0 V	4.2 V dc
Input rise and fall times (t_r, t_f):	
V_{CC} = 2.0 V	1000 ns 5/
V_{CC} = 4.5 V	500 ns
V_{CC} = 6.0 V	400 ns
Minimum high level output current (I_{OH})	-5.2 mA at V_{CC} = 6.0 V
Maximum low level output current (I_{OL})	+5.2 mA at V_{CC} = 6.0 V

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2/ Unless otherwise specified, all voltages are referenced to GND.

3/ For T_C = +100°C to +125°C, derate linearly at 8 mW/°C to 300 mW.

4/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

5/ Transition times = 1000 ns will not harm the device, however, functionality is not guaranteed for the CLK input while in the shift mode.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD7 - Standard for Description of 54/74HCXXXXX and 54/74HCTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at https://www.jedec.org).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $2.0\ V \le V_{CC} \le 6.0\ V$ unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits 2/		Unit
						Min	Max	
High level output voltage 3006	V_{OH1}	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 1.5\ V$, $V_{IL} = 0.3\ V$ For all other $V_{IN} = V_{CC}$ or GND $I_{OH} = -20\ \mu A$	2.0 V	All	1, 2, 3	1.9		V
	V_{OH2}	For all inputs affecting output under test, $V_{IN} = V_{IH99}$ or V_{IL} $V_{IH} = 3.15\ V$, $V_{IL} = 0.9\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -20\ \mu A$	4.5 V	All	1, 2, 3	4.4		
	V_{OH3}	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 4.2\ V$, $V_{IL} = 1.2\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -20\ \mu A$	6.0 V	All	1, 2, 3	5.9		
	V_{OH4}	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$, $V_{IL} = 0.9\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -4.0\ mA$	4.5 V	All	1	3.98		
					2, 3	3.70		
	V_{OH5}	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 4.2\ V$, $V_{IL} = 1.2\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -5.2\ mA$	6.0 V	All	1	5.48		
					2, 3	5.20		
Low level output voltage 3007	V_{OL1}	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 1.5\ V$, $V_{IL} = 0.3\ V$ For all other, $V_{IN} = V_{CC}$ or GND $I_{OL} = +20\ \mu A$	2.0 V	All	1, 2, 3		0.1	V
	V_{OL2}	For all inputs affecting output under test, $V_{IN} = V_{IH99}$ or V_{IL} $V_{IH} = 3.15\ V$, $V_{IL} = 0.9\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = +20\ \mu A$	4.5 V	All	1, 2, 3		0.1	
	V_{OL3}	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 4.2\ V$, $V_{IL} = 1.2\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = +20\ \mu A$	6.0 V	All	1, 2, 3		0.1	
	V_{OL4}	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$, $V_{IL} = 0.9\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = +4.0\ mA$	4.5 V	All	1		0.26	
					2, 3		0.4	
	V_{OL5}	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 4.2\ V$, $V_{IL} = 1.2\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = +5.2\ mA$	6.0 V	All	1		0.26	
					2, 3		0.4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $2.0\ V \le V_{CC} \le 6.0\ V$ unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits 2/		Unit
						Min	Max	
Input current high 3010	I_{IH}	For input under test, $V_{IN} = V_{CC}$ For all other, $V_{IN} = V_{CC}$ or GND	6.0 V	All	1		0.1	µA
					2, 3		1.0	
Input current low 3009	I_{IL}	For input under test, V_{IN} = GND For all other, $V_{IN} = V_{CC}$ or GND	6.0 V	All	1		-0.1	µA
					2, 3		-1.0	
Quiescent supply current output high 3005	I_{CCH}	For all inputs, $V_{IN} = V_{CC}$ or GND I_{OUT} = 0.0 mA	6.0 V	All	1		8.0	µA
					2, 3		160	
Quiescent supply current output low 3005	I_{CCL}	For all inputs, $V_{IN} = V_{CC}$ or GND I_{OUT} = 0.0 mA	6.0 V	All	1		8.0	µA
					2, 3		160	
Input capacitance 3012	C_{IN}	V_{IN} = 0.0 V T_C = 125°C See 4.4.1c	GND	All	4		10	pF
Truth table test output voltage 3014	3/ 4/	V_{IL} = 50% V_{IL} max $V_{IH} = V_{IH}$ min+20% Verify output V_O See 4.4.1b	2.0 V	All	7, 8	L	H	
			4.5 V			L	H	
			6.0 V			L	H	
Maximum clock frequency	f_{CLOCK}	C_L = 50 pF minimum See figure 4	2.0 V	All	9		6	MHz
					10, 11		4.2	
			4.5 V		9		31	
					10, 11		21	
			6.0 V		9		36	
					10, 11		25	
Minimum pulse width, $\overline{CLR}$ low	t_{w1}		2.0 V	All	9	100		ns
					10, 11	150		
			4.5 V		9	20		
					10, 11	30		
			6.0 V		9	17		
					10, 11	26		
Minimum pulse width, CLK high or low	t_{w2}		2.0 V	All	9	80		ns
					10, 11	120		
			4.5 V		9	16		
					10, 11	24		
			6.0 V		9	14		
					10, 11	20		
Minimum setup time, SH/$\overline{LD}$ high before CLK ↑	t_{s1}		2.0 V	All	9	145		ns
					10, 11	220		
			4.5 V		9	29		
					10, 11	44		
			6.0 V		9	25		
					10, 11	38		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $2.0\ V \le V_{CC} \le 6.0\ V$ unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits 2/		Unit
						Min	Max	
Minimum setup time, SER before CLK ↑	t_{s2}	C_L = 50 pF minimum See figure 4	2.0 V	All	9	80		ns
					10, 11	120		
			4.5 V		9	16		
					10, 11	24		
			6.0 V		9	14		
					10, 11	20		
Minimum setup time, CLK INH low before CLK ↑	t_{s3}		2.0 V	All	9	100		ns
					10, 11	150		
			4.5 V		9	20		
					10, 11	30		
			6.0 V		9	17		
					10, 11	26		
Minimum setup time, data before CLK ↑	t_{s4}		2.0 V	All	9	80		ns
					10, 11	120		
			4.5 V		9	16		
					10, 11	24		
			6.0 V		9	14		
					10, 11	20		
Minimum setup time $\overline{CLR}$, inactive before CLK ↑	t_{s5}		2.0 V	All	9	40		ns
					10, 11	60		
			4.5 V		9	8		
					10, 11	12		
			6.0 V		9	7		
					10, 11	10		
Minimum hold time, SH/$\overline{LD}$ high after CLK ↑	t_{h1}		2.0 V	All	9, 10, 11	0		ns
			4.5 V		9, 10, 11	0		
			6.0 V		9, 10, 11	0		
Minimum hold time, SER after CLK ↑	t_{h2}		2.0 V	All	9, 10, 11	5		ns
			4.5 V		9, 10, 11	5		
			6.0 V		9, 10, 11	5		
Minimum hold time, CLK INH high after CLK ↑	t_{h3}		2.0 V	All	9, 10, 11	0		ns
			4.5 V		9, 10, 11	0		
			6.0 V		9, 10, 11	0		
Minimum hold time, data after CLK ↑	t_{h4}		2.0 V	All	9, 10, 11	5		ns
			4.5 V		9, 10, 11	5		
			6.0 V		9, 10, 11	5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $2.0\ V \le V_{CC} \le 6.0\ V$ unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits 2/		Unit
						Min	Max	
Maximum clock frequency	f_{MAX}	C_L = 50 pF minimum See figure 4	2.0 V	All	9	6		MHz
					10, 11	4.2		
			4.5 V	All	9	31		
					10, 11	21		
			6.0 V	All	9	36		
					10, 11	25		
Propagation delay time, clock to output, CLK to QH 3003	t_{PLH1}, t_{PHL1}		2.0 V	All	9	150		ns
					10, 11	225		
			4.5 V	All	9	30		
					10, 11	45		
			6.0 V	All	9	26		
					10, 11	38		
Propagation delay time, clear to output, $\overline{CLR}$ to QH 3003	t_{PHL2}		2.0 V	All	9	120		ns
					10, 11	180		
			4.5 V	All	9	24		
					10, 11	36		
			6.0 V	All	9	20		
					10, 11	31		
Output transition time 3004	t_{TLH}, t_{THL}		2.0 V	All	9		75	ns
					10, 11		110	
			4.5 V	All	9		15	
					10, 11		22	
			6.0 V	All	9		13	
					10, 11		19	

1/ Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

3/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. $H \ge 0.5V_{CC}$, $L < 0.5V_{CC}$.

4/ The values to be used for V_{IL} max and V_{IH} min are listed in section 1.4 herein.

Device type	01	
Case outlines	E	2
Terminal number	Terminal symbol	
1	SER	NC
2	A	SER
3	B	A
4	C	B
5	D	C
6	CLK INH	NC
7	CLK	D
8	GND	CLK INH
9	$\overline{\text{CLR}}$	CLK
10	E	GND
11	F	NC
12	G	$\overline{\text{CLR}}$
13	QH	E
14	H	F
15	SH/$\overline{\text{LD}}$	G
16	V_{CC}	NC
17		QH
18		H
19		SH/$\overline{\text{LD}}$
20		V_{CC}

NC = No internal connection

Terminal description	
Terminal symbol	Description
A through H	Data inputs
SER	Serial data input
QH	Output
SH/$\overline{\text{LD}}$	Shift/load input
CLK	Clock input
CLK INH	Clock inhibit (active high)
$\overline{\text{CLR}}$	Clear input (active low)

FIGURE 1. Terminal connections.

Inputs						Internal outputs		Output QH
Clear ($\overline{CLR}$)	Shift load (SH/$\overline{LD}$)	Clock inhibit (CLK INH)	Clock (CLK)	Serial input (SER)	Parallel inputs			
					A . . . H	QA	QB	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA0	QB0	QH0
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	QAn	QGn
H	H	L	↑	L	X	L	QAn	QGn
H	X	H	↑	X	X	QA0	QB0	QH0

H = High voltage level
L = Low voltage level
X = Irrelevant (any input, including transitions)
↑ = Transition from low-to-high level.
a . . . . h = The level of stead-state input at inputs A through H, respectively.
QA0, QB0, QH0 = The level of QA, QB or QH, respectively, before the indicated steady-state input conditions were established.
QAn, QGn = The level of QA or QG, respectively, before the most recent ↑ clock transition.

FIGURE 2. Truth table.

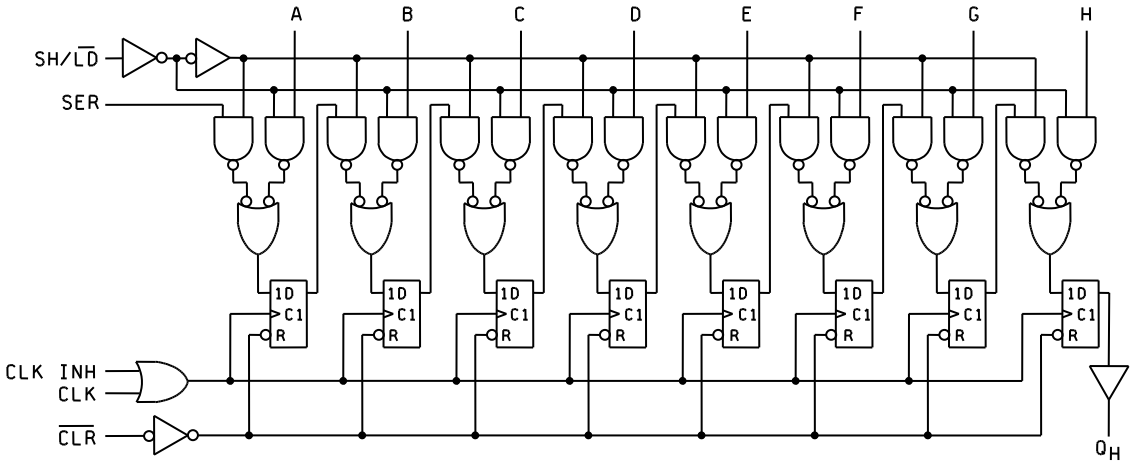


FIGURE 3. Logic diagram.

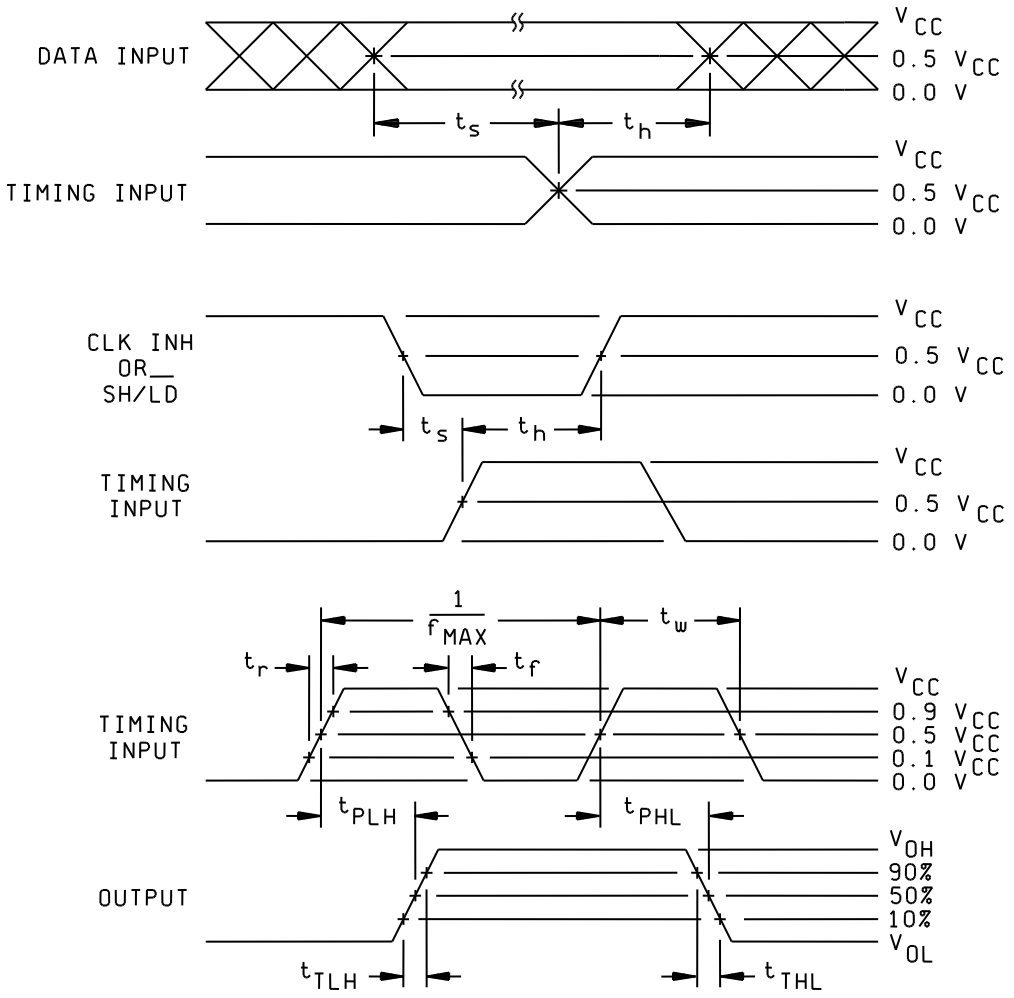
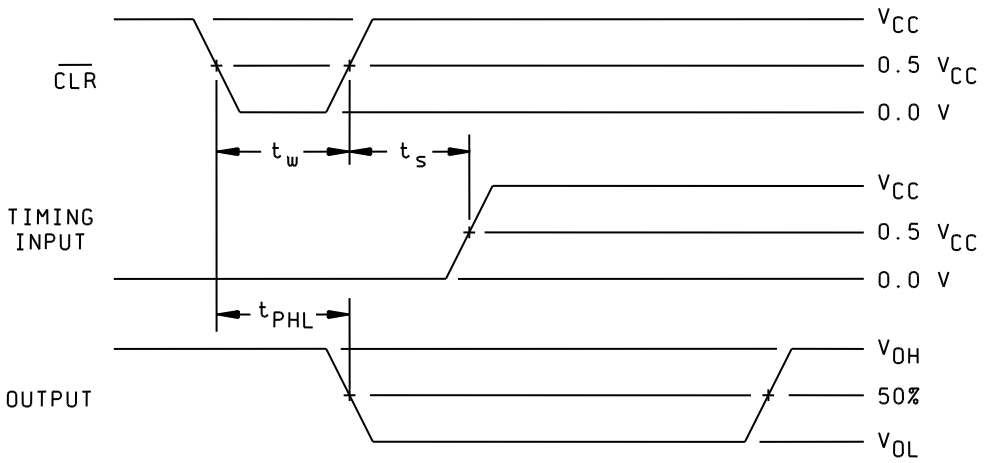
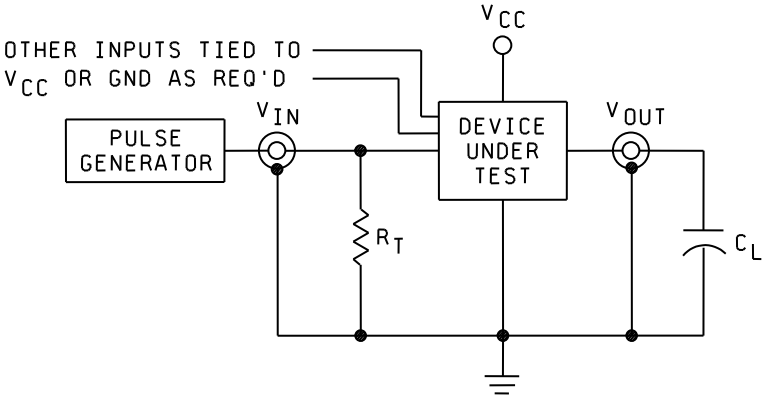


FIGURE 4. Switching waveforms and test circuit.





NOTES:
1. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 1 MHz; t_r ≤ 6 ns; t_f ≤ 6 ns; duty cycle = 50 percent.
2. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
3. R_T = 50Ω or equivalent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in table III shall be required where specified and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE III. Burn-in and operating life test delta parameters (+25°C).

Parameter	Symbol	Delta limits
Quiescent current	I_{CC}	±120 nA
Input current low level	I_{IL}	±20 nA
Input current high level	I_{IH}	±20 nA
Output voltage low level (I_{OL} = 4 mA, V_{CC} = 4.5 V)	V_{OL}	±0.026 V
Output voltage high level (I_{OH} = -4 mA, V_{CC} = 4.5 V)	V_{OH}	±0.20 V

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-03-01

Approved sources of supply for SMD 5962-90501 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9050101QEA	01295	SNJ54HC166J
		CD54HC166F3A
5962-9050101Q2A	01295	SNJ54HC166FK
5962-9050101VEA	01295	SNV54HC166J

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243