REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes IAW NOR 5962-R206-92. Editorial changes. --tvn	92-05-11	Tim H. Noh
B	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	02-06-10	Raymond Monnin
C	Update drawing to current requirements. Editorial changes throughout. - gap	09-08-05	Charles F. Saffle
D	Update drawing to current MIL-PRF-38535 requirements. - jt	16-06-24	Charles F. Saffle

The original first sheet of this drawing has been replaced.

REV																				
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REV STATUS				REV			D	D	D	D	D	D	D	D	D	D	D	D		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Larry T. Gauder

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

CHECKED BY
Tim H. Noh

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
89-10-26

AMSC N/A

REVISION LEVEL
D

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED LOW POWER SCHOTTKY TTL, OCTAL BUS TRANSCEIVERS AND REGISTERS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89956**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89956	01	L	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALS646	Octal bus transceivers and registers with non-inverting 3-state outputs

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line package
K	GDFP2-F24 or CDFP3-F24	24	Flat package
3	CQCC1-N28	28	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage	-1.5 V dc at -18 mA to +7.0 V dc
Off-state output voltage	+5.5 V dc
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	358 mW 1/
Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Maximum high level output current (I_{OH})	-1.0 mA
Maximum low level output current (I_{OL}):	
$Q_{H'}$ output	8 mA
Q output	12 mA

1/ Must withstand the added P_D due to short circuit test (e.g. I_{OS}).

1.4 Recommended operating conditions.

Case operating temperature range (T_C) ..... -55°C to +125°C
Pulse duration, clocks high or low (t_W) ..... 14.5 ns minimum
Setup time, A before CAB↑ or B before CBA↑ (t_S) ..... 15.0 ns minimum
Hold time, A after CAB↑ or B after CBA↑ (t_H) ..... 01.0 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritimes agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified			Group A subgroups	Device type	Limits		Unit
							Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V V_{IH} = 2.0 V 2/	V_{IL} = 0.8 V	I_{OH} = -0.4 mA	1, 3	01	2.5		V
			V_{IL} = 0.7 V		2	01	2.5		V
			V_{IL} = 0.8 V	I_{OH} = -3.0 mA	1, 3	01	2.4		V
			V_{IL} = 0.7 V		2	01	2.4		V
			V_{IL} = 0.8 V	I_{OH} = -12 mA	1, 3	01	2.0		V
			V_{IL} = 0.7 V		2	01	2.0		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V V_{IH} = 2.0 V I_{OL} = 12 mA 2/	V_{IL} = 0.8 V		1,3	01		0.4	V
			V_{IL} = 0.7 V		3	01		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA			1, 2, 3	01		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V 3/	V_{IN} = 7.0 V	Control inputs	1, 2, 3	01		0.1	mA
			V_{IN} = 5.5 V	A or B ports		01		0.1	mA
	I_{IH2}		V_{IN} = 2.7 V	Control inputs		01		20	μA
				A or B ports		01		20	μA
Low level input current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.4 V		Control inputs	1, 2, 3	01		-0.2	mA
				A or B ports	1, 2, 3	01		-0.2	mA
Output current	I_O	V_{CC} = 5.5 V, V_{OUT} = 2.25 V 4/			1, 2, 3	01	-20	-112	mA
Supply current	I_{CCH}	V_{CC} = 5.5 V		Outputs high	1, 2, 3	01		76	mA
	I_{CCL}			Outputs low	1, 2, 3	01		88	mA
	I_{CCZ}			Outputs disabled	1, 2, 3	01		88	mA
Functional tests		See 4.3.1c 5/			7, 8				
Maximum frequency	f_{MAX}	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω See figure 3 6/			9, 10, 11	01	35		MHz
Propagation delay time, CBA, CAB to An, Bn	t_{PLH1}				9, 10, 11	01	10	35	ns
	t_{PHL1}					01	5	20	ns
Propagation delay time, An, Bn to Bn, An	t_{PLH2}				9, 10, 11	01	5	22	ns
	t_{PHL2}					01	3	15	ns
Propagation delay time, SBA, SAB to An, Bn (with An, Bn low) 7/	t_{PLH3}				9, 10, 11	01	10	40	ns
	t_{PHL3}					01	5	23	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. .

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, SBA, SAB to An, Bn (with An, Bn high) 7/	t_{PLH4}	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω See figure 3 6/	9, 10, 11	01	8	30	ns
	t_{PHL4}				5	24	ns
Enable time, $\overline{G}$ to An, Bn	t_{PZH1}		9, 10, 11	01	3	20	ns
	t_{PZL1}			01	5	22	ns
Disable time, $\overline{G}$ to An, Bn	t_{PHZ1}		9, 10, 11	01	1	12	ns
	t_{PLZ1}			01	1	20	ns
Enable time, DIR to An, Bn	t_{PZH2}		9, 10, 11	01	5	38	ns
	t_{PZL2}			01	5	30	ns
Disable time, DIR to An, Bn	t_{PHZ2}		9, 10, 11	01	1	12	ns
	t_{PLZ2}			01	2	21	ns

1/ Unused inputs that do not directly control the pin under test must be put at ≥ 2.5 V or ≤ 0.4 V. No unused inputs shall be floated.
2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper state, the test must be performed with each input being selected as the V_{IL} maximum or V_{IH} minimum input.
3/ For I/O ports, the parameters I_{IH2} and I_{IL} include the off-state output current.
4/ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and duration of the test condition shall not exceed one second.
5/ Functional tests shall be conducted at input test conditions of GND ≤ V_{IL} ≤ V_{OL} and V_{OH} ≤ V_{IH} ≤ V_{CC}.
6/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V.
7/ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Device type 01		
Case outlines	K and L	3
Terminal number	Terminal symbols	
1	CAB	NC
2	SAB	CAB
3	DIR	SAB
4	A1	DIR
5	A2	A1
6	A3	A2
7	A4	A3
8	A5	NC
9	A6	A4
10	A7	A5
11	A8	A6
12	GND	A7
13	B8	A8
14	B7	GND
15	B6	NC
16	B5	B8
17	B4	B7
18	B3	B6
19	B2	B5
20	B1	B4
21	$\overline{G}$	B3
22	SBA	NC
23	CBA	B2
24	V_{CC}	B1
25		$\overline{G}$
26		SBA
27		CBA
28		V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

Inputs						Data I/O		Operation mode
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified 1/	Store A, B unspecified 1/
X	X	X	↑	X	X	Unspecified 1/	Input	Store B, A unspecified 1/
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H/LX	H/L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H/L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H/L	X	H	X	Input	Output	Stored A data to B bus

H = High logic level
L = Low logic level
↑ = Transition from a low to a high logic level
X = Irrelevant
H/L = High or low logic level

1/ The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low to high transition on the clock inputs.

FIGURE 2. Truth table.

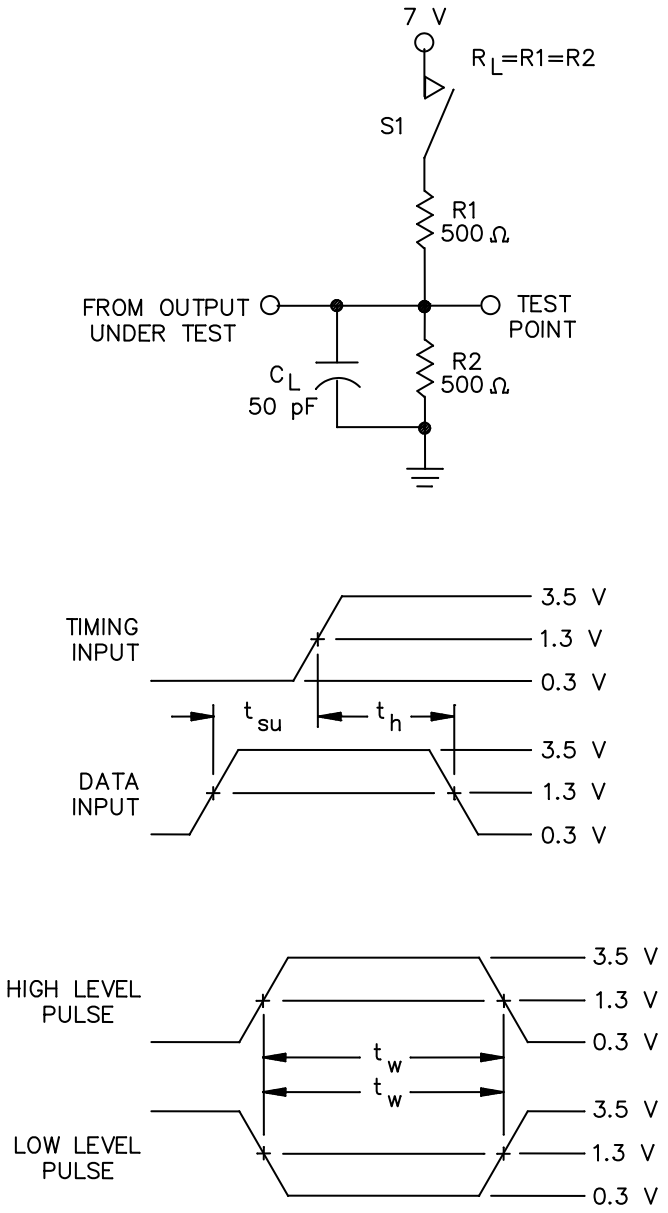
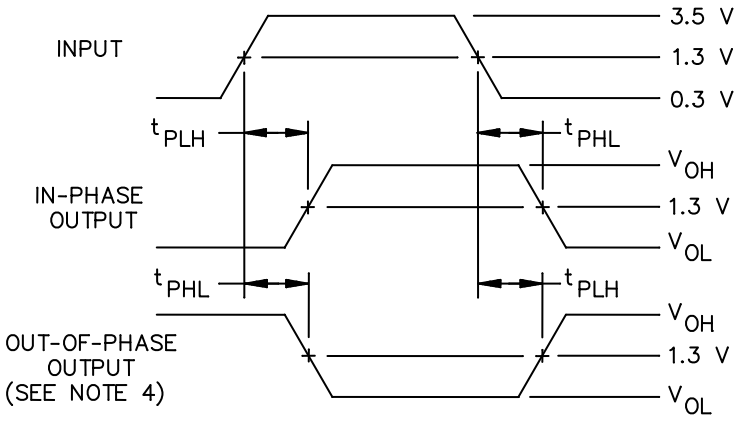
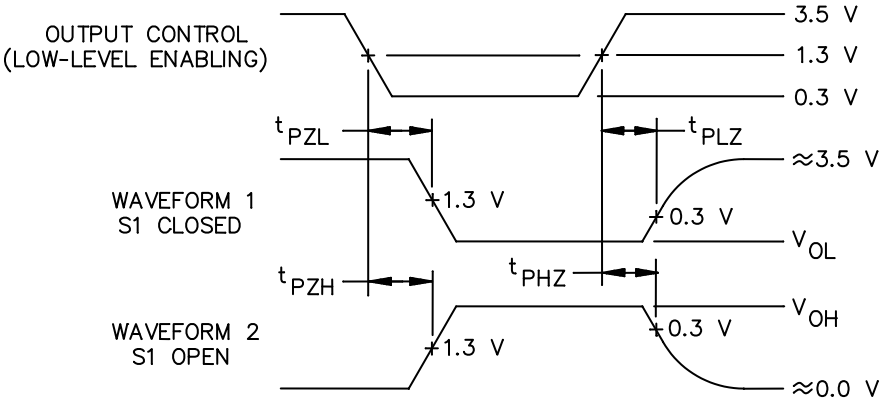


FIGURE 3. Test circuit and switching waveforms.





NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by output control.
3. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by output control.
4. When measuring propagation delay items of three-state outputs, switch S1 is open.
5. The outputs are measured one at a time with one input transition per measurement.
6. All input pulses have the following characteristics: PRR $\leq$ 10 MHz, duty cycle = 50 percent, $t_r = t_f$ = 3 ns $\pm$1 ns.

FIGURE 3. Test circuit and switching waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-06-24

Approved sources of supply for SMD 5962-89956 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8995601LA	01295	SNJ54ALS646JT
5962-8995601KA	01295	SNJ54ALS646W
5962-89956013A	3/	SNJ54ALS646FK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane. P.O. Box 660199 Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.