| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Changes in accordance with NOR 5962-R188-92. | 92-04-14 | Tim H. Noh |
| B | Redraw with changes. Update to current requirements. Editorial changes throughout. - gap | 06-07-06 | Raymnd Monnin |
| C | Update drawing to current MIL-PRF-38535 requirements. - jt | 16-08-08 | Charles F. Saffle |
| D | Update drawing to latest MIL-PRF-38535 requirements. - jt | 21-04-12 | James R. Eschmeyer |

The original first sheet of this drawing has been replaced.

| | | | | | | | | | | | | | | | | | | | | |
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| REV | | | | | | | | | | | | | | | | | | | | |
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| REV STATUS | REV | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | | | | |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | | | | |

PMIC N/A

PREPARED BY
Tim H. Noh

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**https://www.dla.mil/LandandMaritime**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Tim H. Noh

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
89-09-06

REVISION LEVEL
D

MICROCIRCUITS, DIGITAL, BIPOLAR, ADVANCED LOW POWER SCHOTTKY TTL, 8-BIT D-TYPE EDGE-TRIGGERED READ BACK LATCHES, MONOLITHIC SILICON

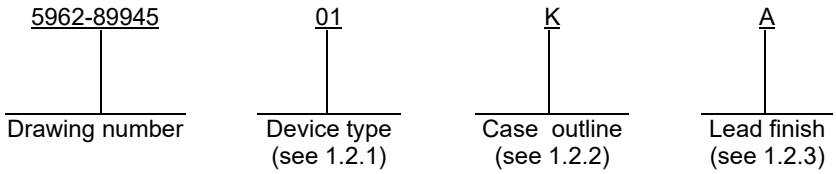
| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-89945** |

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:




1.2.1 Device type. The device type identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54ALS996 | 8-bit D-type edge-triggered read back latches |

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| K | GDFP2-F24 or CDFP3-F24 | 24 | flat |
| L | GDIP3-T24 or CDIP4-T24 | 24 | dual-in-line |
| 3 | CQCC1-N28 | 28 | square chip carrier |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

| | |
|---|---|
| Supply voltage range | -0.5 V dc to +7.0 V dc |
| DC input voltage ( $\overline{G}$ , $\overline{RD}$ , $\overline{EN}$ , CLK and T / $\overline{C}$ ) | +7.0 V dc |
| Voltage applied to D and to disabled three-state outputs | +5.5 V dc |
| Storage temperature range | -65°C to +150°C |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) | See MIL-STD-1835 |
| Maximum power dissipation ($P_D$) 1/ | 467.5 mW |
| Junction temperature ($T_J$) | +175°C |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Minimum high level input voltage ($V_{IH}$) : | |
| $\overline{G}$ and $\overline{RD}$ | +2.2 V dc |
| All others | +2.0 V dc |
| Maximum low level input voltage ($V_{IL}$) | 0.8 V dc |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

1/ Maximum power dissipation is defined as $V_{CC}$ x $I_{CC}$ and must withstand the added $P_D$ due to short-circuit output test, e.g., $I_O$

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$ 1/<br>unless otherwise specified | | | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Min | Max | |
| High level output voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V, $I_{OH}$ = -0.4 mA | | All outputs | 1, 2, 3 | 01 | 2.5 | | V |
| | | $V_{CC}$ = 4.5 V, $I_{OH}$ = -1.0 mA | | Qn outputs | | | 2.4 | | |
| Low level output voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 12 mA | Qn outputs | 1, 2, 3 | 01 | | 0.4 | V |
| | | | $I_{OL}$ = 4.0 mA | Dn outputs | | 01 | | 0.4 | |
| Input clamp voltage | $V_{IC}$ | $V_{CC}$ = 4.5 V, $I_{IC}$ = -18 mA | | | 1, 2, 3 | 01 | | -1.2 | V |
| Output current | $I_O$ | $V_{CC}$ = 5.5 V, $\overline{CLR}$ = 2.5 V<br>$V_{OUT}$ = 2.25 V 1/ | | | 1, 2, 3 | 01 | -20 | -112 | mA |
| Off-state output current | $I_{OZH}$ | $V_{CC}$ = 5.5 V, $V_{OUT}$ = 2.7 V | | | 1, 2, 3 | 01 | | 20 | µA |
| | $I_{OZL}$ | $V_{CC}$ = 5.5 V, $V_{OUT}$ = 0.4 V | | | 1, 2, 3 | 01 | | -20 | µA |
| High level input current | $I_{IH1}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 5.5 V | | Dn inputs | 1, 2, 3 | 01 | | 0.1 | mA |
| | | $V_{CC}$ = 5.5 V, $V_{IN}$ = 7.0 V | | All other inputs | | 01 | | 0.1 | |
| | $I_{IH2}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 2.7 V<br>2/ | | Dn inputs | 1, 2, 3 | 01 | | 20 | µA |
| | | | | All other inputs | | 01 | | 20 | |
| Low level input current | $I_{IL}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0.4 V<br>2/ | | Dn inputs | 1, 2, 3 | 01 | | -0.1 | mA |
| | | | | All other inputs | | 01 | | -0.1 | |
| Supply current | $I_{CC}$ | $V_{CC}$ = 5.5 V | | Outputs high | 1, 2, 3 | 01 | | 55 | mA |
| | | | | Outputs low | | 01 | | 85 | |
| | | | | Outputs disabled | | 01 | | 65 | |
| Maximum operating frequency | $f_{MAX}$ | $V_{CC}$ = 4.5 V to 5.5 V<br>$C_L$ = 50 pF<br>$R_L$ = 500 Ω<br>see figure 4 | | | 9, 10, 11 | 01 | 35 | | MHz |
| Setup time | $t_s$ | | | Data | 9, 10, 11 | 01 | 15 | | ns |
| | | | | $\overline{EN}$ low | | 01 | 10 | | |
| | | | | CLK high before $\overline{EN}$ ↑ | | 01 | 15 | | |
| | | | | $\overline{CLR}$ high (inactive) | | 01 | 10 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$ 1/<br>unless otherwise specified | | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Hold time | $t_h$ | $V_{CC}$ = 4.5 V to 5.5 V<br>$C_L$ = 50 pF<br>$R_L$ = 500 Ω<br>see figure 4 | Data | 9, 10, 11 | 01 | 1 | | ns |
| | | | $\overline{EN}$ low | | | 5 | | |
| | | | $\overline{RD}$ high | | | 5 | | |
| Pulse duration | $t_w$ | | $\overline{CLR}$ low | 9, 10, 11 | 01 | 10 | | ns |
| | | | CLK low | | | 14.5 | | |
| | | | CLK high | | | 14.5 | | |
| Propagation delay time, CLK to any Qn | $t_{PLH1}$ | | | 9, 10, 11 | 01 | 5 | 30 | ns |
| | $t_{PHL1}$ | | | | | 5 | 24 | |
| Propagation delay time, $\overline{CLR}$ to any Qn | $t_{PLH2}$ | | | 9, 10, 11 | 01 | 5 | 27 | ns |
| | $t_{PHL2}$ | | | | | 5 | 23 | |
| Propagation delay time, T / $\overline{C}$ to any Qn | $t_{PLH3}$ | | | 9, 10, 11 | 01 | 4 | 23 | ns |
| | $t_{PHL3}$ | | | | | 5 | 23 | |
| Propagation delay time, $\overline{CLR}$ to any Dn | $t_{PHL4}$ | | | 9, 10, 11 | 01 | 5 | 30 | ns |
| Output enable time, $\overline{RD}$ to any Dn | $t_{PZH1}$ | | | 9, 10, 11 | 01 | 2 | 18 | ns |
| | $t_{PZL1}$ | | | | | 2 | 18 | |
| Output disable time, $\overline{RD}$ to any Dn | $t_{PHZ1}$ | | | 9, 10, 11 | 01 | 1 | 19 | ns |
| | $t_{PLZ1}$ | | | | | 1 | 19 | |
| Output enable time, $\overline{EN}$ to any Dn | $t_{PZH2}$ | | | 9, 10, 11 | 01 | 2 | 17 | ns |
| | $t_{PZL2}$ | | | | | 2 | 17 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$ 1/<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| Output disable time, $\overline{EN}$ to any Dn | $t_{PHZ2}$ | | 9, 10, 11 | 01 | 1 | 19 | ns |
| | $t_{PLZ2}$ | | | | 1 | 19 | |
| Output enable time, $\overline{G}$ to Qn | $t_{PZH3}$ | | 9, 10, 11 | 01 | 2 | 15 | ns |
| | $t_{PZL3}$ | | | | 2 | 15 | |
| Output disable time, $\overline{G}$ to Qn | $t_{PHZ3}$ | | 9, 10, 11 | 01 | 1 | 11 | ns |
| | $t_{PLZ3}$ | | | | 1 | 11 | |

1/ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.
2/ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.

| Case outlines | L and K | 3 |
|---|---|---|
| Terminal number | Terminal symbol | |
| 1 | D1 | NC |
| 2 | D2 | D1 |
| 3 | D3 | D2 |
| 4 | D4 | D3 |
| 5 | D5 | D4 |
| 6 | D6 | D5 |
| 7 | D7 | D6 |
| 8 | D8 | NC |
| 9 | $\overline{EN}$ | D7 |
| 10 | $\overline{RD}$ | D8 |
| 11 | CLK | $\overline{EN}$ |
| 12 | GND | $\overline{RD}$ |
| 13 | $\overline{CLR}$ | CLK |
| 14 | T / $\overline{C}$ | GND |
| 15 | $\overline{G}$ | NC |
| 16 | Q8 | $\overline{CLR}$ |
| 17 | Q7 | T / $\overline{C}$ |
| 18 | Q6 | $\overline{G}$ |
| 19 | Q5 | Q8 |
| 20 | Q4 | Q7 |
| 21 | Q3 | Q6 |
| 22 | Q2 | NC |
| 23 | Q1 | Q5 |
| 24 | $V_{CC}$ | Q4 |
| 25 | - - - | Q3 |
| 26 | - - - | Q2 |
| 27 | - - - | Q1 |
| 28 | - - - | $V_{CC}$ |

NC = No internal connection

FIGURE 1. Terminal connections.

| Inputs | | | | | | | Output |
|---|---|---|---|---|---|---|---|
| $\overline{G}$ | T / $\overline{C}$ | $\overline{CLR}$ | $\overline{RD}$ | $\overline{EN}$ | CLK | Dn | Qn |
| H | X | X | X | X | X | X | Z |
| L | H | H | H | L | ↑ | X | D |
| L | X | H | L | L | X | Read back | D |
| L | X | L | X | X | X | X | L |
| L | X | H | L | H | H | Disable | $Q_O$ |
| L | L | H | H | L | ↑ | X | $\overline{D}$ |

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Transition from low to high
$Q_O$ = Q level before steady-state input conditions were established.

NOTE: Transitions on $\overline{EN}$ should only be made with CLK high in order to prevent false clocking.

FIGURE 2. Truth table.

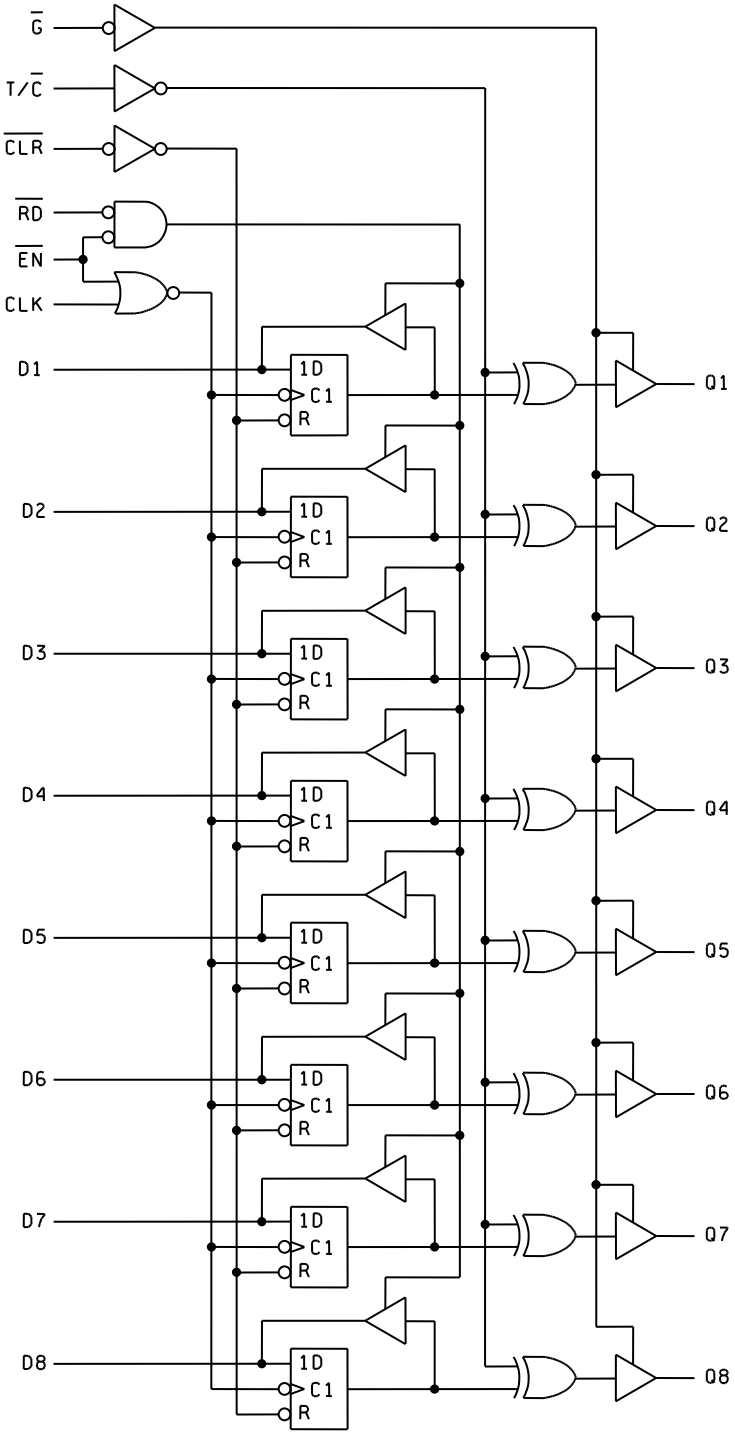



FIGURE 3. Logic diagram.

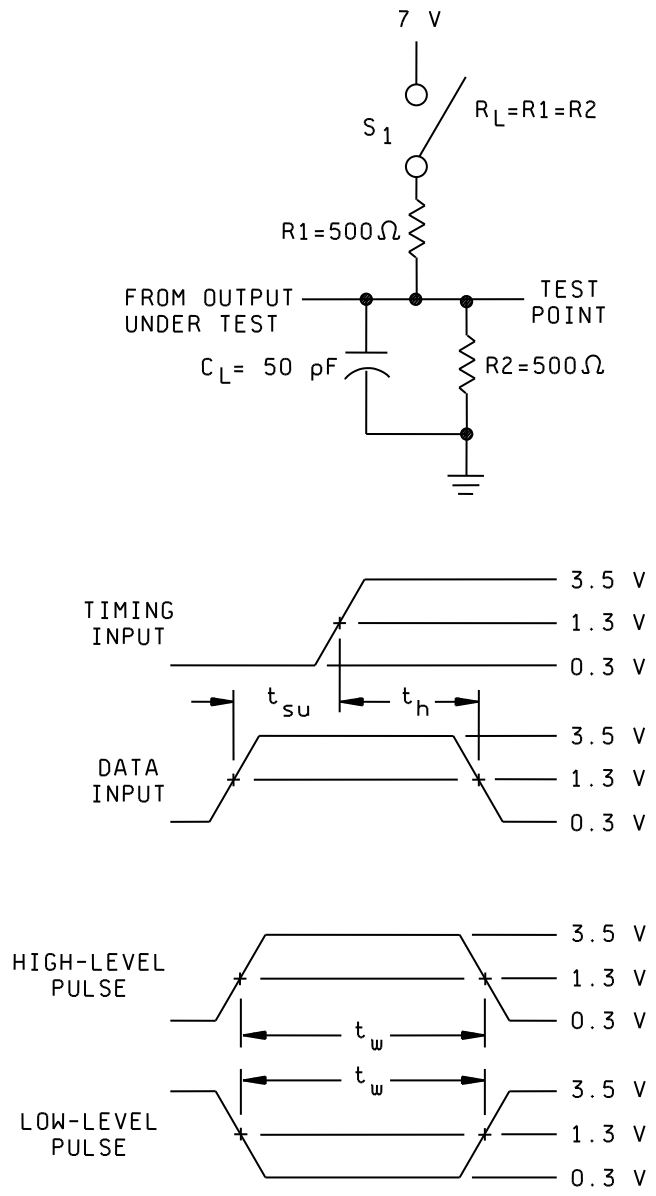
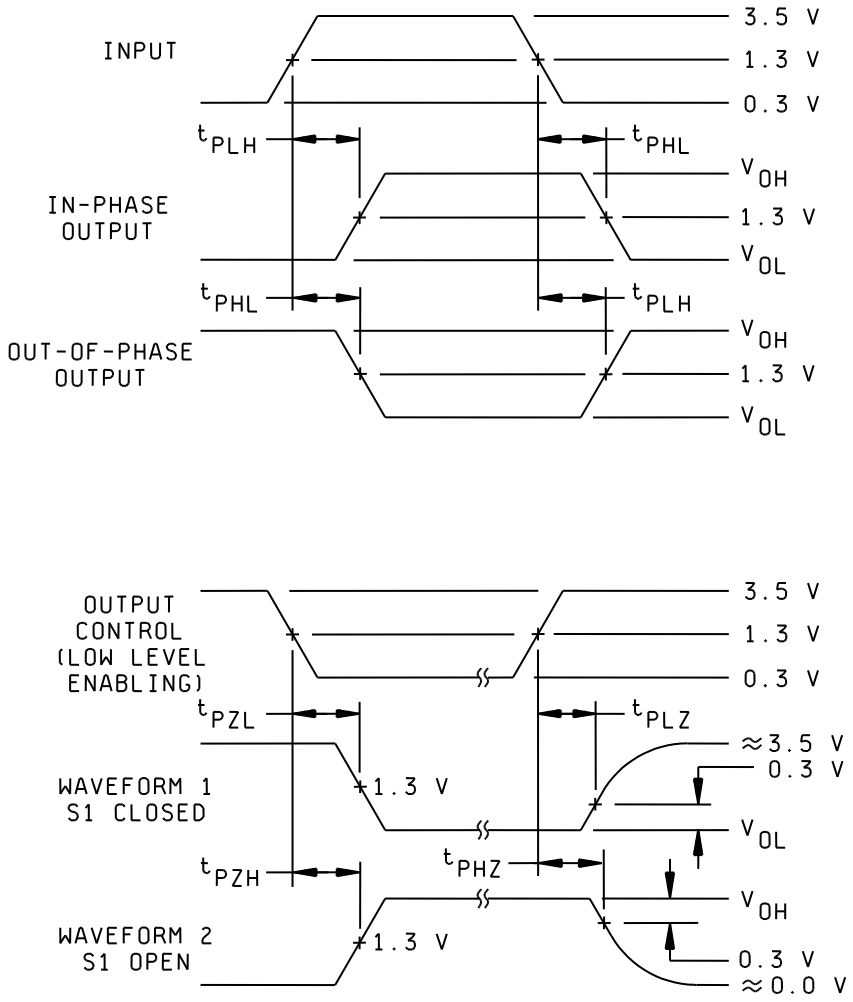



FIGURE 4. Test circuit and switching waveforms.




NOTES:

1. $C_L$ includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. When measuring propagation delay times of three-state outputs, switch S1 is open.
5. The output are measured one at a time with one input transition per measurement.
6. All input pulses have the following characteristics: PRR ≤ 10 MHz, duty cycle = 50 percent, $t_r = t_f = 3$ ns ± 1 ns.

FIGURE 4. Test circuit and switching waveforms - Continued.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | - - - |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 7, 8, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3 |

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-04-12

Approved sources of supply for SMD 5962-89945 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8994501KA | 3/ | SNJ54ALS996W |
| 5962-8994501LA | 01295 | SNJ54ALS996JT |
| 5962-89945013A | 01295 | SNJ54ALS996FK |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of Supply.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Lane<br>P.O. Box 660199<br>Dallas, TX 75243 |