

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 02 and 03. Technical and editorial changes throughout.	95-10-06	M. A. FRYE
B	Correct Figure 1 in regard to device types 02 and 03 for case outline 2. Change $V_{CC}$ to $V_S$ in Figure 2. Technical and editorial changes throughout. - lgt	98-03-27	R. MONNIN
C	Add class V for vendor CAGE 48726. Add table IIB. - rrp	99-11-04	R. MONNIN
D	Make change to the Initial accuracy test as specified in the Oscillator section in table I. - ro	01-03-20	R. MONNIN
E	Make correction to case outline E terminal connections for device types 02 and 03 as specified in figure 1. Add case outline 2 terminal connections for device type 01. - ro	02-06-04	R. MONNIN
F	Drawing updated to reflect current requirements. -rrp	09-04-20	J. RODENBECK
G	Make a correction to output source current test in Table I, move the -0.5 mA limit from the min column to the max column. - ro	10-10-18	C. SAFFLE
H	Make correction to footnote 1/ $V_S$ limit from 15 V to 12 V for device types 02 and 03 only as specified under table I. - ro	12-08-22	C. SAFFLE

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REV																		
SHEET																		
REV	H	H																
SHEET	15	16																
REV STATUS	REV		H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
OF SHEETS	SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14		

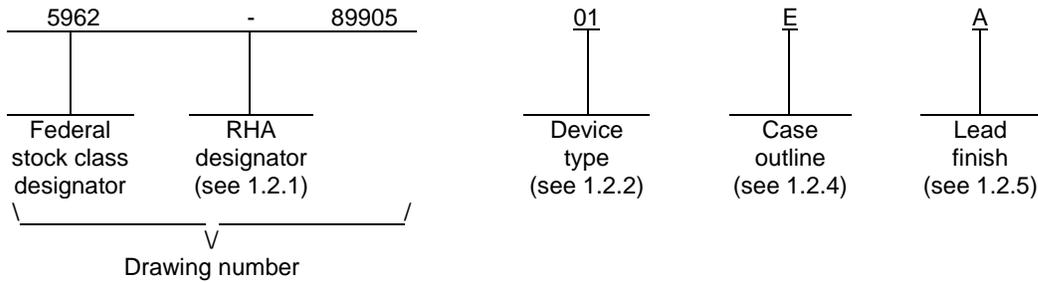
PMIC N/A	PREPARED BY JOSEPH A. KERBY	<b>DLA LAND AND MARITIME</b> <b>COLUMBUS, OHIO 43218-3990</b> <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a>															
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	CHECKED BY CHARLES E. BESORE																
	APPROVED BY MICHAEL A. FRYE	MICROCIRCUIT, LINEAR, HIGH SPEED PULSE WIDTH MODULATOR CONTROLLER, MONOLITHIC SILICON															
	DRAWING APPROVAL DATE 91-01-31																
	REVISION LEVEL H		SIZE A	CAGE CODE <b>67268</b>	<b>5962-89905</b>												
		SHEET 1 OF 16															

1. SCOPE

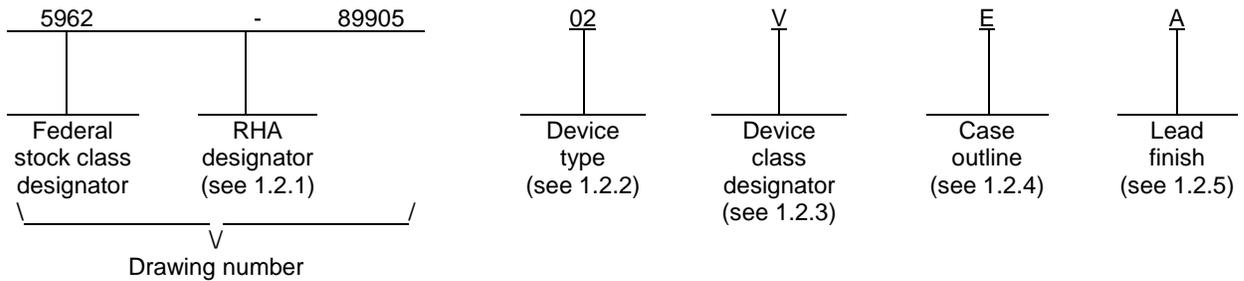
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device class M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	1823	High speed PWM controller
02	1823A	High speed PWM controller
03	1823B	High speed PWM controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

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1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. <sup>1/</sup>

Supply voltage (V <sub>S</sub> ) :	
Device type 01 .....	30 V dc
Device types 02 and 03 .....	22 V dc
DC output current, source or sink .....	0.5 A
Pulse output current, sink or source (0.5 μs)	
Device type 01 .....	2.0 A
Device types 02 and 03 .....	2.2 A
Analog input voltage :	
Device type 01 (pins INV, NINV, RAMP, S/S, and I <sub>LSD</sub> ) .....	-0.3 V dc to 6.0 V dc
Device types 02 and 03 (pins INV, NINV, and RAMP) .....	-0.3 V dc to 7.0 V dc
Device types 02 and 03 (pins S/S and I <sub>LSD</sub> ) .....	-0.3 V dc to 6.0 V dc
Clock output current .....	-5.0 mA
Error amplifier output current .....	5.0 mA
Soft start sink current .....	20 mA
Oscillator charging current .....	-5.0 mA
Power dissipation (P <sub>D</sub> ) <sup>2/ 3/</sup> .....	1.0 W
Storage temperature range .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+300°C
Junction temperature (T <sub>J</sub> ) .....	+150°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ) .....	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ <sub>JA</sub> ) :	
Case outline E .....	80°C/W
Case outline 2 .....	70°C/W
Power ground :	
Device types 02 and 03 .....	± 0.2 V

1.4 Recommended operating conditions.

Supply voltage (V <sub>S</sub> ) .....	10 V dc to 30 V dc
Ambient operating temperature range (T <sub>A</sub> ) .....	-55°C to +125°C

<sup>1/</sup> Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

<sup>2/</sup> For case E, derate linearly above T<sub>A</sub> = +60°C at 11 mW/°C. For case 2, derate linearly above T<sub>A</sub> = +40°C at 9 mW/°C.

<sup>3/</sup> Must withstand the added P<sub>D</sub> due to short circuit test; e.g., I<sub>SC</sub>.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagrams. The block diagrams shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reference section							
Output voltage	V <sub>REF</sub>	T <sub>J</sub> = +25°C, I <sub>O</sub> = 1.0 mA	1	All	5.05	5.15	V
Line regulation	V <sub>RLN</sub>	10 V < V <sub>S</sub> < 30 V	1, 2, 3	01		±20	mV
		12 V < V <sub>S</sub> < 20 V		02, 03		±15	
Load regulation	V <sub>RLD</sub>	1.0 mA < I <sub>O</sub> < 10 mA	1, 2, 3	All		±20	mV
Long term stability 2/	ΔV <sub>REF</sub> / Δt	T <sub>J</sub> = +125°C, t = 1000 hours	2	All		±25	mV
Output noise voltage 2/	N <sub>O</sub>	10 Hz < f < 10 kHz, T <sub>A</sub> = +25°C	1	All		200	μV
Total output variation 2/	V <sub>OM1</sub>	I <sub>O</sub> = -1.0 mA, V <sub>S</sub> = 10 V	1, 2, 3	All	5.00	5.20	V
	V <sub>OM2</sub>	I <sub>O</sub> = -1.0 mA, V <sub>S</sub> = 30 V			5.00	5.20	
	V <sub>OM3</sub>	I <sub>O</sub> = -10 mA, V <sub>S</sub> = 10 V			5.00	5.20	
	V <sub>OM4</sub>	I <sub>O</sub> = -10 mA, V <sub>S</sub> = 30 V			5.00	5.20	
Short circuit current	I <sub>SC</sub>	V <sub>REF</sub> = 0 V	1, 2, 3	01	-15	-100	mA
				02, 03	-30	-90	
Oscillator section							
Initial accuracy 2/	f <sub>O</sub>	T <sub>J</sub> = +25°C	4	01	360	440	kHz
				02, 03	375	425	
Voltage stability	Δf <sub>O</sub> / ΔV	10 V < V <sub>S</sub> < 30 V	4, 5, 6	01		±2.0	%
		12 V < V <sub>S</sub> < 20 V		02, 03		±1.0	
Total variation 2/	f <sub>OM1</sub>	V <sub>S</sub> = 10 V	4, 5, 6	01	340	460	kHz
				02, 03	350	450	
	f <sub>OM2</sub>	V <sub>S</sub> = 30 V		01	340	460	
				02, 03	350	450	
Clock out high	V <sub>CKH</sub>		1, 2, 3	01	3.9		V
				02, 03	3.7		
Clock out low	V <sub>CKL</sub>		1, 2, 3	ALL		2.9	V
Ramp voltage, peak 2/	V <sub>RP</sub>		1, 2, 3	ALL	2.6	3.0	V
Ramp voltage, valley 2/	V <sub>RV</sub>		1, 2, 3	ALL	0.7	1.25	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Oscillator section – continued							
Ramp voltage, valley <u>2/</u> to peak	V <sub>RVP</sub>		1, 2, 3	ALL	1.6	2.0	V
Oscillator discharge current	I <sub>OD</sub>	R <sub>T</sub> = open, V <sub>(CT)</sub> = 2.0 V	1, 2, 3	02, 03	9.0	11.0	V
Error amplifier section							
Input offset voltage	V <sub>IO</sub>	V <sub>CM</sub> = 3.0 V, V <sub>O</sub> = 3.0 V	1, 2, 3	ALL		±10	mV
Input bias current	I <sub>IS</sub>	V <sub>CM</sub> = 3.0 V, V <sub>O</sub> = 3.0 V	1, 2, 3	ALL		3.0	μA
Input offset current	I <sub>IO</sub>	V <sub>CM</sub> = 3.0 V, V <sub>O</sub> = 3.0 V	1, 2, 3	ALL		±1.0	μA
Open loop gain	A <sub>VOL</sub>	1.0 V < V <sub>O</sub> < 4.0 V	4, 5, 6	ALL	60		dB
Common mode rejection ratio	CMRR	1.5 V < V <sub>CM</sub> < 5.5 V, V <sub>OUT</sub> = 3.0 V	4, 5, 6	ALL	75		dB
Power supply rejection ratio	PSRR	10 V < V <sub>S</sub> < 30 V, V <sub>OUT</sub> = 3.0 V	4, 5, 6	01	85		dB
		12 V < V <sub>S</sub> < 20 V, V <sub>OUT</sub> = 3.0 V		02, 03	85		
Output sink current	I <sub>SNK</sub>	V <sub>E/A OUT</sub> = 1.0 V	1, 2, 3	ALL	1.0		mA
Output source current	I <sub>SRC</sub>	V <sub>E/A OUT</sub> = 4.0 V	1, 2, 3	ALL		-0.5	mA
Output high voltage	V <sub>OH1</sub>	I <sub>E/A OUT</sub> = -0.5 mA	1, 2, 3	01	4.0	5.0	V
				02, 03	4.5	5.0	
Output low voltage	V <sub>OL1</sub>	I <sub>E/A OUT</sub> = 1.0 mA	1, 2, 3	ALL	0	1.0	V
Unity gain bandwidth <u>2/</u>	BW	f = 200 kHz	4, 5, 6	01	3.0		MHz
				02, 03	6.0		
Slew rate <u>2/</u>	SR		4, 5, 6	ALL	6.0		V/μs

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
PWM comparator section							
RAMP bias current	I <sub>B</sub>	V <sub>RAMP</sub> = 0 V	1, 2, 3	01		-5.0	μA
				02, 03		-8.0	
Duty cycle range	DCRG		4, 5, 6	01	0	80	%
				02, 03	0	85	
E/A OUT zero dc threshold voltage	V <sub>TH</sub>	V <sub>RAMP</sub> = 0 V	1, 2, 3	ALL	1.1	1.4	V
Delay to output 2/	t <sub>DI</sub>		9, 10, 11	ALL		80	ns
Soft start duty cycle clamp section							
Charge current	I <sub>CHG</sub>	V <sub>S/S</sub> = 0.5 V	1, 2, 3	01	3.0	20	μA
		V <sub>S/S</sub> = 2.5 V		02, 03	8.0	20	
Discharge current	I <sub>DCG</sub>	V <sub>S/S</sub> = 1.0 V	1, 2, 3	01	1.0		mA
		V <sub>S/S</sub> = 2.5 V		02, 03	100	350	
Current limit / shutdown section							
I <sub>LSD</sub> pin bias current	I <sub>B</sub>	0 V < V(I <sub>LSD</sub> ) < 4.0 V	1, 2, 3	01		±10	μA
		0 V < V(I <sub>LSD</sub> ) < 2.0 V		02, 03		±15	
Current limit offset voltage	V <sub>LIM</sub>	V(LIMREF) = 1.1 V	1, 2, 3	01		15	mV
Shutdown threshold	V <sub>SDN</sub>		1, 2, 3	01	1.25	1.55	V
Current limit common mode range	I <sub>CMR</sub>		1, 2, 3	01	1.0	1.25	V
Delay to output 2/	t <sub>D2</sub>		9, 10, 11	ALL		80	ns
Output section							
Output low level	V <sub>OL2</sub>	I <sub>OUT</sub> = 20 mA	1, 2, 3	ALL		0.4	V
		I <sub>OUT</sub> = 200 mA				2.2	
Output high level	V <sub>OH2</sub>	I <sub>OUT</sub> = -20 mA	1, 2, 3	01	13.0		V
				02, 03		2.9	
		I <sub>OUT</sub> = -200 mA		01	12.0		
				02, 03		3.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output section – continued							
Collector leakage	I <sub>LC</sub>	V <sub>C</sub> = 30 V	1, 2, 3	01		500	μA
		V <sub>C</sub> = 20 V		02, 03		150	
Rise time <u>2/</u>	t <sub>r</sub>	C <sub>L</sub> = 1.0 nF	9, 10, 11	01		60	ns
				02, 03		45	
Fall time <u>2/</u>	t <sub>f</sub>	C <sub>L</sub> = 1.0 nF	9, 10, 11	01		60	ns
				02, 03		45	
UVLO output low saturation	V <sub>OLS</sub>	I <sub>O</sub> = 20 mA	1, 2, 3	02, 03		1.2	V
Under voltage lockout section							
Start threshold	V <sub>TH</sub>		1, 2, 3	01	8.8	9.6	V
				02	8.4	9.6	
				03		17	
Stop threshold	V <sub>STH</sub>		1, 2, 3	03	9.0		V
UVLO hysteresis	V <sub>hys</sub>		1, 2, 3	01, 02	0.4	1.2	V
				03	5.0	7.0	
Supply current							
Start-up current	I <sub>STR</sub>	V <sub>S</sub> = 8.0 V	1, 2, 3	01		2.5	mA
		V <sub>C</sub> = V <sub>CC</sub> = V <sub>TH</sub> (START) – 0.5 V		02, 03		0.3	
Supply current	I <sub>S</sub>	V(INV, RAMP, and ILS D) = 0 V, V <sub>NINV</sub> = 1.0 V	1, 2, 3	01		33	mA
				02, 03		36	

1/ Unless specified otherwise, characteristics apply at R<sub>T</sub> = 3.65 kΩ, C<sub>T</sub> = 1.0 nF, for device type 01, V<sub>S</sub> = 15 V and for device types 02 and 03, V<sub>S</sub> = 12 V.

2/ Guaranteed, if not tested, to the specified limits in table I herein.

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Device types	01	02, 03
Case outline	E	
Terminal number	Terminal symbol	
1	INVERTING INPUT (INV)	INVERTING INPUT (INV)
2	NONINVERTING INPUT (NINV)	NONINVERTING INPUT (NINV)
3	ERROR AMPLIFIER OUTPUT (E/A OUT)	ERROR AMPLIFIER OUTPUT (E/A OUT)
4	CLOCK	CLOCK / LEB
5	R <sub>T</sub>	R <sub>T</sub>
6	C <sub>T</sub>	C <sub>T</sub>
7	RAMP	RAMP
8	SOFT START (S/S)	SOFT START (S/S)
9	CURRENT LIMIT SHUT DOWN (I <sub>LSD</sub> )	CURRENT LIMIT (I <sub>LIM</sub> )
10	GROUND	GROUND
11	CURRENT LIMIT REFERENCE (I <sub>LIMREF</sub> )	OUTPUT A
12	POWER GROUND	POWER GROUND
13	V <sub>C</sub>	V <sub>C</sub>
14	OUTPUT	OUTPUT B
15	V <sub>S</sub>	V <sub>S</sub>
16	VOLTAGE REFERENCE 5.1 VOLTS	VOLTAGE REFERENCE 5.1 VOLTS

NC = No connection

FIGURE 1. Terminal connections.

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Device types	01	02, 03
Case outline	2	
Terminal number	Terminal symbol	
1	N/C	N/C
2	INVERTING INPUT (INV)	INVERTING INPUT (INV)
3	NONINVERTING INPUT (NINV)	NONINVERTING INPUT (NINV)
4	ERROR AMPLIFIER OUTPUT (E/A OUT)	ERROR AMPLIFIER OUTPUT (E/A OUT)
5	CLOCK	CLOCK / LEB
6	N/C	N/C
7	R <sub>T</sub>	R <sub>T</sub>
8	C <sub>T</sub>	C <sub>T</sub>
9	RAMP	RAMP
10	SOFT START (S/S)	SOFT START (S/S)
11	N/C	N/C
12	CURRENT LIMIT SHUT DOWN (I <sub>LSD</sub> )	CURRENT LIMIT (I <sub>LIM</sub> )
13	GROUND	GROUND
14	CURRENT LIMIT REFERENCE (I <sub>LIMREF</sub> )	OUTPUT A
15	POWER GROUND	POWER GROUND
16	N/C	N/C
17	V <sub>C</sub>	V <sub>C</sub>
18	OUTPUT	OUTPUT B
19	V <sub>S</sub>	V <sub>S</sub>
20	VOLTAGE REFERENCE 5.1 VOLTS	VOLTAGE REFERENCE 5.1 VOLTS

NC = No connection

FIGURE 1. Terminal connections – Continued.

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Device type 01

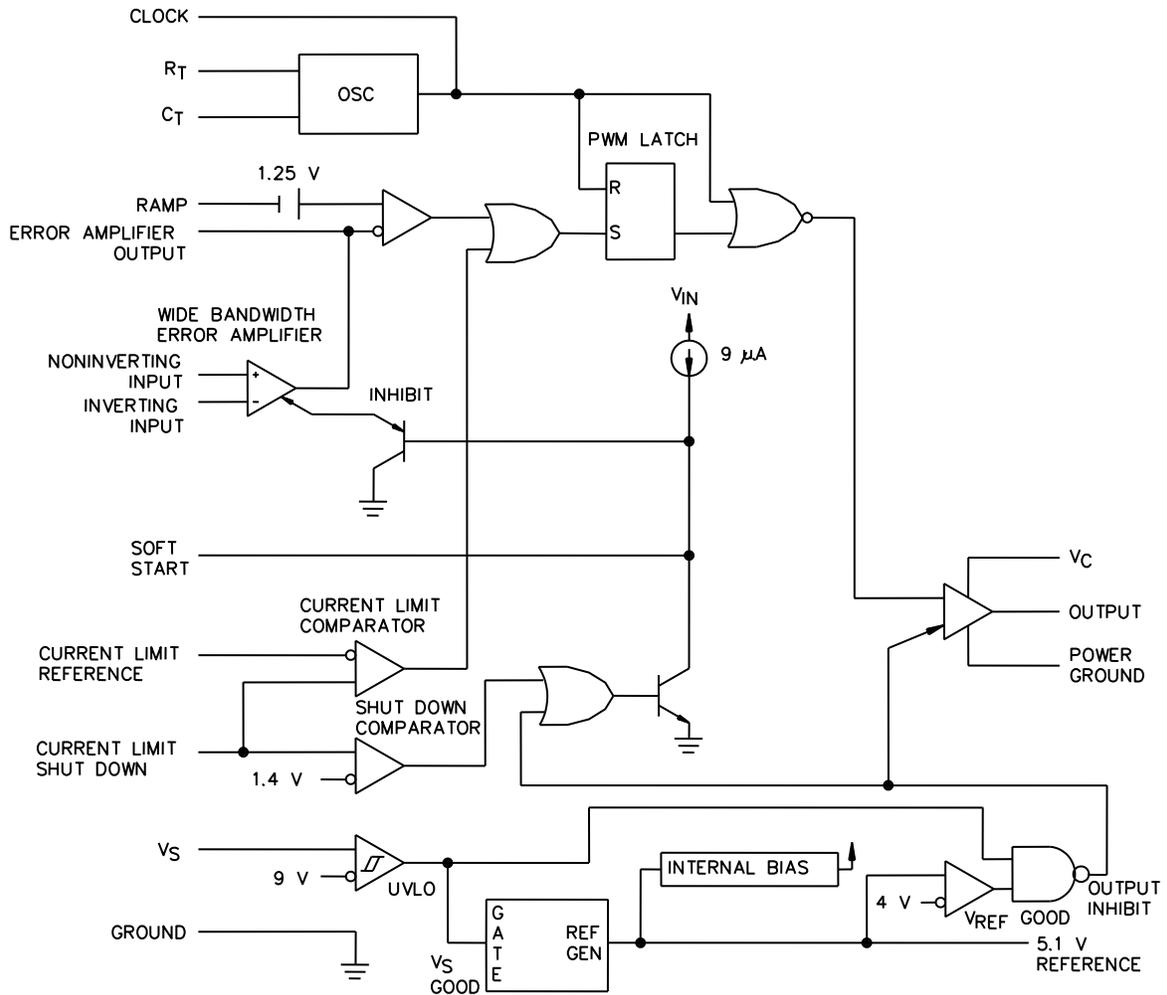


FIGURE 2. Block diagram.

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COLUMBUS, OHIO 43218-3990

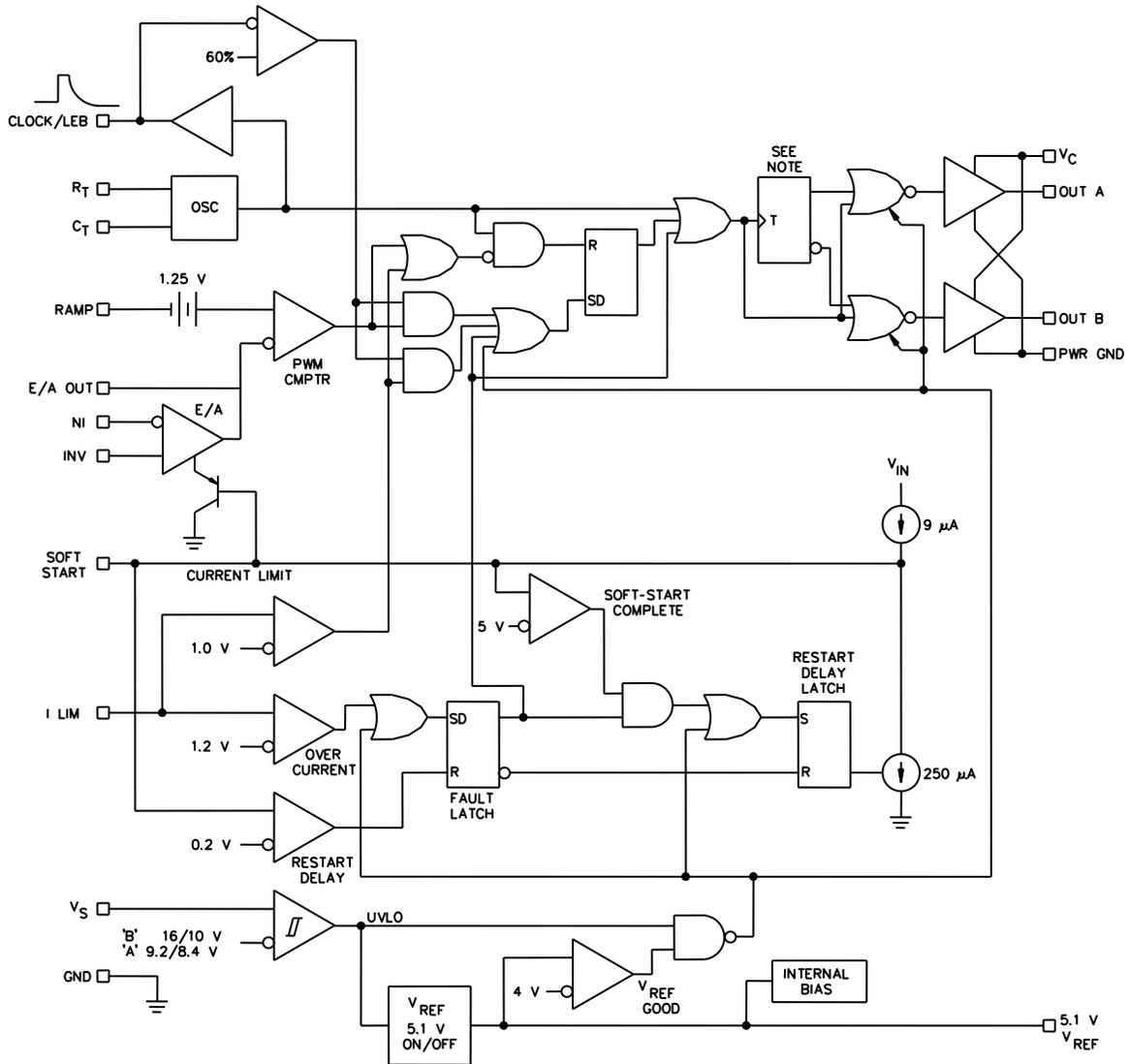
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**11**

Device types 02 and 03



NOTE: Device 02 and 03 toggles Q and  $\bar{Q}$  are always low.

FIGURE 2. Block diagram – Continued.

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3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 110 (see MIL-PRF-38535, appendix A).

#### 4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

##### 4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2)  $T_A = +125^{\circ}\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 4 <u>1/</u>	1, 2, 3, 4 <u>1/</u>	1,2,3,4 <u>1/ 2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, <u>3/</u> 9, 10, 11	1, 2, 3, 4, <u>3/</u> 5, 6, 9, 10, 11	1, 2, 3, <u>3/</u> 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3 <u>2/</u>
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	----	----	----

1/ PDA applies to subgroup 1.

2/ Delta limits in accordance with table IIB shall be computed with reference to the previous interim electrical parameters.

3/ Subgroups 9, 10, and 11, if not tested, shall be guaranteed to the limits specified in table I.

TABLE IIB. Burn-in and operating life test delta parameters. 1/ 2/

Parameter	Delta	Unit
Output voltage	±0.025	V
Output low saturation voltage	±0.2	V
Output high saturation voltage	±0.2	V
Supply current	±10	mA

1/ Deltas are performed at room temperature. T<sub>A</sub> = +25°C.

2/ 240 hour burn-in and 1,000 hour operating group C life test.

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4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b.  $T_A = +125^{\circ}\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table IIA herein.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

### 6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-08-22

Approved sources of supply for SMD 5962-89905 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8990501EA	01295	UC1823J883B
	<u>3/</u>	UC1823J/883BC
5962-89905012A	01295	UC1823L883B
	<u>3/</u>	UC1823L/883BC
5962-8990502EA	01295	UC1823AJ883B
	<u>3/</u>	UC1823AJ/883BC
5962-89905022A	01295	UC1823AL883B
	<u>3/</u>	UC1823AL/883BC
5962-8990502VEA	01295	UC1823AJQMLV
5962-8990503EA	<u>3/</u>	UC1823BJ883B
5962-89905032A	<u>3/</u>	UC1823BL883

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

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