

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes in 1.3 and figure 3. Editorial changes throughout.	90-08-08	W. Heckman
B	Changes in accordance with NOR 5962-R294-92.	92-09-02	Monica L. Poelking
C	Redrawn with changes. Update drawing to current requirements. Editorial changes throughout. - gap	07-08-14	Robert M. Heber

The original first sheet of this drawing has been replaced.

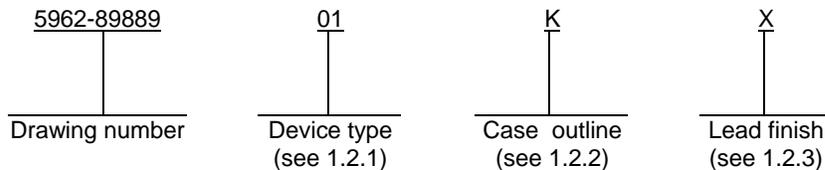
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REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A	PREPARED BY Larry T. Gauder	<p align="center"><b>DEFENSE SUPPLY CENTER COLUMBUS</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.dsccl.dla.mil">http://www.dsccl.dla.mil</a></p> <p align="center">MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED          LOW POWER SCHOTTKY TTL, DUAL 16-WORD          BY 4-BIT REGISTER FILES, MONOLITHIC          SILICON</p>																	
<p align="center"><b>STANDARD          MICROCIRCUIT          DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE          FOR USE BY ALL          DEPARTMENTS          AND AGENCIES OF THE          DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Tim H. Noh																		
	APPROVED BY William K. Heckman																		
	DRAWING APPROVAL DATE 89-08-28																		
	REVISION LEVEL C	SIZE A	CAGE CODE <b>67268</b>	<b>5962-89889</b>															
		SHEET 1 OF 14																	

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ALS870	Dual 16-word by 4-bit register files

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Leadless square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range .....	-0.5 V dc to +7.0 V dc
Input voltage:	
All inputs .....	-1.2 V dc at -18 mA to +7.0 V dc
I/O ports .....	-1.2 V dc at -18 mA to +5.5 V dc
Voltage applied to a disabled three state output .....	+5.5 V dc
Storage temperature range .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	See MIL-STD-1835
Maximum power dissipation ( $P_D$ ) <sup>1/</sup> .....	605 mW
Junction temperature ( $T_J$ ) .....	+175°C

<sup>1/</sup> Maximum power dissipation is defined as  $V_{CC} \times I_{CC}$ , and must withstand the added  $P_D$  due to short circuit test; e.g.,  $I_O$ .

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1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ ) .....	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage ( $V_{IH}$ ) .....	2.0 V dc
Maximum low level input voltage ( $V_{IL}$ ):	
$T_C = +125^\circ\text{C}$ .....	0.7 V dc
$T_C = -55^\circ\text{C}$ .....	0.8 V dc
$T_C = +25^\circ\text{C}$ .....	0.8 V dc
Maximum high level output current ( $I_{OH}$ ) .....	-1.0 mA
Maximum low level output current ( $I_{OL}$ ) .....	12 mA
Case operating temperature range ( $T_C$ ) .....	-55°C to +125°C
Width of WRITE pulse ( $t_P \bar{W}$ ) .....	12 ns minimum
Setup times ( $t_s$ ):	
Address before write going low .....	5 ns minimum
Data before write going high .....	15 ns minimum
Select before write going low .....	12 ns minimum
Hold times ( $t_h$ ):	
Address after write going high .....	0 ns minimum
Data after write going high .....	0 ns minimum
Select after write going high .....	12 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or [www.dodssp.daps.mil](http://www.dodssp.daps.mil) or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified 1/			Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, V <sub>IH</sub> = 2.0 V 2/	I <sub>OH</sub> = -0.4 mA	V <sub>IL</sub> = 0.8 V	1, 3	2.5		V
				V <sub>IL</sub> = 0.7 V	2	2.5		
			I <sub>OH</sub> = -1.0 mA	V <sub>IL</sub> = 0.8 V	1, 3	2.4		
				V <sub>IL</sub> = 0.7 V	2	2.4		
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, V <sub>IH</sub> = 2.0 V, I <sub>OL</sub> = 12 mA 2/	V <sub>IL</sub> = 0.8 V	1, 3		0.5	V	
			V <sub>IL</sub> = 0.7 V	2		0.5		
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA			1, 2, 3		-1.2	V
High level input current	I <sub>IH1</sub>	V <sub>CC</sub> = 5.5 V	V <sub>IN</sub> = 7.0 V	Control inputs	1, 2, 3		100	μA
			V <sub>IN</sub> = 5.5 V	DQA and DQB ports			200	
			V <sub>IN</sub> = 2.7 V	1 $\bar{W}$ and 2 $\bar{W}$			20	
	Other control inputs					40		
	I <sub>IH2</sub>		DQA and DQB ports 3/			50		
Low level input current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V	Control inputs	1, 2, 3		-0.2	mA	
			DQA and DQB ports 3/			-0.2		
Output current	I <sub>O</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.25 V 4/			1, 2, 3	-20	-112	mA
Quiescent current	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V			1, 2, 3		110	mA
Functional tests		See 4.3.1c 5/			7, 8			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified 1/ 6/			Group A subgroups	Limits		Unit
						Min	Max	
Access time	t <sub>a</sub>	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω see figure 4 6/	V <sub>CC</sub> = 5.0 V	Any A to any DQ	9	1.5	18	ns
			V <sub>CC</sub> = 4.5 V to 5.5 V		10, 11	1.5	24	
			V <sub>CC</sub> = 5.0 V	S0 to DQA	9	1.5	14	
				S1 to DQB		1.5	14	
			V <sub>CC</sub> = 4.5 V to 5.5 V	S0 to DQA	10, 11	1.5	18	
				S1 to DQB		1.5	18	
Output disable time	t <sub>PHZ</sub>	V <sub>CC</sub> = 5.0 V	S2 to DQA	9	1.5	11	ns	
			S3 to DQB		1.5	11		
			V <sub>CC</sub> = 4.5 V to 5.5 V	S2 to DQA	10, 11	1.5		18
				S3 to DQB		1.5		18
	t <sub>PLZ</sub>	V <sub>CC</sub> = 5.0 V	S2 to DQA	9	1.5	11	ns	
			S3 to DQB		1.5	11		
V <sub>CC</sub> = 4.5 V to 5.5 V	S2 to DQA	10, 11	1.5	18				
	S3 to DQB		1.5	18				
Output enable time	t <sub>PZH</sub>	V <sub>CC</sub> = 5.0 V	S2 to DQA	9	1.5	14	ns	
			S3 to DQB		1.5	14		
			V <sub>CC</sub> = 4.5 V to 5.5 V	S2 to DQA	10, 11	1.5		20
				S3 to DQB		1.5		20
	t <sub>PZL</sub>	V <sub>CC</sub> = 5.0 V	S2 to DQA	9	1.5	14	ns	
			S3 to DQB		1.5	14		
V <sub>CC</sub> = 4.5 V to 5.5 V	S2 to DQA	10, 11	1.5	20				
	S3 to DQB		1.5	20				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified 1/			Group A subgroups	Limits		Unit
						Min	Max	
Propagation delay time	t <sub>PHL</sub>	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω see figure 4 6/	V <sub>CC</sub> = 5.0 V	W to DQ	9	3	20	ns
				DQA to DQB		3	22	
				DQB to DQA		3	22	
			V <sub>CC</sub> = 4.5 V to 5.5 V	W to DQ	10, 11	3	26	
				DQA to DQB		3	29	
				DQB to DQA		3	29	
Propagation delay time	t <sub>PLH</sub>		V <sub>CC</sub> = 5.0 V	W to DQ	9	3	20	ns
				DQA to DQB		3	22	
				DQB to DQA		3	22	
			V <sub>CC</sub> = 4.5 V to 5.5 V	W to DQ	10, 11	3	26	
				DQA to DQB		3	29	
				DQB to DQA		3	29	

- 1/ Unused inputs that do not directly control the pin under test must be put at ≥ 2.5 V or ≤ 0.4 V. No unused inputs shall exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.
- 2/ All outputs must be tested. In the case where only one input at V<sub>IL</sub> maximum or V<sub>IH</sub> minimum produces the proper state, the test must be performed with each input being selected as the V<sub>IL</sub> maximum or V<sub>IH</sub> minimum input.
- 3/ For I/O ports, the parameters I<sub>IH2</sub> and I<sub>IL</sub> include the off-state output current.
- 4/ The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit output current, I<sub>OS</sub>. Not more than one output will be tested at one time and duration of the test condition shall not exceed 1 second.
- 5/ Functional tests shall be conducted at input test conditions of GND ≤ V<sub>IL</sub> ≤ V<sub>OL</sub> and V<sub>OH</sub> ≤ V<sub>IH</sub> ≤ V<sub>CC</sub>.
- 6/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V

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Device type	01	
Case outlines	K and L	3
Terminal number	Terminal symbol	
1	S0	NC
2	1A0	S0
3	1A1	1A0
4	1A2	1A1
5	1A3	1A2
6	1 $\bar{W}$	1A3
7	S2	1 $\bar{W}$
8	DQA1	NC
9	DQA2	S2
10	DQA3	DQA1
11	DQA4	DQA2
12	GND	DQA3
13	DQB1	DQA4
14	DQB2	GND
15	DQB3	NC
16	DQB4	DQB1
17	S3	DQB2
18	2 $\bar{W}$	DQB3
19	2A0	DQB4
20	2A1	S3
21	2A2	2 $\bar{W}$
22	2A3	NC
23	S1	2A0
24	V <sub>CC</sub>	2A1
25		2A2
26		2A3
27		S1
28		V <sub>CC</sub>

NC = No internal connection

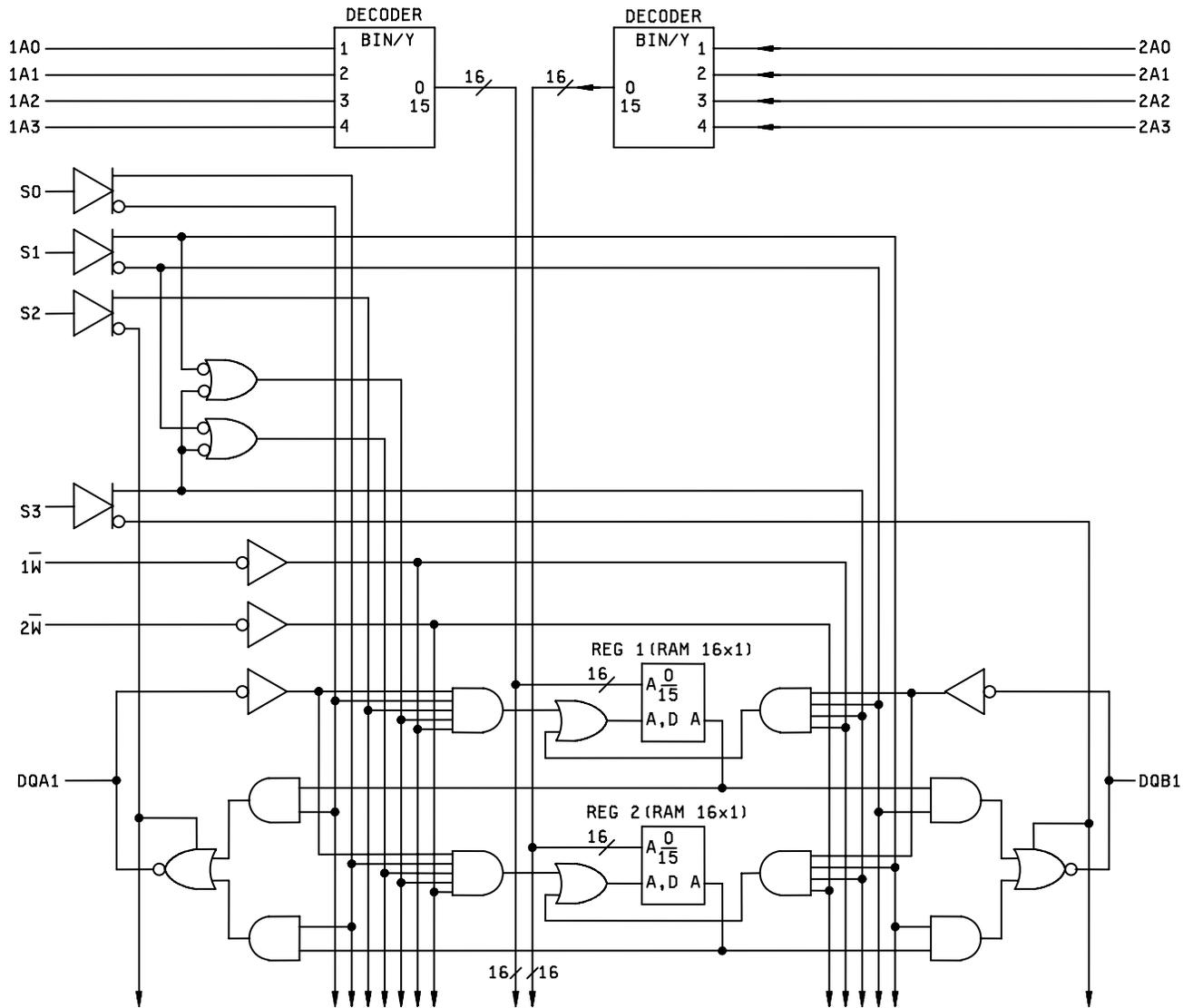
FIGURE 1. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-89889</b>
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File select			Input/Output		
S0	S1	File sel	S2	S3	I/O sel
L	L	REG1 TO A, REG1 TO B	L	L	A OUT, B OUT
H	L	REG2 TO A, REG1 TO B			
L	H	REG1 TO A, REG2 TO B			
H	H	REG2 TO A, REG2 TO B			
L	L	A TO REG1, REG1 TO B	H	L	A IN, B OUT
H	L	A TO REG2, REG1 TO B			
L	H	A TO REG1, REG2 TO B			
H	H	A TO REG2, REG2 TO B			
L	L	REG1 TO A, B TO REG1	L	H	A OUT, B IN
H	L	REG2 TO A, B TO REG1			
L	H	REG1 TO A, B TO REG2			
H	H	REG2 TO A, B TO REG2			
L	L	B TO REG1	H	H	A IN, B IN
H	L	A TO REG2, B TO REG1			
L	H	A TO REG1, B TO REG2			
H	H	B TO REG2			

FIGURE 2. Truth table.

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NOTE: THREE IDENTICAL CHANNELS NOT SHOWN

FIGURE 3. Logic diagram.

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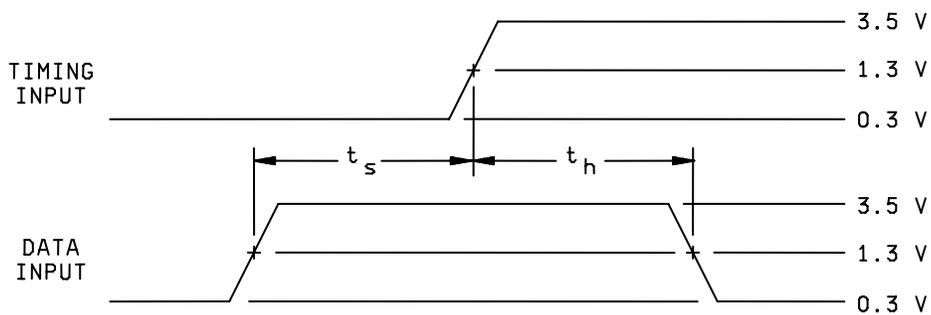
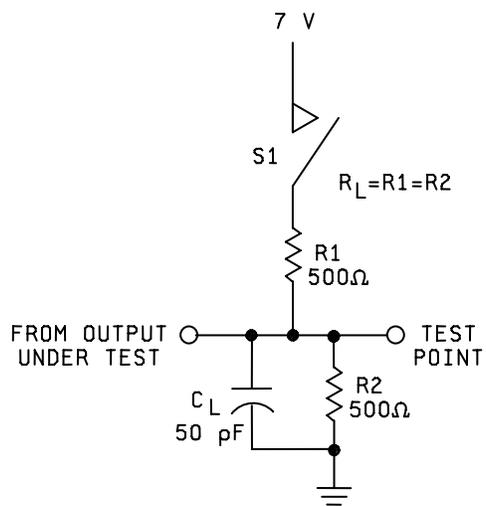
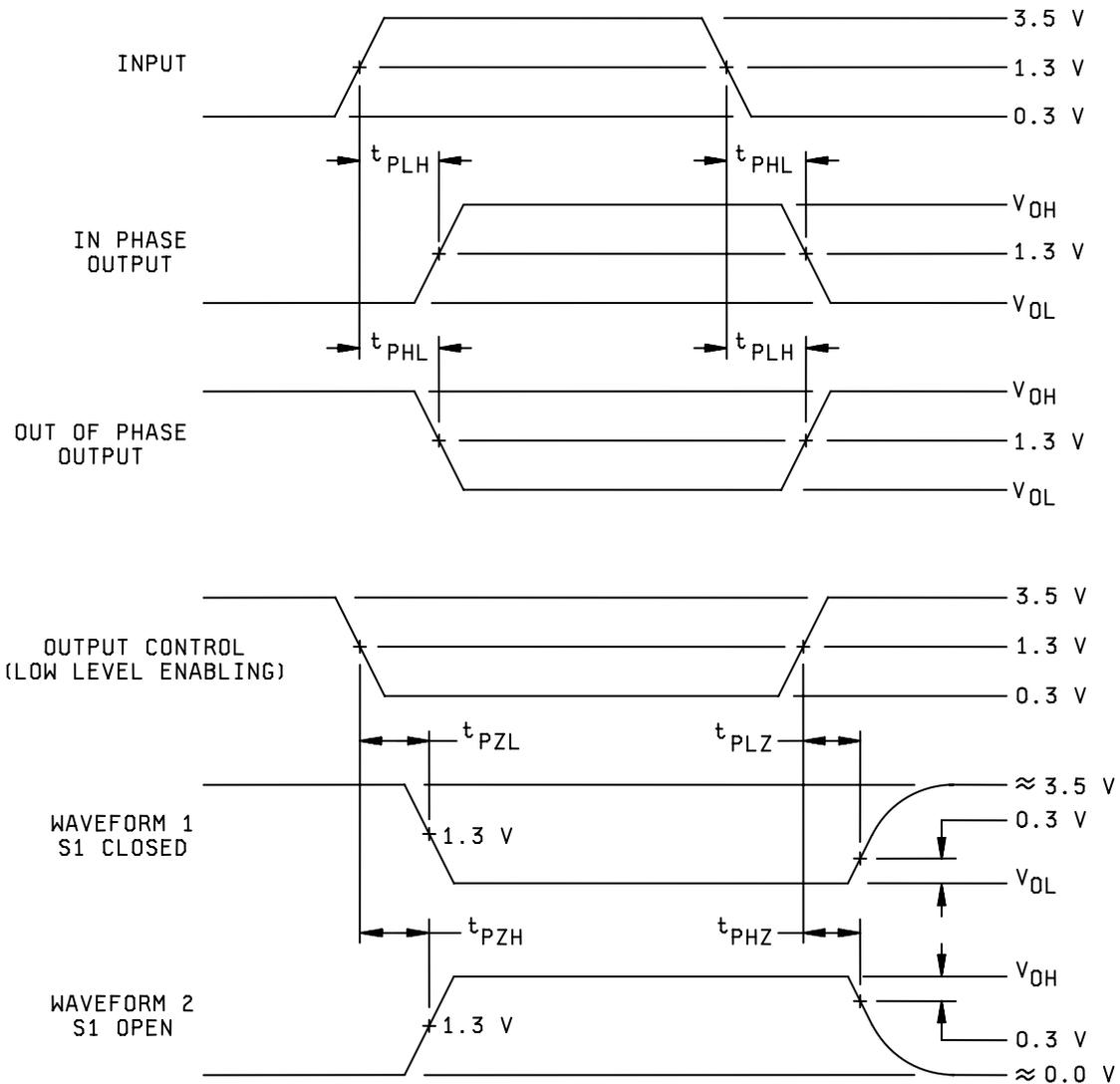


FIGURE 4. Test circuit and switching waveforms.

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NOTES:

1.  $C_L$  includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. When measuring propagation delay items of three-state outputs, switch S1 is open.
5. The outputs are measured one at a time with one input transition per measurement.
6. All input pulses have the following characteristics:  $PRR \leq 10$  MHz, duty cycle = 50 percent,  $t_r = t_f = 3$  ns  $\pm 1$  ns.

FIGURE 4. Test circuit and switching waveforms - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

\* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 shall include verification of the truth table.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-89889</b>
		REVISION LEVEL <b>C</b>	SHEET <b>14</b>

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-08-14

Approved sources of supply for SMD 5962-89889 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8988901KA	<u>3/</u>	SNJ54ALS870W
5962-8988901LA	<u>3/</u>	SNJ54ALS870JT
5962-89889013A	<u>3/</u>	SNJ54ALS870FK

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply. The last known source of supply is listed below.

Vendor CAGE  
number

Vendor name  
and address

01295

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
PO Box 660199  
Dallas, TX 75243

POC U.S. Highway 75 South  
P.O. Box 84, M/S 853  
Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.