

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. - jak	06-11-01	Thomas M. Hess
B	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	13-05-16	Thomas M. Hess
C	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - TTM	20-06-17	Muhammad A. Akbar

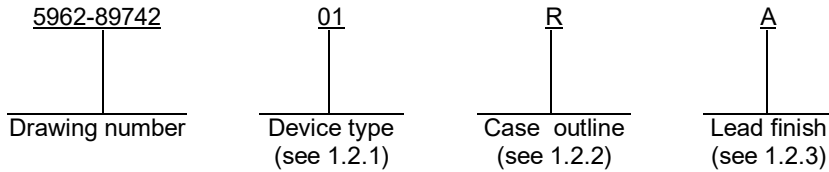


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PMIC N/A	PREPARED BY Wanda L. Meadows	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime</p>																		
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Thomas J. Ricciuti																			
	APPROVED BY Monica L. Poelking	<p>MICROCIRCUIT, DIGITAL, HIGH-SPEED CMOS, OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON</p>																		
	DRAWING APPROVAL DATE 93-03-05																			
	REVISION LEVEL C	<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-89742</td> </tr> <tr> <td colspan="2">SHEET</td> <td>1 OF 12</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-89742	SHEET		1 OF 12												
SIZE A	CAGE CODE 67268	5962-89742																		
SHEET		1 OF 12																		

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54HCT574	Octal D-type edge-triggered flip-flop with three-state outputs, TTL compatible inputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage range (V_{OUT})	-0.5 V dc to $V_{CC} + 0.5$ V dc
Input clamp current (I_{IK}) ($V_{IN} < 0.0$ V, $V_{IN} > V_{CC}$)	± 20 mA
Output clamp current (I_{OK}) ($V_{OUT} < 0.0$ V, $V_{OUT} > V_{CC}$)	± 20 mA
DC output current (I_{OUT}) ($V_{OUT} = 0.0$ V to V_{CC}) (per output pin)	± 35 mA
DC V_{CC} or GND current (I_{CC} , I_{GND}) (per pin)	± 70 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW 4/
Lead temperature (soldering, 10 seconds)	+265°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltages are referenced to ground.

3/ The limits for parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ For $T_C = +100^\circ\text{C}$ to +125°C, derate linearly at 8 mW/°C.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-89742
		REVISION LEVEL C	SHEET 2

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time (t_r , t_f) (0.1 V_{CC} to 0.9 V_{CC} or 0.9 V_{CC} to 0.1 V_{CC})	0 to 500 ns
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Maximum high level output current (I_{OH})	-6 mA
Maximum low level output current (I_{OL})	+6 mA

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD7 - Standard for Description of 54/74HCXXXXX and 54/74HCTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at <https://www.jedec.org/>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2/ Unless otherwise specified, all voltages are referenced to ground.

3/ The limits for parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-89742
		REVISION LEVEL C	SHEET 3

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-89742
		REVISION LEVEL C	SHEET 4

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Device type	V _{CC}	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage 3006	V _{OH1} 1/	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -20 μA	All	4.5 V	1, 2, 3	4.4		V
	V _{OH2} 1/	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -6.0 mA	All	4.5 V	1 2, 3	3.98 3.7		
Low level output voltage 3007	V _{OL1} 1/	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OL} = +20 μA	All	4.5 V	1, 2, 3		0.1	V
	V _{OL2} 1/	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OL} = +6.0 mA	All	4.5 V	1 2, 3		0.26 0.4	
Input current low 3009	I _{IL}	For input under test V _{IN} = GND For all other inputs V _{IN} = V _{CC} or GND	All	5.5 V	1		-0.1	μA
					2, 3		-1.0	
Input current high 3010	I _{IH}	For input under test V _{IN} = V _{CC} For all other inputs V _{IN} = V _{CC} or GND	All	5.5 V	1		0.1	μA
					2, 3		1.0	
Quiescent supply current, output three-state 3005	I _{CCZ}	\overline{OC} = GND For all other inputs V _{IN} = V _{CC} or GND	All	5.5 V	1		8	μA
					2, 3		160	
Quiescent supply current, output high 3005	I _{CCH}	For all inputs, V _{IN} = V _{CC} or GND	All	5.5 V	1		8	μA
					2, 3		160	
Quiescent supply current, output low 3005	I _{CCL}	For all inputs, V _{IN} = V _{CC} or GND	All	5.5 V	1		8	μA
					2, 3		160	
Additional quiescent supply current	ΔI _{CC} 2/	For input under test V _{IN} = 2.4 V or 0.5 V For all other inputs V _{IN} = V _{CC} or GND	All	5.5 V	1		2.4	mA
					2, 3		3.0	
Three-state output leakage current low 3020	I _{OZL}	\overline{OC} = 0.8 V or 2.0 V For all other inputs V _{IN} = V _{CC} or GND For output under test V _{OUT} = GND	All	5.5 V	1		-0.5	μA
					2, 3		-10.0	
Three-state output leakage current high 3021	I _{OZH}	\overline{OC} = 0.8 V or 2.0 V For all other inputs V _{IN} = V _{CC} or GND For output under test V _{OUT} = GND	All	5.5 V	1		0.5	μA
					2, 3		10.0	
Input capacitance 3012	C _{IN}	T _C = +25°C See 4.3.1c	All	GND	4		10	pF

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
C

5962-89742

SHEET
5

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Device type	V _{CC}	Group A subgroups	Limits		Unit	
						Min	Max		
Output three-state capacitance 3012	C _{OUT}	T _C = +25°C See 4.3.1c	All	5.5 V	4		20	pF	
Power dissipation capacitance	C _{PD} 3/	T _C = +25°C See 4.3.1c	All	5.0 V	4		93	pF	
Functional tests 3014		See 4.3.1d	All		7, 8				
Maximum clock frequency	f _{MAX} 2/	C _L = 50 pF minimum See figure 4	All	4.5 V	9	30		MHz	
Minimum high or low clock pulse width	t _w 2/		All	4.5 V	9	16		ns	
					10, 11	24			
Minimum high or low setup time, nD to CLK rising	t _{SU} 2/		All	4.5 V	9	12		ns	
					10, 11	18			
Minimum high or low hold time, nD from CLK rising	t _H 2/		All	4.5 V	9, 10, 11	5		ns	
Propagation delay time, CLK to nQ 3003	t _{PLH} , t _{PHL}	All	4.5 V	9		33	ns		
				10, 11		50			
Propagation delay time, output enable, $\overline{0C}$ to nQ 3003	t _{PZL} , t _{PZH}	C _L = 50 pF minimum R _L = 1 kΩ See figure 4	All	4.5 V	9		30	ns	
					10, 11		45		
Propagation delay time, output disable, $\overline{0C}$ to nQ 3003	t _{PLZ} , t _{PHZ}		All	4.5 V	9		28	ns	
					10, 11		42		
Output transition time, nQ 3003	t _{TLH} , t _{THL} 2/		C _L = 50 pF minimum See figure 4	All	4.5 V	9		12	ns
						10, 11		18	

1/ For power supply of 5 V ±10 percent, the worst case output voltages (V_{OH} and V_{OL}) occur for HCT at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst cases V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively.

2/ Guaranteed, if not tested, to the limits specified in table I.

3/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, P_D (total) = C_{PD} V_{CC}² f + (I_{CC} x V_{CC}) + n(ΔI_{CC} x V_{CC} x d), and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC} + n x d x ΔI_{CC}

Where:

P_D = dynamic power dissipation

C_{PD} = power dissipation capacitance of the device

f = input switching frequency

n = number of inputs

d = duty cycle

**STANDARD
MICROCIRCUIT DRAWING**

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-89742

REVISION LEVEL
C

SHEET
6

Device type	01
Case outlines	R and 2
Terminal number	Terminal symbol
1	$\overline{0C}$
2	1D
3	2D
4	3D
5	4D
6	5D
7	6D
8	7D
9	8D
10	GND
11	CLK
12	8Q
13	7Q
14	6Q
15	5Q
16	4Q
17	3Q
18	2Q
19	1Q
20	V_{CC}

Terminal symbol description	
Terminal symbol	Description
nD (n = 1 to 8)	Data inputs
$\overline{0C}$	Output enable control input (active low)
nQ (n = 1 to 8)	Outputs (non-inverting)
CLK	Clock pulse timing input (active rising edge)

FIGURE 1. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-89742
		REVISION LEVEL C	SHEET 7

Inputs			Outputs
\overline{OC}	CLK	nD	nQ
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

L = Low voltage level
 H = High voltage level
 X = Irrelevant
 Z = High impedance
 ↑ = Low-to-high clock transition.
 Q0 = Previous nQ before low-to-high transition of the clock

FIGURE 2. Truth table.

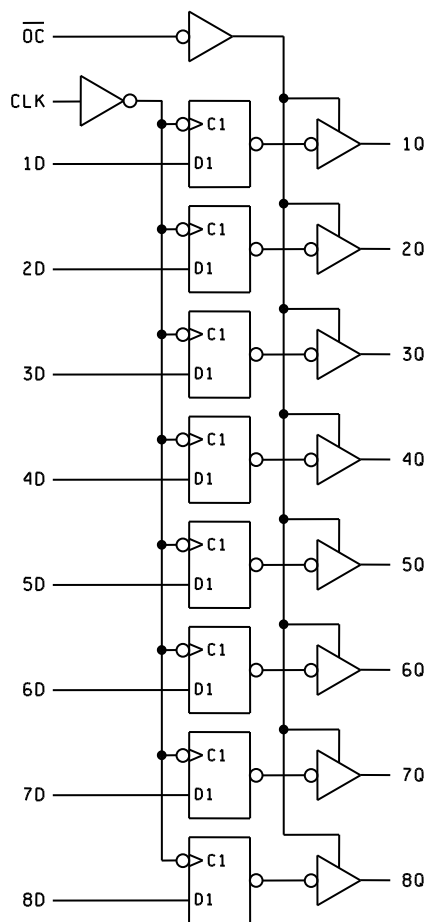


FIGURE 3. Logic diagram.

**STANDARD
MICROCIRCUIT DRAWING**

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-89742

REVISION LEVEL
C

SHEET
8

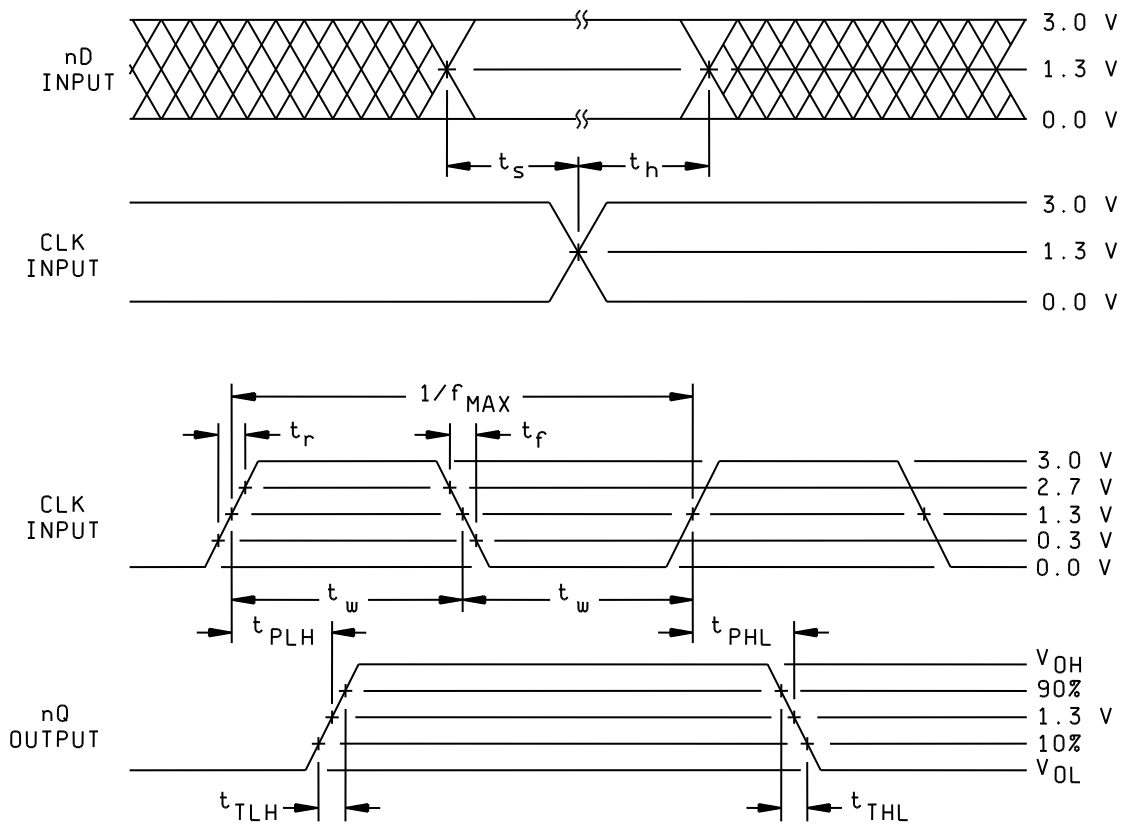


FIGURE 4. Switching waveforms and test circuit.

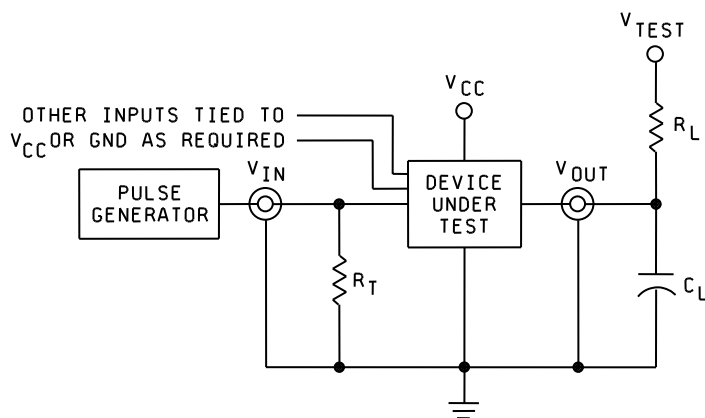
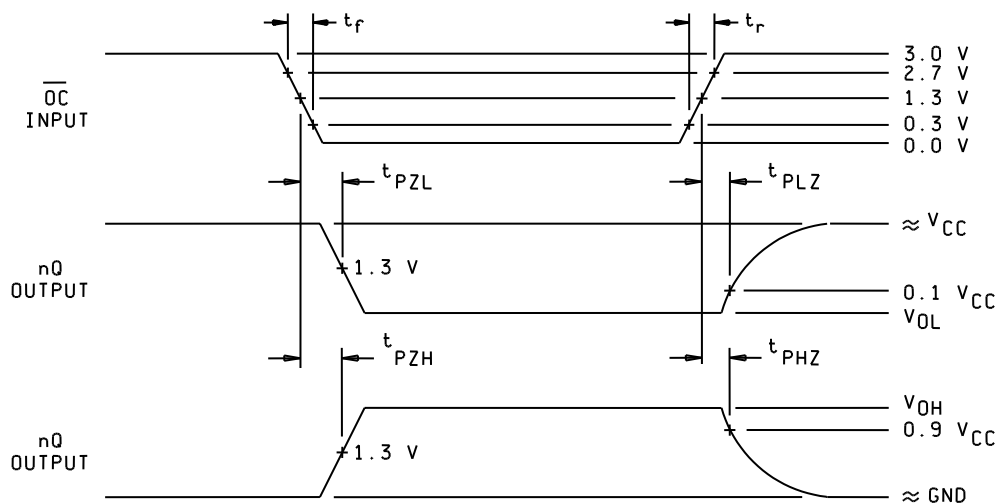
**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-89742

REVISION LEVEL
C

SHEET
9



NOTES:

1. When measuring t_{PHZ} and t_{PZH} : $V_{TEST} = GND$.
2. When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = V_{CC}$.
3. When measuring t_{PLH} , t_{PHL} , t_{TLH} , and t_{THL} : $V_{TEST} = Open$.
4. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
5. $C_L = 50$ pF minimum or equivalent (includes test jig and probe capacitance).
6. $R_L = 1$ k Ω or equivalent. $R_T = 50\Omega$ or equivalent.
7. Input signal from pulse generator: $V_{IN} = 0.0$ V to 3.0 V; $PRR \leq 1$ MHz; $t_r = 6.0$ ns; $t_f = 6.0$ ns; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit – Continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-89742
		REVISION LEVEL C	SHEET 10

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. C_{IN} , C_{OUT} , and C_{PD} , shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JESD7 and table I herein. For C_{IN} , C_{OUT} , and C_{PD} , test all applicable pins on five devices with zero failures.

d. Subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-89742
		REVISION LEVEL C	SHEET 11

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-89742
		REVISION LEVEL C	SHEET 12

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-06-17

Approved sources of supply for SMD 5962-89742 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8974201RA	01295	CD54HCT574F3A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

Vendor name
and address

01295

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The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.