

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. -ro	02-05-28	R. MONNIN
B	Update drawing as part of 5 year review. -rrp	09-05-18	J. RODENBECK
C	Update drawing to current MIL-PRF-38535 requirements. -rrp	15-07-21	C. SAFFLE
D	Drawing updated to current MIL-PRF-38535 requirements. -rrp	20-10-13	J. ESCHMEYER



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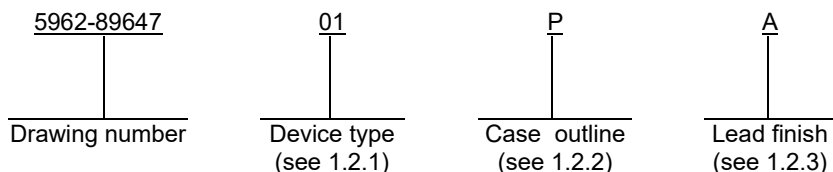
REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12				

PMIC N/A	PREPARED BY RICK C. OFFICER	<p align="center"><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="https://www.dla.mil/LandandMaritime">https://www.dla.mil/LandandMaritime</a></p>					
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY CHARLES E. BESORE						
	APPROVED BY MICHAEL A. FRYE						
	DRAWING APPROVAL DATE 93-01-19						
AMSC N/A	REVISION LEVEL D	SIZE A	CAGE CODE <b>67268</b>	<b>5962-89647</b>			
			SHEET		1 OF 12		

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	AD847S	High speed, low power, operational amplifier

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. (Unless otherwise specified, T<sub>A</sub> = +25°C)

Positive supply voltage (+V <sub>S</sub> ) .....	+18 V dc
Negative supply voltage (-V <sub>S</sub> ) .....	-18 V dc
Differential input voltage .....	±6.0 V dc
Input common mode voltage .....	±V <sub>S</sub>
Junction temperature (T <sub>J</sub> ) .....	+175°C
Storage temperature range .....	-65°C to +150°C
Power dissipation (P <sub>D</sub> ) .....	1.1 W <u>1/</u>
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ) .....	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ <sub>JA</sub> ) .....	110°C/W

1.4 Recommended operating conditions.

Positive supply voltage range (+V <sub>S</sub> ) .....	+4.5 V dc to +15 V dc
Negative supply voltage range (-V <sub>S</sub> ) .....	-4.5 V dc to -15 V dc
Common mode input voltage (V <sub>CM</sub> ) .....	±12 V dc
Ambient operating temperature range(T <sub>A</sub> ) .....	-55°C to +125°C

1/ Derate linearity above T<sub>A</sub> = +25°C at 7.3 mW/°C.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-89647</b>
		REVISION LEVEL <b>D</b>	SHEET <b>2</b>

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-89647</b>
		REVISION LEVEL <b>D</b>	SHEET <b>3</b>

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Input offset voltage	V <sub>IO</sub>	V <sub>CM</sub> = 0 V, V <sub>S</sub> = ±5 V	1	01		±1.0	mV
			2,3			±4.0	
Input bias current	+I <sub>IB</sub>	V <sub>CM</sub> = 0 V, V <sub>S</sub> = ±5 V, V <sub>S</sub> = ±15 V	1	01		+5.0	μA
			2,3			+7.5	
	-I <sub>IB</sub>		1			+5.0	
			2,3			+7.5	
Input offset current	I <sub>IO</sub>	V <sub>CM</sub> = 0 V, V <sub>S</sub> = ±5 V, ±15 V	1	01		±300	nA
			2,3			±400	
Common mode input voltage range <u>3/</u>	+IVR	V <sub>CM</sub> = +2.5 V, V <sub>S</sub> = ±5 V	1,2,3	01		+2.5	V
	-IVR	V <sub>CM</sub> = -2.5 V, V <sub>S</sub> = ±5 V				-2.5	
	+IVR	V <sub>CM</sub> = +12 V, V <sub>S</sub> = ±15 V				+12	
	-IVR	V <sub>CM</sub> = -12 V, V <sub>S</sub> = ±15 V				-12	
Open loop gain	+AVOL	V <sub>OUT</sub> = +2.5 V, V <sub>S</sub> = ±5 V, R <sub>L</sub> = 500 Ω	1	01	2.0		V/mV
			2,3		1.0		
		V <sub>OUT</sub> = +10 V, V <sub>S</sub> = ±15 V, R <sub>L</sub> = 1 kΩ	1		3.0		
			2,3		1.5		

See footnotes at end of table.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-89647**

REVISION LEVEL  
**D**

SHEET  
**4**

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Open loop gain	-AVOL	VOUT = -2.5 V, VS = ±5 V, RL = 500 Ω	1	01	2.0		V/mV
			2,3		1.0		
		VOUT = -10 V, VS = ±15 V, RL = 1 kΩ	1		3.0		
			2,3		1.5		
Common mode rejection ratio	+CMRR	VCM = +2.5 V, VS = ±5 V	1	01	80		dB
		VCM = +12 V, VS = ±15 V	1		80		
			2,3		75		
	-CMRR	VCM = -2.5 V, VS = ±5 V	1		80		
		VCM = -12 V, VS = ±15 V	1		80		
			2,3		75		
Output current <u>4/</u>	IOUT	VOUT = ±2.5 V, VS = ±5 V, TA = +25°C	4	01	13		mA
		VOUT = ±10 V, VS = ±15 V, TA = +25°C			20		
Output voltage swing	+VOUT	VS = ±5 V, RL = 500 Ω	1	01	+3.0		V
			2,3		+2.5		
		VS = ±5 V, RL = 150 Ω	1		+2.5		
		VS = ±15 V, RL = 1 kΩ	1,2,3		+12		
		VS = ±15 V, RL = 500 Ω	1		+10		

See footnotes at end of table.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**D**

**5962-89647**  
SHEET  
**5**

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Output voltage swing	-V <sub>OUT</sub>	V <sub>S</sub> = ±5 V, R <sub>L</sub> = 500 Ω	1	01	-3.0		V
			2,3		-2.5		
		V <sub>S</sub> = ±5 V, R <sub>L</sub> = 150 Ω	1		-2.5		
		V <sub>S</sub> = ±15 V, R <sub>L</sub> = 1 kΩ	1,2,3		-12		
		V <sub>S</sub> = ±15 V, R <sub>L</sub> = 500 Ω	1		-10		
Quiescent power supply current	I <sub>CC</sub>	V <sub>OUT</sub> = 0 V, I <sub>OUT</sub> = 0 mA, V <sub>S</sub> = ±5 V	1	01		5.7	mA
			2,3			7.8	
		V <sub>OUT</sub> = 0 V, I <sub>OUT</sub> = 0 mA, V <sub>S</sub> = ±15 V	1			6.3	
			2,3			8.4	
Power supply rejection ratio	PSRR	V <sub>S</sub> = ±5 V to ±15 V	1	01	75		dB
			2,3		72		
Quiescent power <u>5/</u> consumption	P <sub>Q</sub>	V <sub>OUT</sub> = 0 V, I <sub>OUT</sub> = 0 mA, V <sub>S</sub> = ±5 V	1	01		57	mW
			2,3			78	
		V <sub>OUT</sub> = 0 V, I <sub>OUT</sub> = 0 mA, V <sub>S</sub> = ±15 V	1			189	
			2,3			252	
Differential input <u>4/</u> resistance	R <sub>IN</sub>	V <sub>CM</sub> = 0 V, T <sub>A</sub> = +25°C, V <sub>S</sub> = ±5 V, ±15 V	4	01	80		kΩ

See footnotes at end of table.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-89647**

REVISION LEVEL  
**D**

SHEET  
**6**

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit			
					Min	Max				
Slew rate <u>4/ 6/</u>	+SR	VOUT = -2.5 V to +2.5 V, RL = 500 Ω, AV = 1 V/V, VS = ±5 V, measured from 10 % to 90 % point, rising edge	4	01	120		V/μs			
			5,6		90					
	-SR	VOUT = +2.5 V to -2.5 V, RL = 500 Ω, AV = 1 V/V, VS = ±5 V, measured from 90 % to 10 % point, falling edge	4		90					
			5,6		65					
	+SR	VOUT = -5 V to +5 V, RL = 1 kΩ, AV = 1 V/V, VS = ±15 V, measured from 10 % to 90 % point, rising edge	4		200					
			5,6		130					
	-SR	VOUT = +5 V to -5 V, RL = 1 kΩ, AV = 1 V/V, VS = ±15 V, measured from 90 % to 10 % point, falling edge	4		145					
			5,6		120					
	Gain bandwidth <u>4/</u> product	GBWP	VOUT = ±100 mV, RL = 500 Ω, VS = ±5 V, TA = +25°C		4	01		25		MHz
			VOUT = ±100 mV, RL = 1 kΩ, VS = ±15 V, TA = +25°C					40		
	Full power <u>4/ 7/</u> bandwidth	FPBW	VPK = 2.5 V, RL = 500 Ω, VS = ±5 V, TA = +25°C		4	01		5.7		MHz
			VPK = 10 V, RL = 1 kΩ, VS = ±15 V, TA = +25°C					2.8		
Closed loop stable <u>4/</u> gain	CLSG	VS = ±5 V, ±15 V, RL = 1 kΩ	4,5,6	01	1.0		V/V			

See footnotes at end of table.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-89647**

REVISION LEVEL  
**D**

SHEET  
**7**

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Rise time <u>4/ 8/</u>	t <sub>r</sub>	V <sub>OUT</sub> = 0 V to +200 mV, A <sub>V</sub> = +1, R <sub>L</sub> = 1 kΩ, V <sub>S</sub> = ±15 V	4,5,6	01		10	ns
Fall time <u>4/ 8/</u>	t <sub>f</sub>	V <sub>OUT</sub> = 0 V to -200 mV, A <sub>V</sub> = +1, R <sub>L</sub> = 1 kΩ, V <sub>S</sub> = ±15 V	4,5,6	01		10	ns
Settling time <u>4/</u>	t <sub>s</sub>	A <sub>V</sub> = -1 V/V, R <sub>L</sub> = 1 kΩ, V <sub>S</sub> = ±15 V, T <sub>A</sub> = +25°C, 10 V step at 0.1% of the fixed value	4	01		150	ns
		A <sub>V</sub> = -1 V/V, R <sub>L</sub> = 1 kΩ, V <sub>S</sub> = ±15 V, T <sub>A</sub> = +25°C, 10 V step at 0.01% of the fixed value				200	
Overshoot <u>4/</u>	+OS	V <sub>OUT</sub> = 0 V to +200 mV, A <sub>V</sub> = +1, R <sub>L</sub> = 1 kΩ, V <sub>S</sub> = ±15 V, T <sub>A</sub> = +25°C	4	01		30	%
	-OS	V <sub>OUT</sub> = 0 V to -200 mV, A <sub>V</sub> = +1, R <sub>L</sub> = 1 kΩ, V <sub>S</sub> = ±15 V, T <sub>A</sub> = +25°C				30	

- 1/ Unless otherwise specified, for dc tests, R<sub>S</sub> < 100 Ω, R<sub>L</sub> > 100 kΩ, V<sub>OUT</sub> = 0 V, and C<sub>L</sub> ≤ 10 pF.  
Unless otherwise specified, for ac tests, A<sub>V</sub> = ±1 V/V, R<sub>L</sub> = 1 kΩ, and C<sub>L</sub> ≤ 10 pF.
- 2/ The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only.  
Negative current shall be defined as conventional current flow out of a device terminal.
- 3/ This test is guaranteed by testing CMRR.
- 4/ If not tested, shall be guaranteed to the limits specified in table I herein.
- 5/ Quiescent power consumption is based on quiescent supply current test maximum (no load at the output).
- 6/ Slew rate test limits are guarantee after 5 minutes of warm-up.
- 7/ Full power bandwidth = SR / (2 × π × V<sub>PK</sub>).
- 8/ Rise and fall times measured between 10 percent and 90 percent point.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-89647**

REVISION LEVEL  
**D**

SHEET  
**8**



Device type	01
Case outline	P
Terminal number	Terminal symbol
1	NULL
2	-INPUT
3	+INPUT
4	-Vs
5	NC
6	OUTPUT
7	+Vs
8	NULL

NC = No connection

FIGURE 1. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-89647</b>
		REVISION LEVEL <b>D</b>	SHEET <b>9</b>

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2)  $T_A = +125^{\circ}\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-89647</b>
		REVISION LEVEL <b>D</b>	SHEET <b>10</b>

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

\* PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-89647</b>
		REVISION LEVEL D	SHEET <b>11</b>

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-89647</b>
		REVISION LEVEL D	SHEET <b>12</b>

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-10-13

Approved sources of supply for SMD 5962-89647 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8964701PA	24355	AD847SQ/883

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

24355

Vendor name and address

Analog Devices  
 Route 1 Industrial Park  
 P.O. Box 9106  
 Norwood, MA 02062  
 Point of contact: 804 Woburn Street  
 Wilmington, MA 01887-3462

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