

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with N.O.R. 5962-R035-93.	93-03-18	M. A. FRYE
B	Changes in accordance with N.O.R. 5962-R176-96.	94-01-03	M. A. FRYE
C	Drawing updated to reflect current requirements. -ro	01-04-11	R. MONNIN
D	Update drawing as part of 5-year review. -rrp	07-07-11	R. HEBER
E	Update to reflect latest changes in format and requirements. -rrp	12-12-04	C. SAFFLE
F	Update to meet current MIL-PRF-38535 requirements. - glg	18-09-13	C. SAFFLE



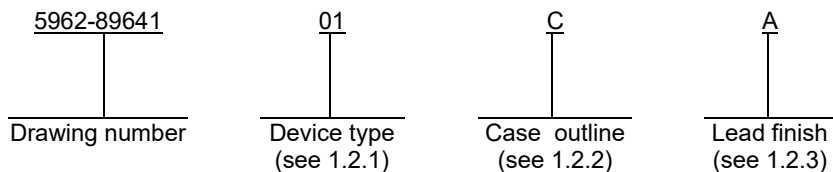
THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F					
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11								
PMIC N/A	PREPARED BY RICK C. OFFICER		<b>DLA LAND AND MARITIME</b> <b>COLUMBUS, OHIO 43218-3990</b> <a href="http://www.dla.mil/landandmaritime/">http://www.dla.mil/landandmaritime/</a>																	
<b>STANDARD MICROCIRCUIT DRAWING</b>	CHECKED BY CHARLES E. BESORE																			
	APPROVED BY MICHAEL A. FRYE																			
	DRAWING APPROVAL DATE 92-07-07																			
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE			MICROCIRCUIT, LINEAR, FAST SETTLING, UNITY-GAIN STABLE, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON																	
AMSC N/A	REVISION LEVEL F	SIZE A	CAGE CODE <b>67268</b>	<b>5962-89641</b>																
				SHEET 1 OF 11																

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	AD841	Unity-gain stable, fast settling operational amplifier

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
X	See figure 1	12	Can
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/ 2/

Voltage between +VS and -VS terminals .....	36 V dc
Differential input voltage .....	±6.0 V dc
Voltage at either input terminal .....	+VS and -VS
Peak output current (< 10 % duty cycle) .....	100 mA
Power dissipation (PD):	
Case C .....	1.3 W <u>3/</u>
Case X .....	1.5 W <u>3/</u>
Case 2 .....	1.0 W <u>3/</u>
Junction temperature (T <sub>J</sub> ) .....	+175°C
Storage temperature range .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ):	
Cases C and X .....	30°C/W
Case 2 .....	35°C/W
Thermal resistance, junction-to-case (θ <sub>JA</sub> ):	
Case C .....	110°C/W
Case X .....	100°C/W
Case 2 .....	150°C/W

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, T<sub>A</sub> = +25°C.

3/ Derate linearly above T<sub>A</sub> = +25°C for case C at 8.7mW/°C, case X at 10 mW/°C and case 2 at 6.7 mW/°C.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-89641</b>
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1.4 Recommended operating conditions.

Positive supply voltage range (+VS) ..... +5 V dc to +15 V dc  
Negative supply voltage range (-VS) ..... -5 V dc to -15 V dc  
Common mode input voltage (VCM) ..... ±10 V dc  
Load resistance (RL) ..... 500 Ω  
Ambient operating temperature range (TA) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil>).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ TA ≤ +125°C ±VS = ±15 V unless otherwise specified	Group A subgroups	Device type	Limits <sup>2/</sup>		Unit
					Min	Max	
Input offset voltage	V <sub>IO</sub>	V <sub>CM</sub> = 0 V	1	01	-2.0	+2.0	mV
			2,3		-5.5	+5.5	
Input bias current	+I <sub>B</sub>	V <sub>CM</sub> = 0 V	1	01		+8	μA
			2,3			+12	
	-I <sub>B</sub>		1			+8	
			2,3			+12	
Input offset current	I <sub>IO</sub>	V <sub>CM</sub> = 0 V	1	01	-0.4	+0.4	μA
			2,3		-0.6	+0.6	
Common mode voltage range	+V <sub>CM</sub>	+V <sub>S</sub> = 5.0 V, -V <sub>S</sub> = -25 V V <sub>OUT</sub> = -10 V	1,2,3	01	10		V
	-V <sub>CM</sub>	+V <sub>S</sub> = 25 V, -V <sub>S</sub> = -5 V V <sub>OUT</sub> = 10 V				-10	
Large signal voltage gain	+A <sub>VOL</sub>	V <sub>OUT</sub> = 0 V and 10 V, R <sub>L</sub> = 500 Ω	1	01	25		V/mV
			2,3		12		
	-A <sub>VOL</sub>		1		25		
			2,3		12		
Output current	+I <sub>OUT</sub>	V <sub>OUT</sub> = 0 V, T <sub>A</sub> = +25°C	1	01	50		mA
	-I <sub>OUT</sub>					-50	
Output voltage swing	+V <sub>OUT</sub>	R <sub>L</sub> = 500 Ω	1,2,3	01	10		V
	-V <sub>OUT</sub>					-10	
Quiescent power supply current	+I <sub>CC</sub>	V <sub>OUT</sub> = 0 V, I <sub>OUT</sub> = 0 mA	1	01		+12	mA
			2,3			+16	
	-I <sub>CC</sub>		1		-12		
			2,3		-16		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>A</sub> ≤ +125°C ±V <sub>S</sub> = ±15 V unless otherwise specified	Group A subgroups	Device type	Limits <sup>2/</sup>		Unit
					Min	Max	
Power supply rejection ratio	+PSRR	+V <sub>S</sub> = 5.0 V to 18 V, -V <sub>S</sub> = -15 V	1	01	86		dB
			2,3		80		
	-PSRR	-V <sub>S</sub> = -5.0 V to -18 V +V <sub>S</sub> = +15 V	1		86		
			2,3		80		
Quiescent power <sup>3/</sup> consumption	P <sub>C</sub>	V <sub>OUT</sub> = 0 V, I <sub>OUT</sub> = 0 mA	1	01		360	mW
			2,3			480	
Common mode rejection ratio	+CMRR	ΔV <sub>CM</sub> = 10 V, +V <sub>S</sub> = 5.0 V, -V <sub>S</sub> = -25 V, V <sub>OUT</sub> = -10 V	1	01	86		dB
			2,3		80		
	-CMRR	ΔV <sub>CM</sub> = -10 V, +V <sub>S</sub> = 25 V, -V <sub>S</sub> = -5 V, V <sub>OUT</sub> = 10 V	1		86		
			2,3		80		
Differential input <sup>4/</sup> resistance	R <sub>IN</sub>	V <sub>CM</sub> = 0 V, T <sub>A</sub> = +25°C	4	01	65		kΩ
Gain bandwidth <sup>4/</sup> product	GBWP	V <sub>OUT</sub> = ±100 mV, f <sub>1</sub> = 100 kHz, f <sub>2</sub> = 10 MHz, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = +25°C	4	01	23		MHz
Full power bandwidth <sup>4/ 5/</sup>	FPBW	V <sub>PK</sub> = 10 V, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = +25°C	4	01	3.1		MHz
Closed loop stable <sup>4/</sup> gain	CLSG	R <sub>L</sub> = 500 Ω, C <sub>L</sub> ≤ 10 pF	4,5,6	01	1		V/V
Slew rate <sup>4/</sup>	+SR	V <sub>OUT</sub> = -5.0 V to 5.0 V, measured from 10 % to 90 % point, R <sub>L</sub> = 500 Ω, A <sub>V</sub> = -1 V/V, rising edge	9	01	220		V/μs
			10,11		140		
	-SR		9		220		
			10,11		140		

See footnotes at end of table.

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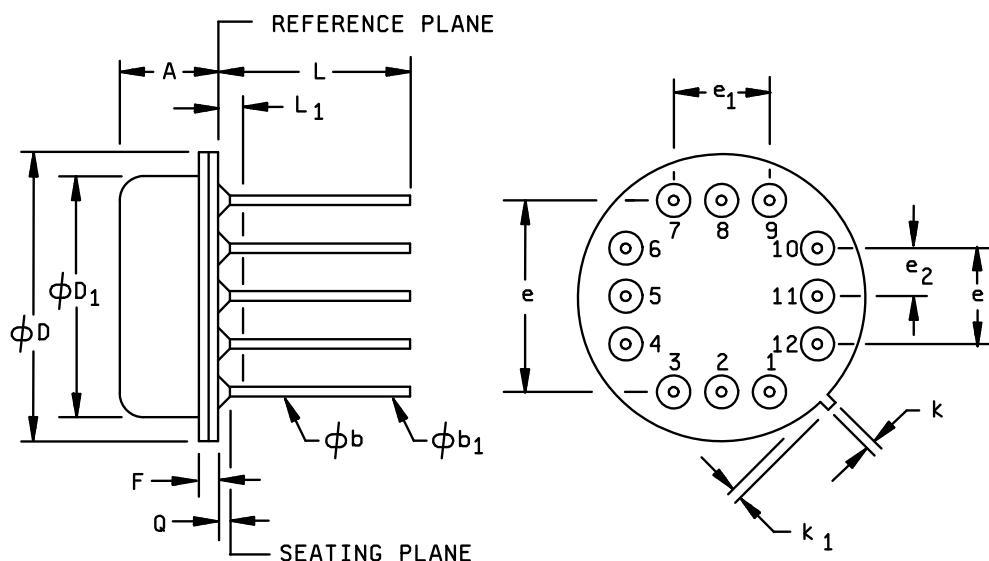
TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C ±VS = ±15 V unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Rise time <u>4/ 6/</u>	tR	VOUT = 0 V to +200 mV, AV = +1, RL = 500 Ω,	9,10,11	01		10	ns
Fall time <u>4/ 6/</u>	tF	VOUT = 0 V to -200 mV, AV = +1, RL = 500 Ω,	9,10,11	01		10	ns
Settling time <u>4/</u>	ts	AV = -1 V/V, RL = 500 Ω, 10 V step at 0.1 % of the fixed value, TA = +25°C	9	01		150	ns
		AV = -1 V/V, RL = 500 Ω, 10 V step at 0.01 % of the fixed value, TA = +25°C				200	
Overshoot <u>4/</u>	+OS	VOUT = 0 V to +200 mV, AV = +1, RL = 500 Ω, TA = +25°C	9	01		40	%
	-OS	VOUT = 0 V to -200 mV, AV = +1, RL = 500 Ω, TA = +25°C				40	

- 1/ Unless otherwise specified, for dc tests, RL = 100 kΩ and VOUT = 0 V.
- 2/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of device terminal.
- 3/ Quiescent power consumption is based on quiescent supply current test maximum with no load on outputs.
- 4/ If not tested, shall be guaranteed to the limits specified in table I herein.
- 5/ Full power bandwidth = SR / ( 2π x VPK ).
- 6/ Rise and fall times measured between 10 percent and 90 percent point.

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Case outline X



Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.148	.181	3.76	4.60	
$\phi b$	.016	.019	0.41	0.48	1
$\phi b_1$	.016	.021	0.41	0.53	1
$\phi D$	.592	.615	15.04	15.62	
$\phi D_1$	.545	.555	13.84	14.10	
e	.400 BSC		10.16 BSC		3
e1	.200 BSC		5.00 BSC		3
e2	.100 BSC		2.54 BSC		3
F	---	.040	---	1.02	
k	.026	.036	0.66	0.91	
k1	.027	.037	0.68	0.94	2
L	.375	---	9.50	---	
L1	---	.050	---	1.27	1
Q	.010	.045	0.25	1.14	

NOTES:

1. All leads  $\phi b$  applies between L and L1.  $\phi b_1$  applies between L1 and .375 inch (9.52 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter .019 inch (0.48 mm) measured in gauging plane .054 inch (1.37 mm) + .001 inch (0.03 mm) - .000 inch (0.000 mm) below the base plane of the product are within .007 inch (0.18 mm) of their true position relative to the maximum width tab.

FIGURE 1. Case outline.

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Device type	01		
Case outlines	C	X	2
Terminal number	Terminal symbol		
1	NC	NC	NC
2	NC	NC	BALANCE
3	BALANCE	BALANCE	NC
4	-INPUT	BALANCE	NC
5	+INPUT	-INPUT	-INPUT
6	-Vs	+INPUT	NC
7	NC	NC	+INPUT
8	NC	NC	NC
9	NC	NC	NC
10	OUTPUT	-Vs	-Vs
11	+Vs	OUTPUT	NC
12	BALANCE	+Vs	NC
13	NC	---	NC
14	NC	---	NC
15	---	---	OUTPUT
16	---	---	NC
17	---	---	+Vs
18	---	---	NC
19	---	---	NC
20	---	---	BALANCE

NC = No connection

FIGURE 2. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-89641</b>
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3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

#### 4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1,4
Final electrical test parameters (method 5004)	1*,2,3,4,
Group A test requirements (method 5005)	1,2,3,4**,5**,6**,9**,10**,11**
Groups C and D end-point electrical parameters (method 5005)	1

\* PDA applies to subgroup 1.

\*\* Subgroups 4, 5, 6, 9, 10, and 11, if not tested, shall be guaranteed to the limits specified in table I herein.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

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6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 18-09-13

Approved sources of supply for SMD 5962-89641 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8964101CA	<u>3/</u>	AD841SQ/883B
5962-8964101XA	<u>3/</u>	AD841SH/883B
5962-89641012A	24355	AD841SE/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number

24355

Vendor name and address

Analog Devices  
Route 1 Industrial Park  
P.O. Box 9106  
Norwood, MA 02062  
Point of contact: 804 Woburn Street  
Wilmington, MA 01887-3462

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