REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add notes and correct waveforms in figure 4, switching waveforms and test circuit. Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. – jak.	05-08-31	Thomas M. Hess
B	Update the boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. - MAA.	11-10-19	Thomas M. Hess

REV																				
SHEET																				
REV	B																			
SHEET	15																			

REV STATUS OF SHEETS		REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
		SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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Michael A. Frye

DRAWING APPROVAL DATE
89-07-07

REVISION LEVEL
B

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, DIGITAL, HIGH SPEED CMOS, 8-INPUT BINARY COUNTER WITH THREE-STATE OUTPUT REGISTERS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89603**

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89603	01	E	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC590A	8-input binary counter with three-state output registers

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) .... -0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}) .... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) .... -0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK}) .... ±20 mA
DC output current (per pin) (I_{OUT}) .... ±35 mA
DC V_{CC} or GND current (per pin) (I_{CC}, I_{GND}) .... ±70 mA
Storage temperature range (T_{STG}) .... -65°C to +150°C
Maximum power dissipation (P_D) 2/ .... 500 mW
Lead temperature (soldering, 10 seconds) .... +300°C
Thermal resistance, junction-to-case (θ_{JC}) .... See MIL-STD-1835
Junction temperature (T_J) .... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) .... +2.0 V dc to +6.0 V dc
Input voltage range (V_{IN}) .... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) .... +0.0 V dc to V_{CC}
Case operating temperature range (T_C) .... -55°C to +125°C
Input rise or fall time (t_r, t_f):
V_{CC} = 2.0 V .... 0 to 1000 ns
V_{CC} = 4.5 V .... 0 to 500 ns
V_{CC} = 6.0 V .... 0 to 400 ns

1/ Unless other wise specified, all voltages are referenced to ground.
2/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C.

1.4 Recommended operating conditions – Continued.

Minimum setup time, $\overline{CCKEN}$ low before CCK rising (t_{s1}):
T_C = +25°C:
V_{CC} = 2.0 V .... 100 ns
V_{CC} = 4.5 V .... 20 ns
V_{CC} = 6.0 V .... 17 ns
T_C = -55°C to +25°C:
V_{CC} = 2.0 V .... 150 ns
V_{CC} = 4.5 V .... 30 ns
V_{CC} = 6.0 V .... 26 ns

Minimum setup time, $\overline{CCLR}$ high (inactive) before CCK rising (t_{s2}):
T_C = +25°C:
V_{CC} = 2.0 V .... 100 ns
V_{CC} = 4.5 V .... 20 ns
V_{CC} = 6.0 V .... 17 ns
T_C = -55°C to +25°C:
V_{CC} = 2.0 V .... 150 ns
V_{CC} = 4.5 V .... 30 ns
V_{CC} = 6.0 V .... 26 ns

Minimum setup time, CCK rising before RCK rising (t_{s3}): 3/
T_C = +25°C:
V_{CC} = 2.0 V .... 100 ns
V_{CC} = 4.5 V .... 20 ns
V_{CC} = 6.0 V .... 17 ns
T_C = -55°C to +25°C:
V_{CC} = 2.0 V .... 150 ns
V_{CC} = 4.5 V .... 30 ns
V_{CC} = 6.0 V .... 26 ns

Minimum hold time, $\overline{CCKEN}$ low after CCK rising (t_h):
T_C = +25°C:
V_{CC} = 2.0 V .... 50 ns
V_{CC} = 4.5 V .... 10 ns
V_{CC} = 6.0 V .... 9 ns
T_C = -55°C to +25°C:
V_{CC} = 2.0 V .... 75 ns
V_{CC} = 4.5 V .... 15 ns
V_{CC} = 6.0 V .... 13 ns

Minimum pulse width, CCK or RCK high or low (t_{w1}):
T_C = +25°C:
V_{CC} = 2.0 V .... 125 ns
V_{CC} = 4.5 V .... 25 ns
V_{CC} = 6.0 V .... 21 ns
T_C = -55°C to +25°C:
V_{CC} = 2.0 V .... 200 ns
V_{CC} = 4.5 V .... 38 ns
V_{CC} = 6.0 V .... 32 ns

Minimum pulse width, $\overline{CCLR}$ low (t_{w2}):
T_C = +25°C:
V_{CC} = 2.0 V .... 100 ns
V_{CC} = 4.5 V .... 20 ns
V_{CC} = 6.0 V .... 17 ns
T_C = -55°C to +25°C:
V_{CC} = 2.0 V .... 150 ns
V_{CC} = 4.5 V .... 30 ns
V_{CC} = 6.0 V .... 26 ns

3/ This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register will be one clock pulse behind the counter.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	V_{CC}	Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -20\ \mu A$	2.0 V	1, 2, 3	1.9		V
			4.5 V		4.4		
			6.0 V		5.9		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -6.0$ mA for QA-QH $I_{OH} = -4.0$ mA for $\overline{RCO}$	4.5 V		3.7		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -7.8$ mA for QA-QH $I_{OH} = -5.2$ mA for $\overline{RCO}$	6.0 V		5.2		
Low level output voltage	V_{OL}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = 20\ \mu A$	2.0 V	1, 2, 3		0.1	V
			4.5 V			0.1	
			6.0 V			0.1	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = 6.0$ mA for QA-QH $I_{OL} = 4.0$ mA for $\overline{RCO}$	4.5 V			0.4	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = 7.8$ mA for QA-QH $I_{OL} = 5.2$ mA for $\overline{RCO}$	6.0 V			0.4	
High level input voltage	V_{IH}	2/	2.0 V	1, 2, 3	1.5		V
			4.5 V		3.15		
			6.0 V		4.2		
Low level input voltage	V_{IL}	2/	2.0 V	1, 2, 3		0.3	V
			4.5 V			0.9	
			6.0 V			1.2	
Input capacitance	C_{IN}	$T_C = +25°C$ $V_{IN} = 0$ V See 4.3.1c		4		10	pF
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0 V	1, 2, 3		160	µA
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0 V	1, 2, 3		±1	µA
Off-state output leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND $I_{OUT} = 0.0$ A	6.0 V	1, 2, 3		±10	µA
Functional tests		See 4.3.1d		7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	V_{CC}	Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay time, CCK rising to $\overline{RCO}$	t_{PHL1}, t_{PLH1}	C_L = 50 pF See figure 4	2.0 V	9		150	ns
			4.5 V			31	
			6.0 V			26	
			2.0 V	10, 11		225	ns
			4.5 V			45	
			6.0 V			38	
Propagation delay time, CCLR falling to $\overline{RCO}$	t_{PLH2}	C_L = 50 pF See figure 4	2.0 V	9		130	ns
			4.5 V			28	
			6.0 V			23	
			2.0 V	10, 11		195	ns
			4.5 V			39	
			6.0 V			33	
Propagation delay time, RCK rising to Qn	t_{PHL3}, t_{PLH3}	C_L = 50 pF See figure 4	2.0 V	9		140	ns
			4.5 V			31	
			6.0 V			25	
			2.0 V	10, 11		210	ns
			4.5 V			42	
			6.0 V			36	
Propagation delay time, output enable, $\overline{G}$ falling to Qn	t_{PZH}, t_{PZL}	C_L = 50 pF See figure 4	2.0 V	9		125	ns
			4.5 V			30	
			6.0 V			28	
			2.0 V	10, 11		185	ns
			4.5 V			37	
			6.0 V			31	
Propagation delay time, output disable, $\overline{G}$ rising to Qn	t_{PHZ}, t_{PLZ}	C_L = 50 pF See figure 4	2.0 V	9		125	ns
			4.5 V			30	
			6.0 V			28	
			2.0 V	10, 11		185	ns
			4.5 V			37	
			6.0 V			31	
Transition time, $\overline{RCO}$	t_{TLH1}, t_{THL1} 3/	C_L = 50 pF See figure 4	2.0 V	9		75	ns
			4.5 V			15	
			6.0 V			13	
			2.0 V	10, 11		110	ns
			4.5 V			22	
			6.0 V			19	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	V_{CC}	Group A subgroups	Limits		Unit
					Min	Max	
Transition time, Qn	t_{TLH2}, t_{THL2} 3/	C_L = 50 pF See figure 4	2.0 V	9		60	ns
			4.5 V			12	
			6.0 V			10	
			2.0 V	10, 11		90	ns
			4.5 V			18	
			6.0 V			15	
Maximum frequency, CCK or RCK	f_{MAX}	C_L = 50 pF See figure 4	2.0 V	9	4.0		MHz
			4.5 V		20		
			6.0 V		24		
			2.0 V	10, 11	2.5		MHz
			4.5 V		13		
			6.0 V		16		

1/ For power supply of 5 V ±10 percent, the worst case output voltages (V_{OH} and V_{OL}) occur for high-speed CMOS at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst cases V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively. The V_{IH} value at 5.5 V is 3.85 V. The worst case leakage currents (I_{IN}, I_{CC}, and I_{OZ}) occur for high-speed CMOS at the higher voltages so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 250 pF determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $P_D = C_{PD} V_{CC} f + I_{CC}$.

2/ V_{IH} and V_{IL} tests are not required and shall be applied as forcing functions for V_{OH} or V_{OL} tests.

3/ Transition times (t_{TLH}, t_{THL}), if not tested, shall be guaranteed to the specified limits in table I.

Device type	01	
Case outlines	E and F	2
Terminal number	Terminal symbol	
1	QB	NC
2	QC	QB
3	QD	QC
4	QE	QD
5	QF	QE
6	QG	NC
7	QH	QF
8	GND	QG
9	$\overline{RCO}$	QH
10	$\overline{CCLR}$	GND
11	CCK	NC
12	$\overline{CCKEN}$	$\overline{RCO}$
13	RCK	$\overline{CCLR}$
14	$\overline{G}$	CCK
15	QA	$\overline{CCKEN}$
16	V_{CC}	NC
17	- - -	RCK
18	- - -	$\overline{G}$
19	- - -	QA
20	- - -	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

Inputs					Operation
$\overline{G}$	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	RCK	
H	X	X	X	X	Disabled
L	L	X	X	↑	Clear
L	H	H	X	X	No change
L	H	L	↑	X	Internal count
L	H	L	↑	↑	External count

L = Low voltage level
H = High voltage level
X = Don't care
↑ = Clock transition from low to high

FIGURE 2. Truth table.

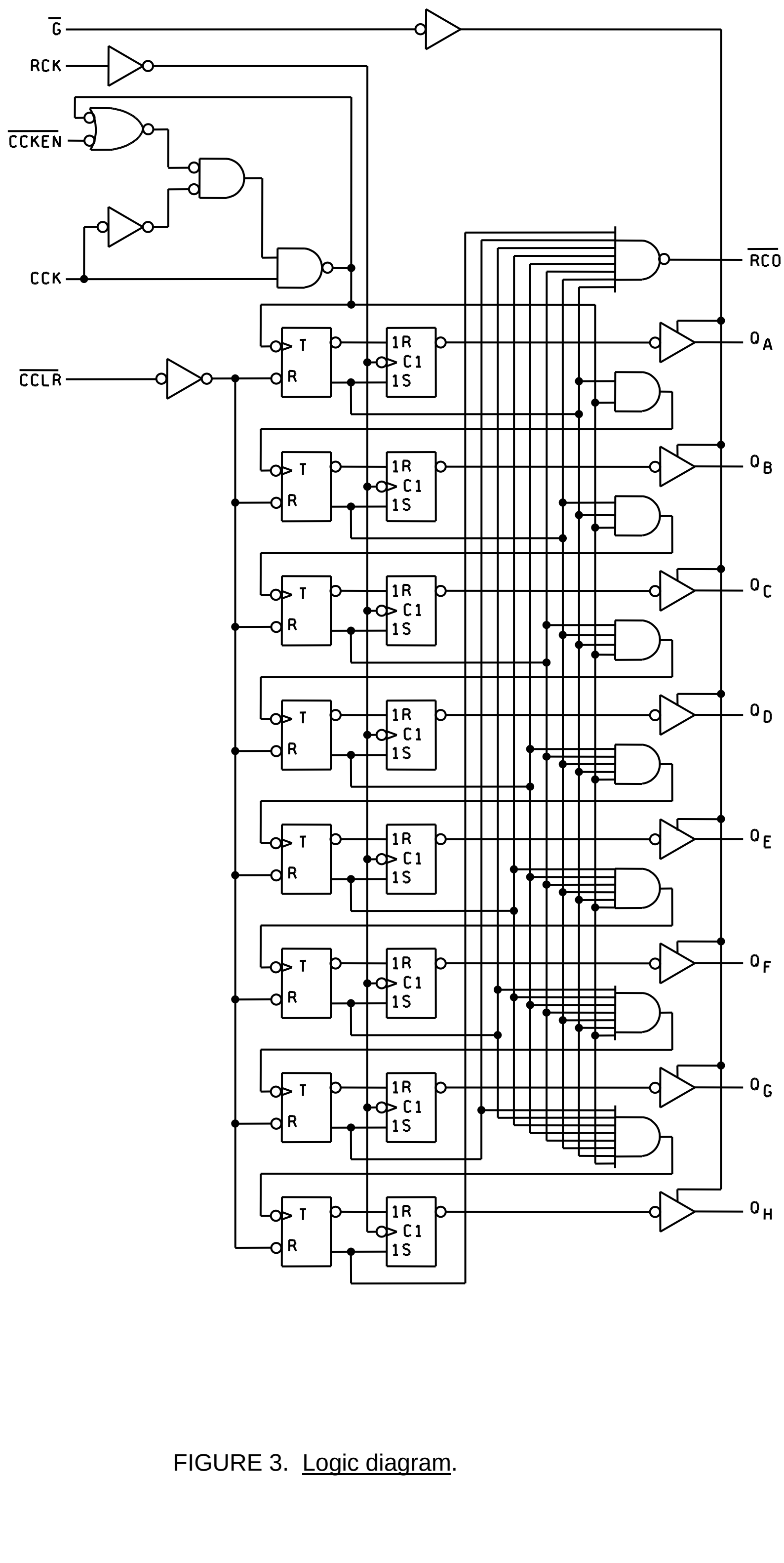


FIGURE 3. Logic diagram.

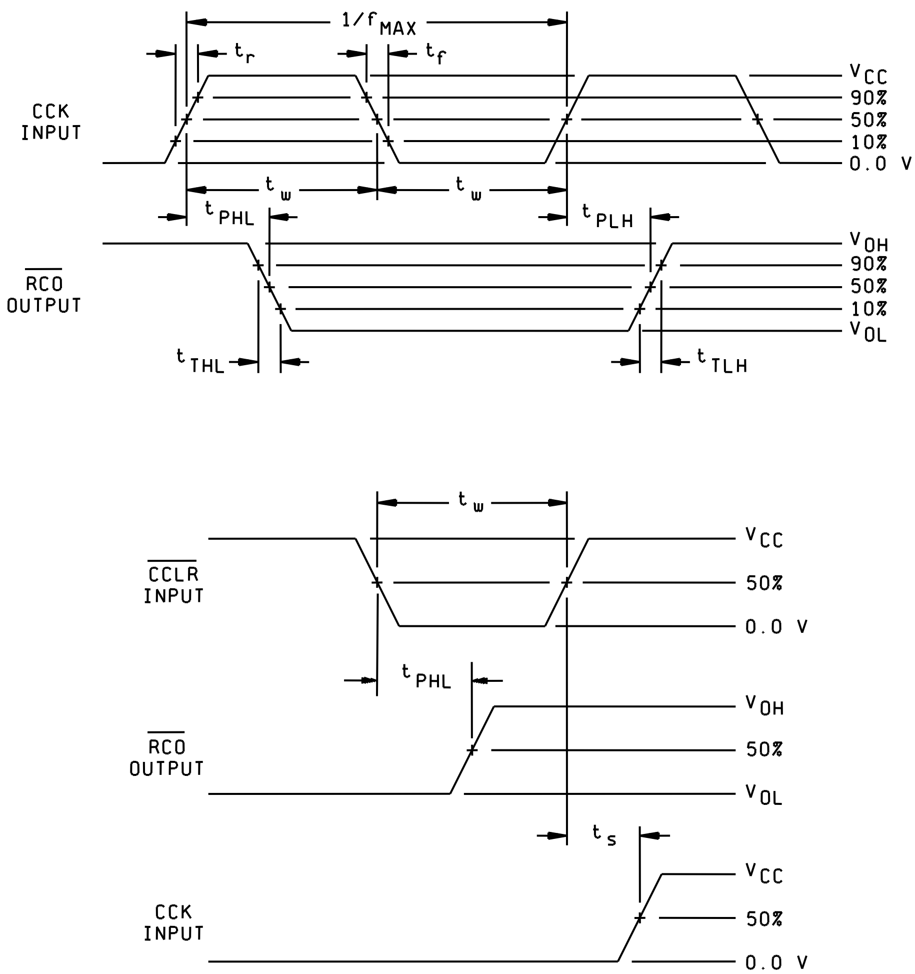


FIGURE 4. Switching waveforms and test circuit.

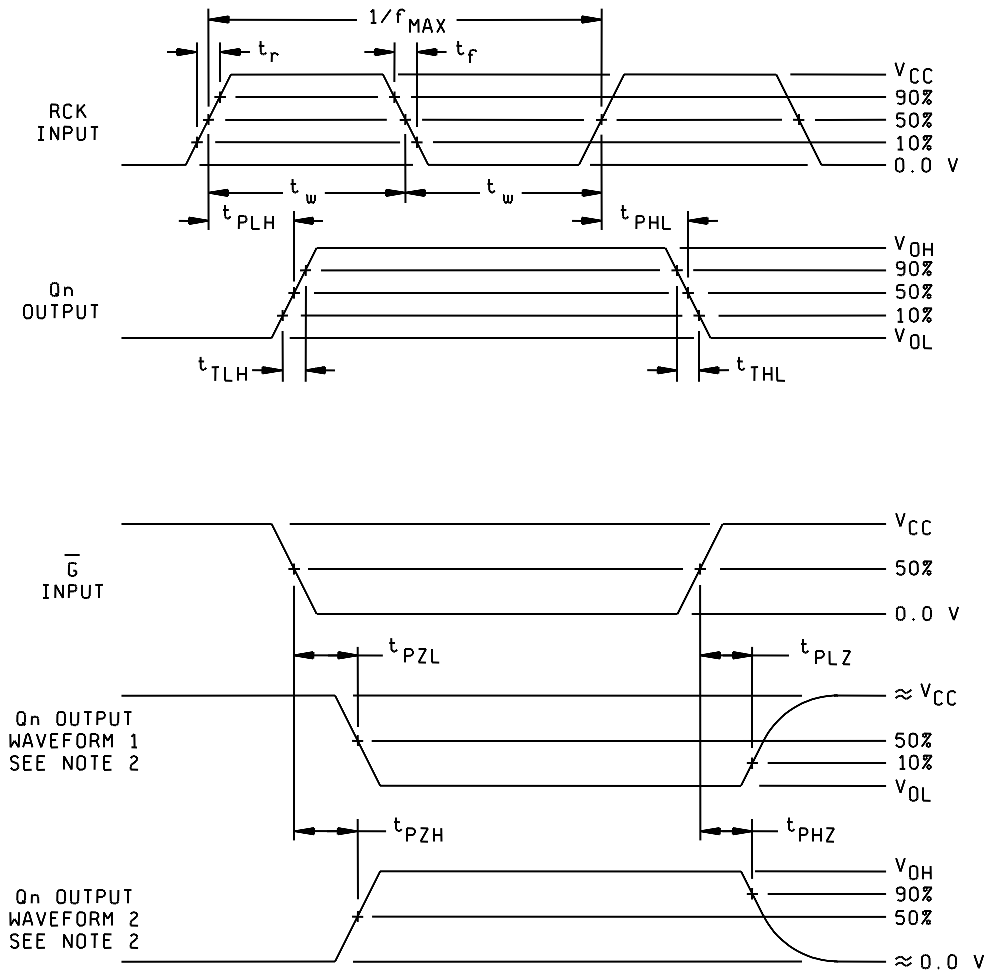
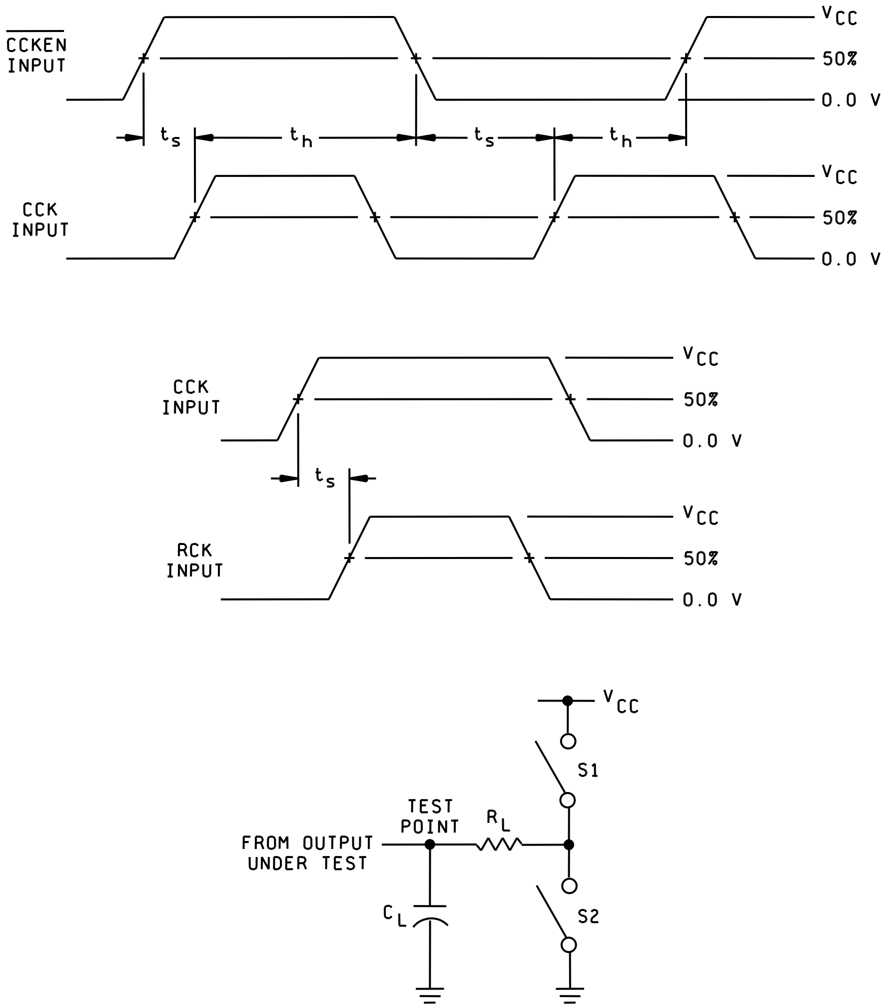


FIGURE 4. Switching waveforms and test circuit – Continued.



NOTES:

1. When measuring t_{PLH}, t_{PHL}, t_{TLH}, and t_{THL}: S1 = Open; S2 = Open.
   When measuring t_{PZH} and t_{PHZ}: S1 = Open; S2 = Closed.
   When measuring t_{PZL} and t_{PLZ}: S1 = Closed; S2 = Open.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. C_L = 50 pF or equivalent, includes test jig and probe capacitance.
4. R_L = 1.0 kΩ.
5. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 1 MHz; Z_O = 50Ω; tr = 6.0 ns; t_f = 6.0 ns; t_r and t_f shall be measured from10% of V_{CC} to 90% of V_{CC} and from 90% of V_{CC} to 10% of V_{CC}, respectively; duty cycle = 50 percent.
6. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroup 7 and 8 tests shall verify the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-10-19

Approved source of supply for SMD 5962-89603 is listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8960301EA	01295	SNJ54HC590AJ
5962-8960301FA	01295	SNJ54HC590AW
5962-89603012A	01295	SNJ54HC590AFK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493