

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add B, S, Q, and V test limits change to one part-one part number format. Add ground bounce and latch-up immunity tests. Add 10.1 substitution statements. Editorial changes throughout.	92-07-10	Monica L. Poelking
B	Changes in accordance with NOR 5962-R082-93. – tjr	93-02-26	Monica L. Poelking
C	Changes in accordance with NOR 5962-R373-97. – cfs	97-07-08	Monica L. Poelking
D	Add device type 02. Add vendor CAGE F8859. Add case outlines X and Z. Add radiation features for device type 01. Update boilerplate to MIL-PRF-38535 requirements. – jak	02-09-24	Thomas M. Hess
E	Add radiation features for device type 02 in section 1.5. Update the boilerplate to include radiation hardness assured requirements for device type 02. Editorial changes throughout. – jak	05-03-18	Thomas M. Hess
F	Update radiation features in section 1.5. Add SEP table IB and paragraph 4.4.5.2. Update the boilerplate paragraphs to current MIL-PRF-38535 requirements. – MAA	11-11-10	Thomas M. Hess
G	Update dimensions of case outline X to figure 1. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	12-12-19	Thomas M. Hess

REV																				
SHEET																				
REV	G	G	G	G	G	G	G	G	G	G	G	G								
SHEET	15	16	17	18	19	20	21	22	23	24	25	26								
REV STATUS				REV	G			G	G	G	G	G	G	G	G	G	G	G	G	G
OF SHEETS				SHEET	1			2	3	4	5	6	7	8	9	10	11	12	13	14
PMIC N/A					PREPARED BY	Tim H. Noh				DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil MICROCIRCUIT, DIGITAL, ADVANCED CMOS, RADIATION HARDENED, OCTAL POSITIVE EDGED-TRIGGERED D-TYPE FLIP-FLOP WITH THREE STATE OUTPUTS AND TTL COMPATIBLE MONOLITHIC SILICON										
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A					CHECKED BY	Wm J. Johnson														
					APPROVED BY	Michael A. Frye														
					DRAWING APPROVAL DATE	89-05-18														
					REVISION LEVEL	G				SIZE	CAGE CODE	5962-89601								
										A	67268									
										SHEET		1 OF 26								

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}).....	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN}).....	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}).....	-0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK}).....	± 20 mA
DC output current (I_{OUT}).....	± 50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}).....	± 200 mA 3/
Storage temperature range (T_{STG}).....	-65°C to +150°C
Maximum power dissipation (P_D).....	500 mW
Lead temperature (soldering, 10 seconds):	
Case outline X.....	+260°C
All other case outlines except case X.....	+300°C
Thermal resistance, junction-to-case (θ_{JC}).....	See MIL-STD-1835
Junction temperature (T_J).....	+175°C

1.4 Recommended operating conditions. 2/ 4/

Supply voltage range (V_{CC}).....	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}).....	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT}).....	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL}) ($V_{CC} = 4.5$ V and 5.5 V).....	0.8 V
Minimum high level input voltage (V_{IH}) ($V_{CC} = 4.5$ V and 5.5 V).....	2.0 V
Case operating temperature range (T_C).....	-55°C to +125°C
Input rise or fall rate ($\Delta t/\Delta V$) maximum:	
$V_{CC} = 4.5$ V.....	10 ns/V
$V_{CC} = 5.5$ V.....	8 ns/V
Maximum high level output current (I_{OH}).....	-24 mA
Maximum low level output current (I_{OL}).....	24 mA

1.5 Radiation features.

Device type 02:

 Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)..... 300 krads (Si)

Single event phenomenon (SEP):

For device type 02:

 No Single Event Latch-up (SEL) occurs at effective LET (see 4.4.5.2) ≤ 93 MeV-cm²/mg

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ For packages with multiple V_{CC} and GND pins, this value represents the maximum total current flowing into or out of all V_{CC} or GND pins.

4/ Unless otherwise specified, the values listed above shall apply over the full V_{CC} and T_C recommended operating range.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <http://www.astm.org> or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD78 - IC Latch-up Test

JESD20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

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3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes B, S, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 5.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes B, S, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes B, S, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes B, S, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes B, S, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

3.11 Substitution. Substitution data shall be as indicated in the appendix herein.

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TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit		
						Min	Max			
High level output voltage 3006	V _{OH1} <u>6/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OH} = -50 μA	All All	4.5 V	1, 2, 3	4.4		V		
	V _{OH2} <u>7/ 8/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OH} = -50 μA	All All	5.5 V	1, 2, 3	5.4				
									M	01 B, S, Q, V
									D	
	P, L, R									
	V _{OH3} <u>7/ 8/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OH} = -24 mA	All All	4.5 V	1, 2, 3	3.7				
									M	01 B, S, Q, V
									D	
	P, L, R									
	V _{OH4} <u>6/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OH} = -24 mA	All All	5.5 V	1, 2, 3	4.7				
V _{OH5} <u>7/ 8/ 9/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OH} = -50 mA	All All	5.5 V	1, 2, 3	3.85					
								M	01 B, S, Q, V	
								D		
P, L, R										
Low level output voltage 3007	V _{OL1} <u>6/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OL} = +50 μA	All All	4.5 V	1, 2, 3		0.1	V		
	V _{OL2} <u>7/ 8/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OL} = +50 μA	All All	5.5 V	1, 2, 3		0.1			
									M	01 B, S, Q, V
									D	
P, L, R										

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit					
						Min	Max						
Low level output voltage 3007	V _{OL3} <u>7/ 8/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OL} = 24 mA	All B, S, Q, V	4.5 V	1, 3		0.4	V					
							All M		2	0.5			
			01 B, S, Q, V		1	0.4							
					1	2, 3	0.5						
									0.4				
									0.4				
	V _{OL4} <u>6/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OL} = 24 mA	All B, S, Q, V	5.5 V	1, 3		0.4						
							All M		2	0.5			
					1	0.4							
						2, 3	0.5						
V _{OL5} <u>7/ 8/ 9/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OL} = 50 mA	All All	5.5 V	1, 2, 3		1.65							
						01 B, S, Q, V		1		1.65			
				1.65									
				1.65									
Three-state output leakage current high 3021	I _{OZH} <u>7/ 8/ 10/</u>	$\overline{OE} = V_{IH}$ or V _{IL} V _{IH} = 2.0 V, V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND V _{OUT} = GND	All B, S, Q, V	5.5 V	1		0.5	μA					
							All M		2	10.0			
			01 B, S, Q, V		1				0.5				
							2, 3		10.0				
									25.0				
							25.0						
			02 Q, V				25.0						
						5.0							
			Three-state output leakage current low 3020		I _{OZL} <u>7/ 8/ 10/</u>	$\overline{OE} = V_{IH}$ or V _{IL} V _{IH} = 2.0 V, V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND V _{OUT} = GND	All B, S, Q, V		5.5 V	1		-0.5	μA
												All M	
01 B, S, Q, V	1			-0.5									
				2, 3			-10.0						
							-25.0						
				-25.0									
02 Q, V				-25.0									
		-5.0											

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit
						Min	Max	
Positive input clamp voltage 3022	V _{IC+} <u>7/ 8/</u>	For input under test, I _{IN} = 1 mA	All B, S, Q, V	GND	1	0.4	1.5	V
			01 B, S, Q, V		1	0.4	1.5	
						0.4	1.5	
						0.4	1.5	
Negative input clamp voltage 3022	V _{IC-} <u>7/ 8/</u>	For input under test, I _{IN} = -1 mA	All B, S, Q, V	Open	1	-0.4	-1.5	V
			01 B, S, Q, V		1	-0.4	-1.5	
						-0.4	-1.5	
						-0.4	-1.5	
Input current high 3010	I _{IH} <u>7/ 8/</u>	For input under test, V _{IN} = V _{CC} For all other inputs, V _{IN} = V _{CC} or GND	All B, S, Q, V	5.5 V	1		0.1	μA
					2		1.0	
			All M		1		0.1	
					2, 3		1.0	
			01 B, S, Q, V		1		0.1	
							0.1	
							0.1	
							0.1	
Input current low 3009	I _{IL} <u>7/ 8/</u>	For input under test, V _{IN} = GND For all other inputs, V _{IN} = V _{CC} or GND	All B, S, Q, V	5.5 V	1		-0.1	μA
					2		-1.0	
			All M		1		-0.1	
					2, 3		-1.0	
			01 B, S, Q, V		1		-0.1	
							-0.1	
							-0.1	
							-0.1	
Control input capacitance 3012	C _{IN}	See 4.4.1b T _C = +25°C	All All	GND	4		10.0	pF
Output capacitance 3012	C _{OUT} <u>10/</u>	See 4.4.1b T _C = +25°C	All All	5.5 V	4		15.0	pF
Power dissipation capacitance	C _{PD} <u>11/</u>	See 4.4.1b T _C = +25°C	All All	5.0 V	4		55.0	pF

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit
						Min	Max	
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} <u>7/ 8/ 12/</u>	For input under test, V _{IN} = V _{CC} - 2.1 V For all other inputs, V _{IN} = V _{CC} or GND	01 B, S, Q, V	5.5 V	3		1.6	mA
					1, 2		1.0	
			02 Q, V		1, 2, 3		1.6	
			All M		1, 2, 3		1.6	
			M		01 B, S, Q, V	1	1.6	
			D				1.6	
			P, L, R				3.5	
Quiescent supply current output high 3005	I _{CC} H <u>7/ 8/</u>	$\overline{OE} = GND$ For all other inputs, V _{IN} = V _{CC} or GND	All B, S, Q, V	5.5 V	1		2.0	μA
					2		40.0	
			All M		1		8.0	
					2, 3		160.0	
			M		01 B, S, Q, V	1	100.0	
			D				1.0	
			P, L, R				3.5	
	02 Q, V		50.0	μA				
Quiescent supply current output low 3005	I _{CC} L <u>7/ 8/</u>	$\overline{OE} = GND$ For all other inputs, V _{IN} = V _{CC} or GND	All B, S, Q, V	5.5 V	1		2.0	μA
					2		40.0	
			All M		1		8.0	
					2, 3		160.0	
			M		01 B, S, Q, V	1	100.0	
			D				1.0	
			P, L, R				3.5	
	02 Q, V		50.0	μA				
Quiescent supply current outputs three-state 3005	I _{CC} Z <u>7/ 8/</u>	$\overline{OE} = V_{CC}$ For all other inputs, V _{IN} = V _{CC} or GND	All B, S, Q, V	5.5 V	1		2.0	μA
					2		40.0	
			All M		1		8.0	
					2, 3		160.0	
			M		01 B, S, Q, V	1	100.0	
			D				1.0	
			P, L, R				3.5	
	02 Q, V		50.0	μA				

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit	
						Min	Max		
Low level ground bounce noise	V _{GBL} <u>14/ 15/</u>	V _{LD} = 2.5 V I _{OL} = +24 mA See figure 5	All B, S, Q, V	4.5 V	4		2000	mV	
High level ground bounce noise	V _{GBH} <u>14/ 15/</u>	V _{LD} = 2.5 V I _{OH} = -24 mA See figure 5	All B, S, Q, V	4.5 V	4		2000	mV	
Latch-up input/output over-voltage	I _{CC} (O/V1) <u>16/</u>	t _w ≥ 100 μs t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V V _{CCQ} = 5.5 V V _{over} = 10.5 V	All B, S, Q, V	5.5 V	2		200	mA	
Latch-up input/output positive over-current	I _{CC} (O/I1+) <u>16/</u>	t _w ≥ 100 μs t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V V _{CCQ} = 5.5 V I _{trigger} = +120 mA	All B, S, Q, V	5.5 V	2		200	mA	
Latch-up input/output negative over-current	I _{CC} (O/I1-) <u>16/</u>	t _w ≥ 100 μs t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V V _{CCQ} = 5.5 V I _{trigger} = -120 mA	All B, S, Q, V	5.5 V	2		200	mA	
Latch-up supply over-voltage	I _{CC} (O/V2) <u>16/</u>	t _w ≥ 100 μs t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V V _{CCQ} = 5.5 V V _{over} = 9.0 V	All B, S, Q, V	5.5 V	2		100	mA	
Truth table test output voltage 3014	<u>7/ 8/</u> <u>17/</u>	V _{IL} = 0.40 V V _{IH} = 2.40 V Verify output V _{OUT} See 4.4.1e	All	4.5 V	7, 8	L	H		
			All	5.5 V	7, 8	L	H		
			M	01	4.5 V	7	L		H
			D	B, S, Q, V			L		H
			P, L, R			L	H		
Propagation delay time, clock to output, CP to On 3003	t _{PHL} , t _{PLH} <u>7/ 8/</u> <u>18/ 19/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 6	All	4.5 V	9, 11	1.0	11.0	ns	
			B, S, Q, V		10	1.0	13.5		
			All		9	1.0	11.0		
			M		10, 11	1.0	13.5		
			01		9	1.0	11.0		
			B, S, Q, V			1.0	11.0		
			P, L, R		1.0	11.0			

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit	
						Min	Max		
Propagation delay time, output enable, \overline{OE} to On 3003	t _{PZH} , t _{PZL} <u>7/ 8/</u> <u>18/ 19/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 6	All B, S, Q, V	4.5 V	9, 11	1.0	9.5	ns	
					10	1.0	11.0		
					9	1.0	9.5		
					10, 11	1.0	11.0		
			M		01 B, S, Q, V	9	1.0		9.5
			D			1.0	9.5		
P, L, R	1.0	9.5							
Propagation delay time, output disable, \overline{OE} to On 3003	t _{PHZ} , t _{PLZ} <u>7/ 8/</u> <u>18/ 19/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 6	All B, S, Q, V	4.5 V	9, 11	1.0	10.5	ns	
					10	1.0	12.0		
					9	1.0	10.5		
					10, 11	1.0	12.0		
			M		01 B, S, Q, V	9	1.0		10.5
			D			1.0	10.5		
P, L, R	1.0	10.5							
Maximum operating frequency	f _{MAX}	C _L = 50 pF minimum R _L = 500Ω See figure 6 See 4.4.1f	All B, S, Q, V	4.5 V	9, 11	100		MHz	
					10	70			
			All M		9	95			
					10, 11	70			
Input set-up time, Dn (high and low) to CP	t _s	C _L = 50 pF minimum R _L = 500Ω See figure 6 See 4.4.1g	All All	4.5 V	9	3.5		ns	
					10, 11	3.5			
Input hold time, Dn (high and low) to CP	t _h	C _L = 50 pF minimum R _L = 500Ω See figure 6 See 4.4.1g	All B, S, Q, V	4.5 V	9, 10	1.5		ns	
					11	2.0			
			All M	4.5 V	9	1.5		ns	
					10, 11	2.0			
Clock pulse width (high and low)	t _w	C _L = 50 pF minimum R _L = 500Ω See figure 6 See 4.4.1g	All All	4.5 V	9	5.0		ns	
					10, 11	5.0			

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table IA herein.

2/ Each input/output, as applicable shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

- a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.
- b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.
- c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 02 of this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, these devices are only tested at the 'F' level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

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TABLE IA. Electrical performance characteristics - Continued.

- 4/ The word "All" in the device type and device class column, means non-RHA limits for all device types and classes. Where M, D, P, L, R, and/or F in the conditions column are postirradiation limits for those device types and classes specified in the device type and device class column.
- 5/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.
- 6/ For device classes B, S, Q, and V, this test is guaranteed, if not tested, to the limits specified in table IA.
- 7/ RHA samples do not have to be tested at -55°C and +125°C prior to irradiation.
- 8/ When performing post irradiation electrical measurements for RHA level, $T_A = +25^\circ\text{C}$. Limits shown are guaranteed at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$.
- 9/ Transmission driving tests are performed at $V_{CC} = 5.5\text{ V}$ dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN} = 2.0\text{ V}$ or 0.8 V .
- 10/ Three-state output conditions are required.
- 11/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$ and the dynamic current consumption, $I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + n \times d \times \Delta I_{CC}$. For both P_D and I_S , n is the number of device inputs at TTL levels, f is the frequency of the input signal, and d is the duty cycle of the input signal.
- 12/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1\text{ V}$ (alternate method). Classes B, S, Q, and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limits are equal to the number of inputs at a high TTL input level times the ΔI_{CC} maximum limit, and the preferred method and limits are guaranteed.
- 13/ The maximum limit for this parameter at 100 krad (si) is $2.0\ \mu\text{A}$.
- 14/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} minimum = $\pm 24\text{ mA}$, for example) and 50pF of load capacitance (see figure 5). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse ($t_r = t_f = 3.5 \pm 1.5\text{ ns}$) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F.E.T. oscilloscope probe with at least 1 M Ω impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (figure 5). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.
- 15/ When used in synchronous TTL compatible systems, ground bounce (V_{GBL} and V_{GBH}) = 2,000 mV can be a possible problem.
- 16/ See EIA/JEDEC Standard No. 78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and V_{over} are to be accurate within ± 5 percent.
- 17/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. $H \geq 2.5\text{ V}$, $L < 2.5\text{ V}$; high inputs = 2.4 V and low inputs = 0.4 V. The input voltage levels have the allowable tolerances in accordance with MIL-STD-883 already incorporated. Functional tests at $V_{CC} = 4.5\text{ V}$ are worst case for RHA specified devices.

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TABLE IA. Electrical performance characteristics - Continued.

- 18/ Device classes B, S, Q, and V are tested at $V_{CC} = 4.5$ V at $T_C = +125^\circ\text{C}$ for sample testing and at $V_{CC} = 4.5$ V at $T_C = +25^\circ\text{C}$ for screening. Other voltages of V_{CC} and temperatures are guaranteed, if not tested. See 4.4.1d.
- 19/ AC limits at $V_{CC} = 5.5$ V are equal to the limits at $V_{CC} = 4.5$ V and guaranteed by testing at $V_{CC} = 4.5$ V. Minimum ac limits for $V_{CC} = 5.5$ V are 1.0 ns and guaranteed by guardbanding the $V_{CC} = 4.5$ V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

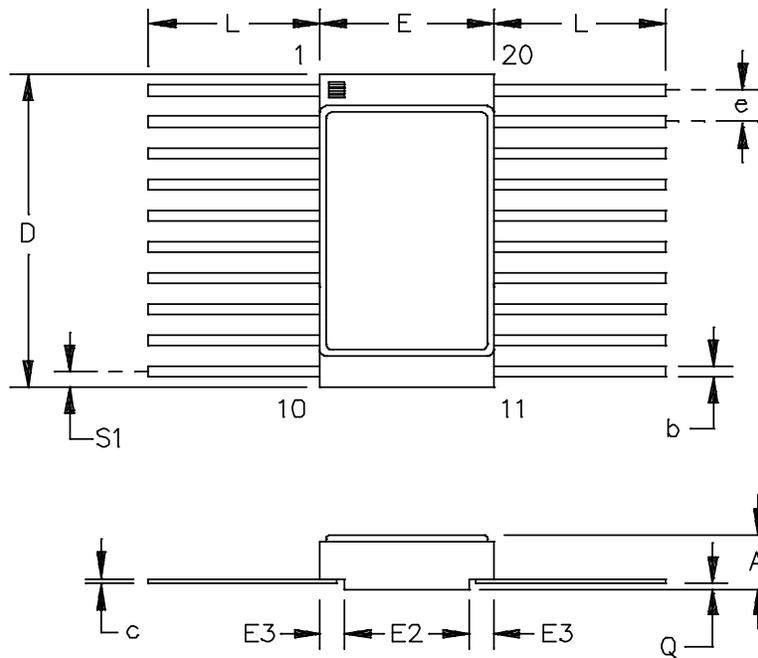
TABLE IB. SEP test limits. 1/ 2/

Device type	Bias for Single event latch-up (SEL) test; maximum operating voltage $V_{DD} = 5.5$ V No SEL at effective LET = <u>3/</u> <u>4/</u>
02	LET ≤ 93 [MeV/(mg/cm ²)]

- 1/ For SEP test conditions, see 4.4.5.2 herein.
- 2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
- 3/ Tested for latch-up at worst case operating temperature, $T_A = +125^\circ\text{C} \pm 10^\circ\text{C}$
- 4/ For device type 02 tested effective LET ≤ 93 MeV/(mg/cm²) and no latch-up occurs.

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Case outline X



Symbol	Dimensions					
	Inches			Millimeters		
	Typical	Min	Max	Typical	Min	Max
A		0.075	0.087		1.91	2.21
b		0.015	0.019		0.38	0.48
c		0.003	0.006		0.076	0.152
D		0.505	0.515		12.83	13.08
E		0.275	0.285		6.99	7.24
E2		0.199	0.211		5.05	5.36
E3	0.037			0.95		
e		0.045	0.055		1.14	1.40
L		0.250	0.370		6.35	9.39
Q		0.010	---		0.25	---
S1	0.021			0.55		

Note: Deviation from MIL-STD-1835 REF. F-9, CONFIG. B the dimension c is 0.003 inches minimum instead of 0.004 inches minimum and dimension Q is 0.010 inches Minimum instead of 0.026 inches minimum.

FIGURE 1. Case outline X.

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Device types	All
Case outlines	R, S X, Z and 2
Terminal number	Terminal symbol
1	\overline{OE}
2	D0
3	D1
4	D2
5	D3
6	D4
7	D5
8	D6
9	D7
10	GND
11	CP
12	O7
13	O6
14	O5
15	O4
16	O3
17	O2
18	O1
19	O0
20	V _{CC}

Terminal descriptions	
Terminal symbol	Description
\overline{OE}	Output enable inputs (active low)
CP	Clock pulse input
D _n (n = 0 to 7)	Data inputs
O _n (n = 0 to 7)	Data outputs

FIGURE 2. Terminal connections.

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Inputs			Output
\overline{OE}	Dn	CP	On
L	L	↑	L
L	H	↑	H
L	X	*	On ₀
H	X	X	Z

H = High voltage level
 L = Low voltage level
 X = Irrelevant
 ↑ = Low-to-high transition of the clock
 ↓ = High-to-low transition of the clock
 Z = High impedance
 * = CP at H or L or ↓
 On₀ = The value of On after the most recent positive transition of CP

FIGURE 3. Truth table.

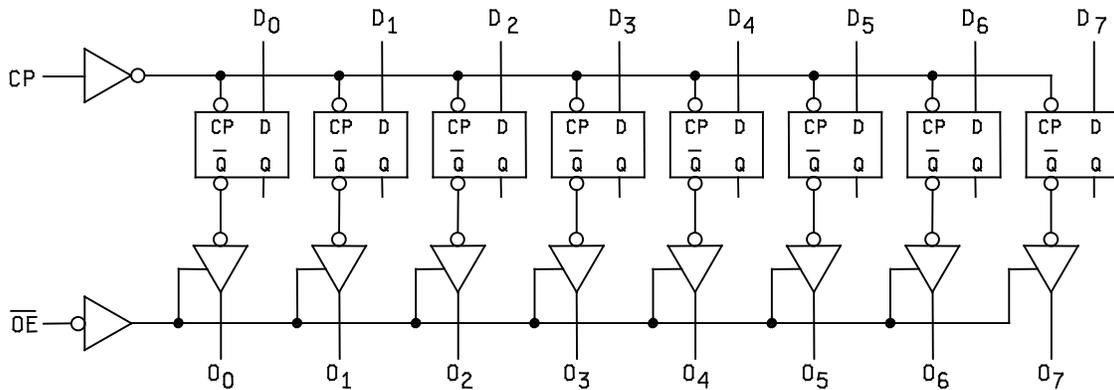


FIGURE 4. Logic diagram.

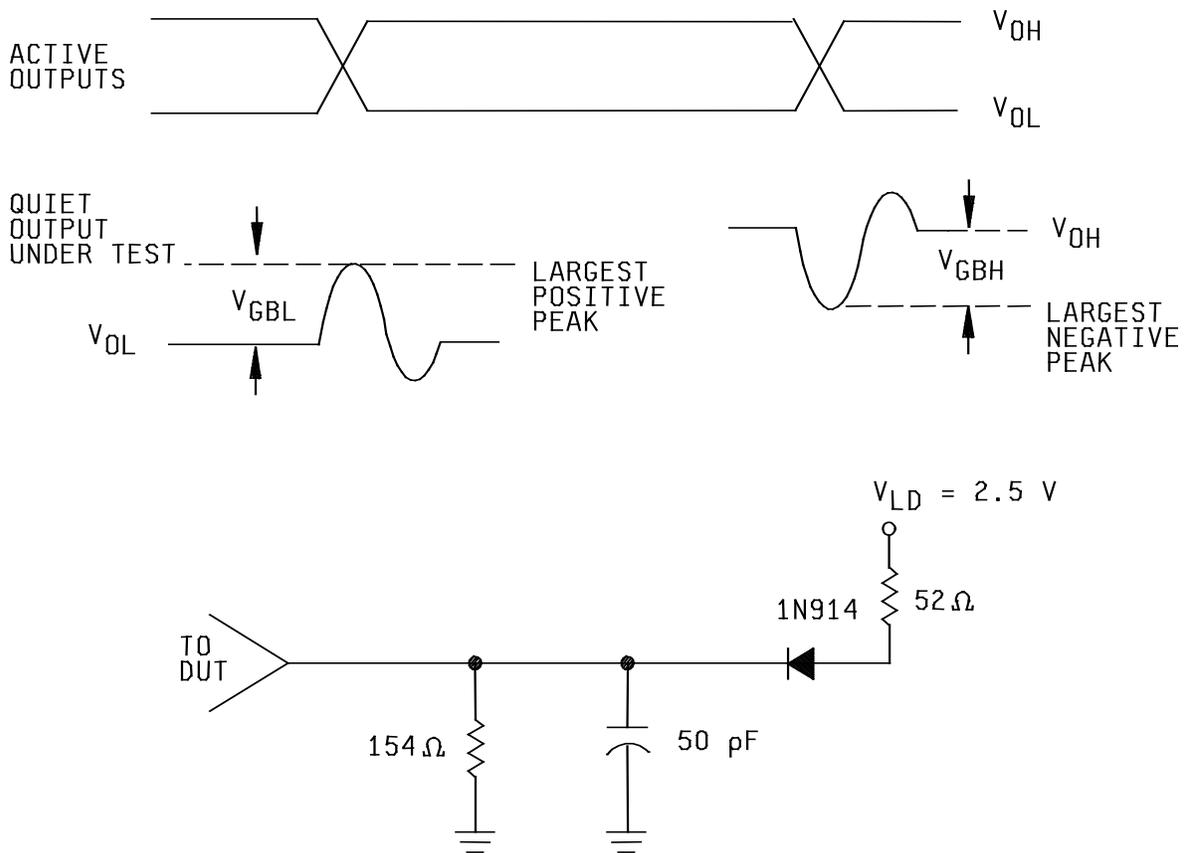
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NOTE: Resistor and capacitor tolerances = $\pm 10\%$.

FIGURE 5. Ground bounce waveforms and test circuit.

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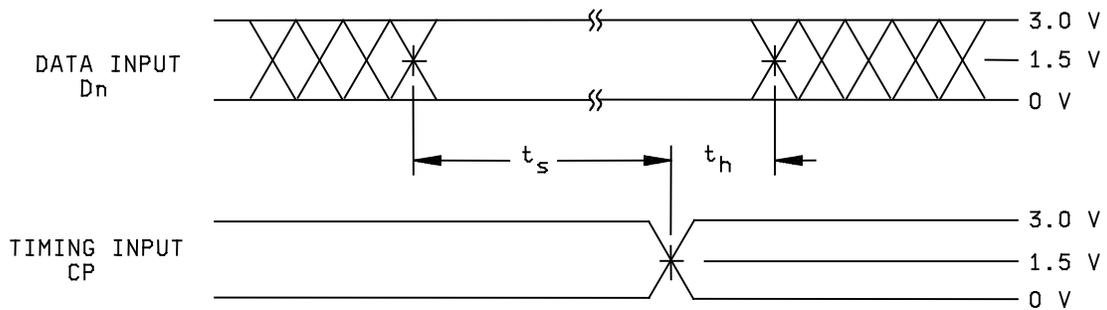


FIGURE 6. Switching waveforms and test circuit.

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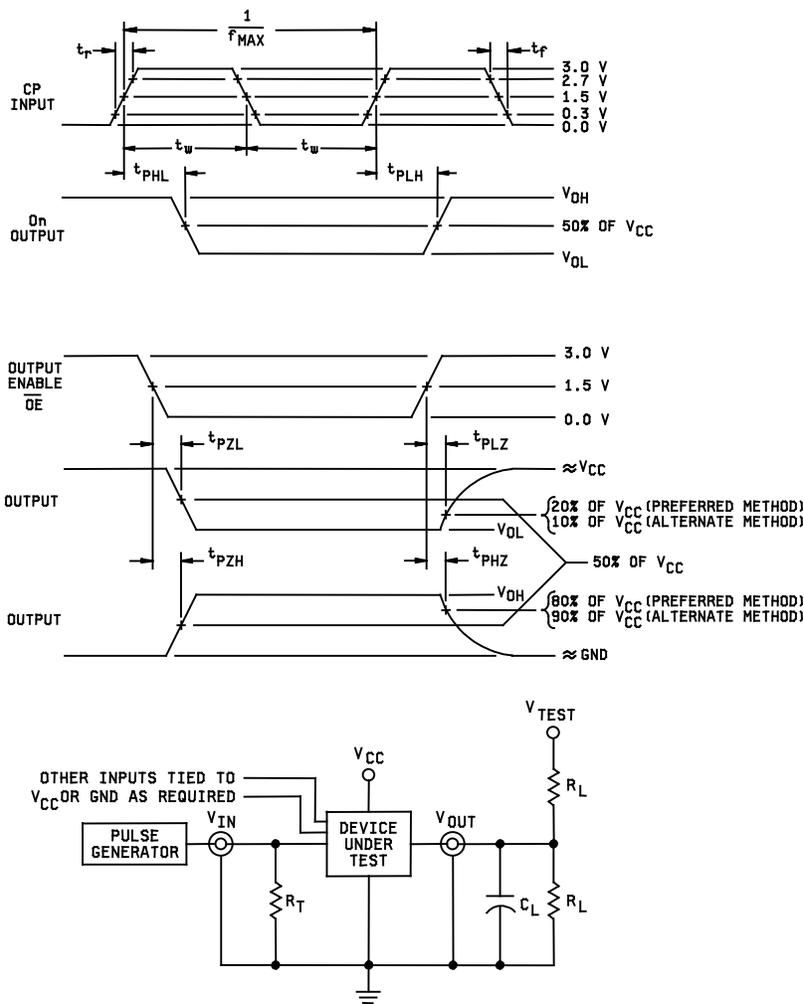
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NOTES:

1. Preferred method:
 When measuring t_{PHZ} and t_{PZH} : $V_{TEST} = GND$
 When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 2 \times V_{CC}$
 When measuring t_{PLH} and t_{PHL} : $V_{TEST} = \text{open}$
 Alternate method:
 When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 2 \times V_{CC}$
 When measuring t_{PHZ} , t_{PZH} , t_{PLH} , and t_{PHL} : $V_{TEST} = \text{open}$
2. $C_L = 50 \text{ pF}$ minimum or equivalent (includes test jig and probe capacitance).
3. $R_T = 50 \Omega$ or equivalent. $R_L = 500 \Omega$ or equivalent.
4. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to 3.0 V ; $PRR \leq 10 \text{ MHz}$; $t_r \leq 3 \text{ ns}$; $t_f \leq 3 \text{ ns}$; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
6. Outputs are measured one at a time with one output per measurement.

FIGURE 6. Switching waveforms and test circuit – Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes B, S, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A

4.2 Screening. For device classes B, S, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

- (1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- (2) $T_A = +125^\circ\text{C}$, minimum.
- (3) Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute lines 1 through 7 requirements of table IIA herein.
- (4) For device class M, unless otherwise noted, the requirements for device class B in method 1015 of MIL-STD-883 shall be followed.
- (5) Unless otherwise specified in the QM plan for static burn-in, device classes B and S, test condition A of test method 1015 of MIL-STD-883; the test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table IA of method 1015 for class B devices.
 - (a) For static burn-in I, all inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2 \pm 0.5\text{ V}$. Resistors R1 are optional on both inputs and open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5\text{ V}$. $R_1 = 220\Omega$ to $47\text{ k}\Omega$.
 - (b) For static burn-in II, all inputs shall be connected through the R1 resistors to V_{CC} . Outputs may be open or connected to $V_{CC}/2 \pm 0.5\text{ V}$. Resistors R1 are optional on open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5\text{ V}$. $R_1 = 220\Omega$ to $47\text{ k}\Omega$.
 - (c) $V_{CC} = 5.5\text{ V} + 0.5\text{ V}, -0.00\text{ V}$.
- (6) Unless otherwise specified in the QM plan for dynamic burn-in, device classes B and S, test condition D of test method 1015 of MIL-STD-883, the following shall apply:
 - (a) Input resistors = 220Ω to $2\text{ k}\Omega \pm 20$ percent.
 - (b) Output resistors = $220\Omega \pm 20$ percent.
 - (c) $V_{CC} = 5.5\text{ V} + 0.5\text{ V}, -0.00\text{ V}$.
 - (d) The output enable control pin(s) shall be connected through the resistors in parallel to V_{CC} . The clock input (CP) shall be connected through a resistor to a clock pulse (CP1). All other inputs shall be connected through the resistors in parallel to a common clock pulse (CP2), as applicable. Outputs shall be connected through the resistors to $V_{CC}/2 \pm 0.5\text{ V}$.
 - (e) $CP1, CP2 = 25\text{ kHz}$ to 1 MHz square wave; $f_{CP1} = f_{CP2}/2$; duty cycle = 50 percent ± 15 percent; $V_{IH} = 4.5\text{ V}$ to V_{CC} ; $V_{IL} = 0\text{ V} \pm 0.5\text{ V}$; $t_r, t_f \leq 100\text{ ns}$.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

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4.2.2 Additional criteria for device classes B, S, Q, and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V or S beyond the requirements of device class Q or B shall be as specified in MIL-PRF-38535, appendix B.

4.2.3 Percent defective allowable (PDA).

- a. The PDA for class S or V devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.
- b. Static burn-in I and II failures shall be cumulative for determining the PDA.
- c. The PDA for class B or Q devices shall be in accordance with MIL-PRF-38535, for static burn-in. Dynamic burn-in is not required.
- d. The PDA for class M devices shall be in accordance with MIL-PRF-38535, appendix A for static burn-in and dynamic burn-in.
- e. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table I, subgroup I, are defective and shall be removed from the lot. The verified number of failed devices times 100 divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection for device classes B, S, Q, and V. Qualification inspection for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Technology conformance inspection for classes B, S, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Latch-up and ground bounce tests are required for device classes B, S, Q, and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up and ground bounce tests, test all applicable pins on five devices with zero failures.
- c. C_{IN} , C_{OUT} , and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table IA herein. For C_{IN} , C_{OUT} , and C_{PD} , test all applicable pins on five devices with zero failures.

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- d. For device classes B, S, Q, and V, subgroups 9 and 11 tests shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.
- e. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3, herein. For device classes B, S, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- f. For device classes B, S, Q, and V, f_{MAX} shall be measured only for initial qualification and after process or design changes which may affect the device frequency. Test all applicable pins on 22 devices with zero failures.
- g. For device classes B, S, Q, and V, t_s , t_h , and t_w shall be guaranteed, if not tested, to the limits specified in table IA.

4.4.2 Group B inspection. When applicable, the group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be maintained by the manufacturer and shall be made available to the acquiring or preparing activity upon request.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes B, S, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes B, S, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^\circ\text{C} \pm 5^\circ$, after exposure, to the subgroups specified in table IIA herein.
- c. RHA tests for device classes M, B, S, Q, and V for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table IA for subgroups specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups <u>1/</u> (in accordance with MIL-STD-883, method 5005, table I)	Subgroups <u>1/</u> (in accordance with MIL-PRF-38535, table III)			
	Device class M	Device <u>2/</u> class B	Device <u>2/</u> class S	Device class Q	Device class V
Interim electrical parameters, method 5004 (see 4.2)		1	1	1	1
Static burn-in I, method 1015 (see 4.2.1a)	<u>3/</u>	Not required	Required <u>4/</u>	Not required	Required <u>4/</u>
Interim electrical parameters, method 5004 (see 4.2.1b)			1 <u>5/</u>		1 <u>5/</u>
Static burn-in II, method 1015 (see 4.2.1a)	<u>3/</u>	Required <u>6/</u>	Required <u>4/</u>	Required <u>6/</u>	Required <u>4/</u>
Interim electrical parameters, method 5004 (see 4.2.1b)		1 <u>2/ 5/</u>	1 <u>2/ 5/</u>	1 <u>2/ 5/</u>	1 <u>2/ 5/</u>
Dynamic burn-in I, method 1015 (see 4.2.1a)	<u>3/</u>	Not required	Required <u>4/</u>	Not required	Required <u>4/</u>
Interim electrical parameters, method 5004 (see 4.2.1b)			1 <u>5/</u>		1 <u>5/</u>
Final electrical parameters, method 5004	1, 2, 3, 7, 8, 9 <u>2/</u>	1, 2, 7, 9 <u>2/ 6/</u>	1, 2, 7, 9 <u>2/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>2/ 6/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>2/</u>
Group A test requirements, method 5005 (see 4.4.1)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group B end-point electrical parameters, method 5005 (see 4.4.2)			1, 2, 3, 7, 8, 9, 10, 11 <u>5/</u>		
Group C end-point electrical parameters, method 5005 (see 4.4.3)	1, 2, 3	1, 2 <u>5/</u>		1, 2, 3 <u>5/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>5/</u>
Group D end-point electrical parameters, method 5005 (see 4.4.4)	1, 2, 3	1, 2	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters, method 5005 (see 4.4.5)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ PDA applies to subgroup 1 (see 4.2.3). For device classes S and V, PDA applies to subgroups 1 and 7 (see 4.2.3).

3/ The burn-in shall meet the requirements of 4.2.1a herein.

4/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with test method 5004 of MIL-STD-883. For pre-burn-in and interim electrical parameters the read-and-record requirements are for delta measurements only.

5/ Delta limits shall be required only on table IA, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table IIB.

6/ The device manufacturer may at his option either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table IIA).

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TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter <u>1/</u>	Symbol	Device type	Delta limits
Quiescent supply current	I_{CCH}, I_{CCL}	01	± 100 nA <u>2/</u>
	I_{CCZ}	02	± 300 nA
Supply current delta	ΔI_{CC}	02	± 0.4 mA
Input current low level	I_{IL}	02	± 20 nA
Input current high level	I_{IH}	02	± 20 nA
Output voltage low level ($I_{OL} = 24$ mA, $V_{CC} = 5.5$ V)	V_{OL}	02	± 0.04 V
Output voltage high level ($I_{OH} = -24$ mA, $V_{CC} = 5.5$ V)	V_{OH}	02	± 0.20 V

- 1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.
2/ Guaranteed, if not tested.

4.4.5.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

Device type 02:

- (1) Inputs tested high, $V_{CC} = 5.5$ V dc $\pm 5\%$, $V_{IN} = 5.0$ V dc $+10\%$, $R_{IN} = 1$ k Ω $\pm 20\%$, and all outputs are open.
- (2) Inputs tested low, $V_{CC} = 5.5$ V dc $\pm 5\%$, $V_{IN} = 0.0$ V dc, $R_{IN} = 1$ k Ω $\pm 20\%$, and all outputs are open.

4.4.5.1.1 Accelerated annealing test. Accelerated annealing test shall be performed on classes M, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C $\pm 5^\circ$ C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.5.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The upset test temperature shall be +25°C. The latch-up test temperature shall be at the maximum rated operating temperature $\pm 10^\circ$ C.
- f. Bias conditions shall be $V_{CC} = 5.5$ V dc for the latch-up measurements.
- g. For SEP test limits, see table IB herein.

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4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes B, S, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes B, S, Q, and V. Sources of supply for device classes B, S, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Number of upsets (SEU).
- d. Number of transients (SET).
- e. Occurrence of latch-up (SEL).

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APPENDIX A

A.1 SCOPE

A.1.1 Scope. This appendix contains the PIN substitution information to support the one part-one part number system. For new designs, after the date of this document the new PIN shall be used in lieu of the old PIN. For existing designs prior to the date of this document the new PIN can be used in lieu of the old PIN. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN substitution data shall be as follows.

A.2 APPLICATION DOCUMENTS

This section is not applicable to this appendix.

A.3 SUBSTITUTION DATA

<u>New PIN</u>	<u>Old PIN</u>
5962-8960101MRA	5962-8960101RA
5962-8960101MSA	5962-8960101SA
5962-8960101M2A	5962-89601012A

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-12-19

Approved sources of supply for SMD 5962-89601 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8960101RA	0C7V7	54ACT574DMQB
		QP54ACT574DMQB
5962-8960101SA	0C7V7	54ACT574FMQB
		QP54ACT574FMQB
5962-89601012A	0C7V7	54ACT574LMQB
		QP54ACT574LMQB
5962-8960101BRA	0C7V7	JM54ACT574BRA
		QP54ACT574BRA
5962-8960101BSA	0C7V7	JM54ACT574BSA
		QP54ACT574BSA
5962-8960101B2A	0C7V7	JM54ACT574B2A
		QP54ACT574B2A
5962-8960101MRA	0C7V7	54ACT574DMQB
		QP54ACT574DMQB
5962-8960101MSA	0C7V7	54ACT574FMQB
		QP54ACT574FMQB
5962-8960101M2A	0C7V7	54ACT574LMQB
		QP54ACT574LMQB
5962R8960101SZA	<u>3/</u>	54ACT574
5962R8960101BRA	<u>3/</u>	54ACT574
5962R8960101BSA	<u>3/</u>	54ACT574
5962R8960101B2A	<u>3/</u>	54ACT574
5962R8960101SRA	<u>3/</u>	54ACT574
5962R8960101SSA	<u>3/</u>	54ACT574
5962R8960101S2A	<u>3/</u>	54ACT574
5962-8960102QXA	<u>3/</u>	54ACT574
5962-8960102QXC	<u>3/</u>	54ACT574
5962-8960102VXA	<u>3/</u>	54ACT574
5962-8960102VXC	<u>3/</u>	54ACT574
5962F8960102QXA	F8859	RHFACT574K02Q
5962F8960102QXC	F8859	RHFACT574K01Q
5962F8960102VXA	F8859	RHFACT574K02V
5962F8960102VXC	F8859	RHFACT574K01V

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

DATE: 12-12-19

Vendor CAGE
number

Vendor name
and address

0C7V7

e2v aerospace and defense, inc.
dba QP Semiconductor, Inc.
765 Sycamore Drive
Milpitas, CA 95035

F8859

ST Microelectronics
3 rue de Suisse
BP4199
35041 RENNES cedex2-FRANCE

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