

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outlines F and 2. Add output noise voltage test to table I, reference section. Change minimum limit for $V_{TH(SYNC)}$ test in table I, oscillator section. Editorial changes throughout.	94-02-28	M. A. FRYE
B	Add device class V device and make change to TABLE II. - ro	00-11-30	R. MONNIN
C	Add device type 05. Make changes to 1.2.2, 1.3, 1.4, table I, figure 1, and figure 2. - ro	01-03-21	R. MONNIN
D	Drawing updated to reflect current requirements. - rrp	06-03-31	R. MONNIN
E	Add device type 06 and Table IIB. Make changes to 1.2.2, 1.4, Table I, figure 1, and figure 2. - ro	08-12-03	R. HEBER
F	Update drawing to current MIL-PRF-38535 requirements. -rrp	15-04-14	C. SAFFLE



THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	F																			
SHEET	15																			

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

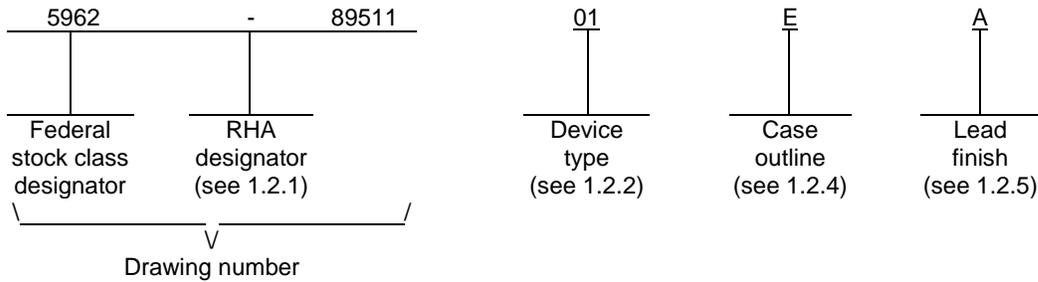
PMIC N/A	PREPARED BY JOSEPH A. KERBY	<p align="center"><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a></p>																	
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY D. H. JOHNSON																		
	APPROVED BY MICHAEL A. FRYE	<p align="center">MICROCIRCUIT, LINEAR, REGULATING, PULSE WIDTH MODULATOR, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 89-04-27																		
	REVISION LEVEL F	SIZE A	CAGE CODE <b>67268</b>	<b>5962-89511</b>															
SHEET 1 OF 15																			

1. SCOPE

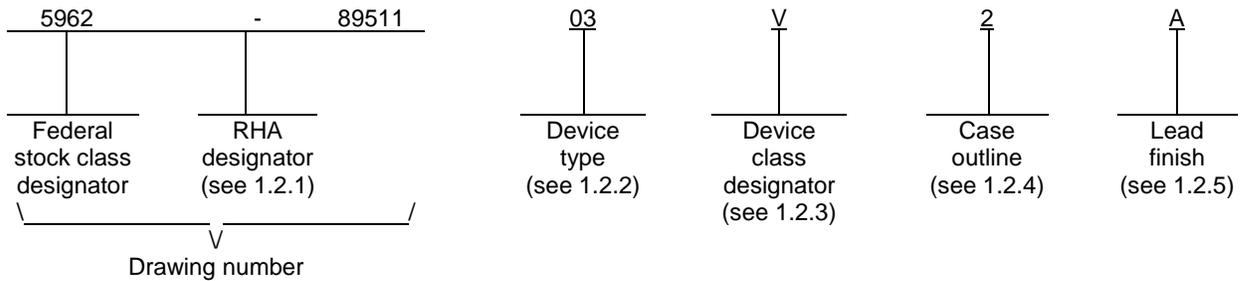
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device class M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	1525A	Regulating pulse width modulator
02	1527A	Regulating pulse width modulator
03	UC1525A	Regulating pulse width modulator
04	UC1527A	Regulating pulse width modulator
05	UC1525B	Regulating pulse width modulator
06	UC1525B-SP	Regulating pulse width modulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

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1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. <sup>1/</sup>

Input voltage (+V <sub>IN</sub> ) .....	+40 V dc
Collector voltage (V <sub>C</sub> ) .....	+40 V dc
Logic inputs range .....	-0.3 V dc to +5.5 V dc
Analog inputs range .....	-0.3 V dc to +V <sub>IN</sub>
Output current, source or sink .....	500 mA
Reference output current .....	50 mA
Oscillator charging current .....	5 mA
Maximum power dissipation (P <sub>D</sub> ) .....	1,000 mW
Lead temperature (soldering, 10 seconds) .....	+300°C
Junction temperature (T <sub>J</sub> ) .....	+150°C
Storage temperature range .....	-65°C to +150°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ) .....	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ <sub>JA</sub> ):	
Cases E and F .....	100°C/W
Case 2.....	70°C/W

1.4 Recommended operating conditions.

Input voltage (+V <sub>IN</sub> ) .....	+8 V dc to +35 V dc
Collector voltage (V <sub>C</sub> ) .....	+4.5 V dc to +35 V dc
Sink/source load current (steady-state) .....	0 mA to 100 mA
Sink/source load current (peak) .....	0 mA to 400 mA
Reference load current range .....	0 mA to 20 mA
Oscillator frequency range:	
Device types 01 - 04 .....	100 Hz to 350 kHz
Device types 05 and 06 .....	100 Hz to 400 kHz
Oscillator timing resistor (R <sub>T</sub> ):	
Device types 01 - 04 .....	2 kΩ to 200 kΩ
Device types 05 and 06 .....	2 kΩ to 150 kΩ
Oscillator timing capacitor range (C <sub>T</sub> ):	
Device types 01 - 04 .....	470 pF to 0.1 μF
Device types 05 and 06 .....	0.001 pF to 0.1 μF
Dead time resistor range (device types 05 and 06 only) .....	0 Ω to 500 Ω
Ambient operating temperature range (T <sub>A</sub> ) .....	-55°C to +125°C

<sup>1/</sup> Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein .

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Reference section							
Reference voltage out	V <sub>REF</sub>		1	01-04	5.05	5.15	V
			2,3		5.0	5.2	
			1	05, 06	5.062	5.138	
Line regulation	V <sub>RLINE</sub>	V <sub>IN</sub> = 8 V to 35 V	1,2,3	01-04	-30	30	mV
				05, 06	-10	10	
Load regulation	V <sub>LOAD</sub>	I <sub>L</sub> = 0 mA to 20 mA	1,2,3	01-04	-50	50	mV
				05, 06	-15	15	
Short-circuit current	I <sub>OS</sub>	V <sub>REF</sub> = 0 V, t < 25 ms, T <sub>A</sub> = +25°C	1	01-04	-100		mA
				05, 06		100	
Temperature stability	V <sub>TS</sub>	<u>3/</u>	2,3	05, 06		50	mV
Total output variation	V <sub>TOV</sub>	Line, load, and temperature	1,2,3	05, 06	5.036	5.164	V
Long term stability	V <sub>LTS</sub>	1000 hours, <u>3/</u> T <sub>A</sub> = +125°C	2	05		10	mV
Output noise voltage	N <sub>O</sub>	10 Hz ≤ f ≤ 10 kHz, <u>3/</u> T <sub>A</sub> = +25°C	7	All		200	μVrms
Oscillator section							
Initial accuracy	F <sub>OSC</sub>	T <sub>A</sub> = +25°C	4	All	37.5	42.5	kHz
Oscillator accuracy over temperature	F <sub>OSC</sub> (OT)	T <sub>A</sub> = -55°C and +125°C	5,6	All	35.2	44.8	kHz
Voltage stability	V <sub>STAB</sub>	V <sub>IN</sub> = 8 V to 35 V	4,5,6	All		±1	%
Clock pulse amplitude	V <sub>OSC</sub>	<u>3/</u>	4,5,6	All	3		V
Clock pulse width	t <sub>PW</sub>	T <sub>A</sub> = +25°C <u>3/</u>	9	All	0.3	1.0	μs
Max oscillator frequency	F <sub>MAX</sub>	R <sub>T</sub> = 2 kΩ, C <sub>T</sub> = .001 μF	4,5,6	01,02	300		kHz
		R <sub>T</sub> = 2 kΩ, C <sub>T</sub> = 470 μF		03,04	350		
				05, 06	400		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Oscillator section – continued.							
Min oscillator frequency	F <sub>MIN</sub>	R <sub>T</sub> = 150 kΩ, C <sub>T</sub> = 0.1 μF	4,5,6	01, 02		150	Hz
		R <sub>T</sub> = 200 kΩ, C <sub>T</sub> = 0.1 μF		03, 04, 05, 06		120	
Threshold SYNC voltage	V <sub>TH</sub> (SYNC)		1,2,3	All	1.2	2.8	V
SYNC input current	I <sub>I</sub> (SYNC)	SYNC voltage = 3.5 V	1,2,3	All		2.5	mA
Pulse width modulator comparator section							
Min duty cycle	t <sub>ON</sub> (min) / t <sub>OSC</sub>	V <sub>COMP</sub> = 0.6 V	9,10,11	01-04		.001	%
				05, 06		0	
Max duty cycle	t <sub>ON</sub> (max) / t <sub>OSC</sub>	V <sub>COMP</sub> = 3.6 V	9,10,11	All	45		%
Input threshold <u>4/</u>	V <sub>TH</sub>	Zero duty cycle	1,2,3	06	0.7		V
		Maximum duty cycle				3.6	
Error amplitude section, V <sub>CM</sub> = 5.1 V (unless otherwise specified)							
Input offset voltage	V <sub>IO</sub>	R <sub>S</sub> ≤ 2 kΩ	1,2,3	All	-5	5	mV
Input bias current	I <sub>IB</sub>		1,2,3	All		10	μA
Input offset current	I <sub>IO</sub>		1,2,3	All	-1	1	μA
DC open loop gain	A <sub>VOL</sub>	T <sub>A</sub> = +25°C, V <sub>CM</sub> = 5.1 V, R <sub>L</sub> ≥ 10 MΩ	4	All	60		dB
Output low level	V <sub>OL</sub>		1,2,3	All		0.5	V
Output high level	V <sub>OH</sub>		1,2,3	All	3.8		V
Common mode rejection ratio	CMRR	V <sub>CM</sub> = 1.5 V to 5.2 V	1,2,3	All	60		dB
Power supply rejection ratio	PSRR	V <sub>IN</sub> = 8 V to 35 V	4,5,6	All	50		dB
Unity gain bandwidth	GBW	A <sub>V</sub> = 0 dB, T <sub>A</sub> = +25°C <u>3/</u>	7	All	1		MHz

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Soft start section							
Soft start current	I <sub>SS</sub>	V <sub>SD</sub> = 0 V, V <sub>SS</sub> = 0 V	1,2,3	All	25	80	μA
Soft start voltage	V <sub>SS</sub>	V <sub>SD</sub> = 2.5 V	1,2,3	All		0.7	V
Shutdown input current	I <sub>SD</sub>	V <sub>SD</sub> = 2.5 V	1,2,3	All		1.0	mA
Shutdown threshold voltage	V <sub>TH</sub>	To outputs, V <sub>SS</sub> = 5.1 V, T <sub>A</sub> = +25°C	4	03, 04, 05, 06	0.6		V
Output section (each output), V <sub>C</sub> = +20 V (unless otherwise specified)							
Output low level	V <sub>OL</sub>	I <sub>SINK</sub> = 20 mA	1,2,3	All		0.4	V
		I <sub>SINK</sub> = 100 mA				2.2	
Output high level	V <sub>OH</sub>	I <sub>SOURCE</sub> = -20 mA	1,2,3	All	18		V
		I <sub>SOURCE</sub> = -100 mA			17		
Under voltage lockout	V <sub>UL</sub>	V <sub>COMP</sub> and V <sub>SS</sub> = high	1,2,3	All	6	8	V
Shutdown delay	t <sub>SD</sub>	V <sub>SD</sub> = 3 V, T <sub>A</sub> = +25°C <u>3/</u>	9	01,02		500	ns
		V <sub>SD</sub> = 2.5 V, T <sub>A</sub> = +25°C <u>3/</u>		03, 04, 05, 06		500	
Rise time	t <sub>r</sub>	C <sub>L</sub> = 1 nF, T <sub>A</sub> = +25°C <u>3/</u>	9	All		600	ns
Collector fall time	t <sub>f</sub>	C <sub>L</sub> = 1 nF, T <sub>A</sub> = +25°C <u>3/</u>	9	All		300	ns
Collector leakage voltage	V <sub>CL</sub>	V <sub>C</sub> = 35 V	1,2,3	05, 06		200	μA
V <sub>C</sub> off current	I <sub>VC</sub> (off)	V <sub>C</sub> = 35 V	1,2,3	01,03		200	μA
Total standby current section							
Supply current	I <sub>S</sub>	V <sub>IN</sub> = 35 V	1,2,3	All		20	mA

1/ Unless otherwise specified, +V<sub>IN</sub> = 20 V, R<sub>T</sub> = 3.6 kΩ, C<sub>T</sub> = 0.01 μF, and R<sub>D</sub> = 0 Ω.

2/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

3/ If not tested, shall be guaranteed to the limits specified in table I herein.

4/ Tested at F<sub>OSC</sub> = 40 kHz, R<sub>T</sub> = 3.6 kΩ, C<sub>T</sub> = 0.01 μF, and R<sub>D</sub> = 0 Ω.  
Approximate oscillator frequency is defined by:  $f = 1 / (C_T (0.7 \times R_T \times 3R_D))$ .

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Device types	01, 02, 03, 04, 05, and 06	
Case outlines	E and F	2
Terminal number	Terminal symbol	
1	INVERTING INPUT	NC
2	NONINVERTING INPUT	INVERTING INPUT
3	SYNC	NONINVERTING INPUT
4	OSCILLATOR OUTPUT	SYNC
5	C <sub>T</sub>	OSCILLATOR OUTPUT
6	R <sub>T</sub>	NC
7	DISCHARGE	C <sub>T</sub>
8	SOFT-START	R <sub>T</sub>
9	COMPENSATION	DISCHARGE
10	SHUTDOWN	SOFT START
11	OUTPUT A	NC
12	GROUND	COMPENSATION
13	V <sub>C</sub>	SHUTDOWN
14	OUTPUT B	OUTPUT A
15	+V <sub>IN</sub>	GROUND
16	V <sub>REF</sub>	NC
17	---	V <sub>C</sub>
18	---	OUTPUT B
19	---	+V <sub>IN</sub>
20	---	V <sub>REF</sub>

NC = No connection

FIGURE 1. Terminal connections.

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Device types 01 and 02

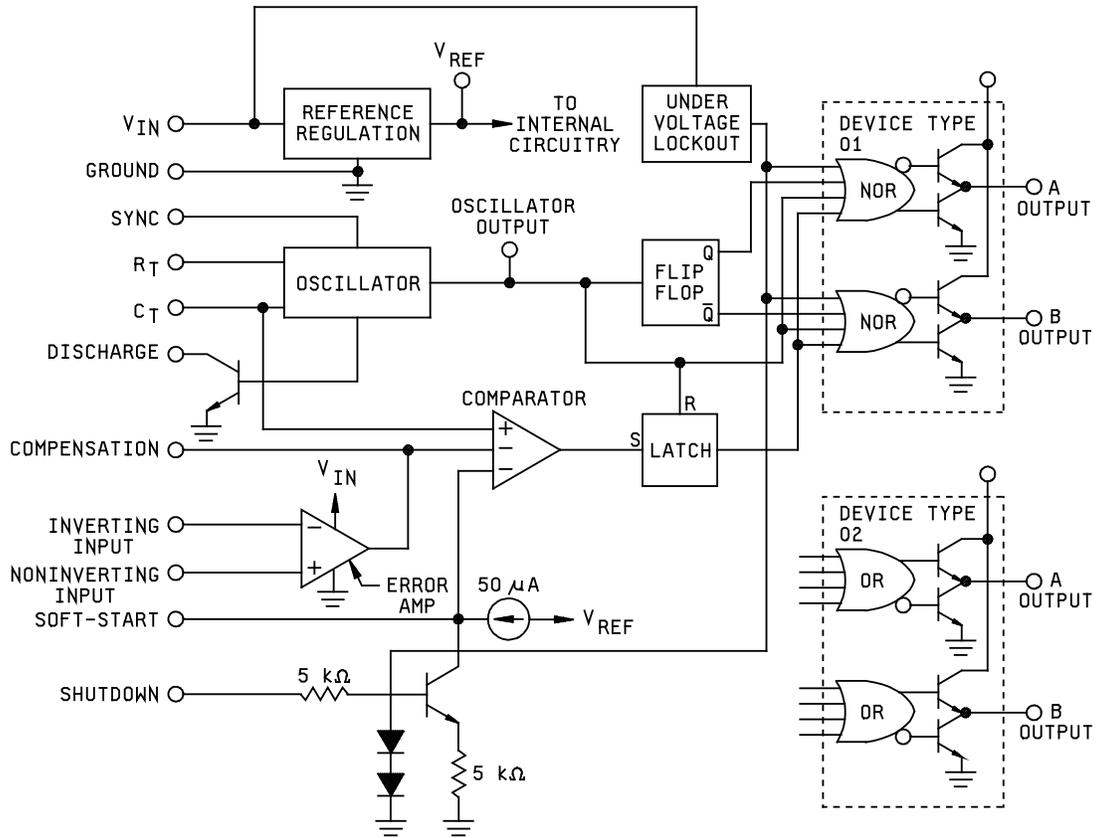


FIGURE 2. Logic diagram.

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Device types 03 and 04

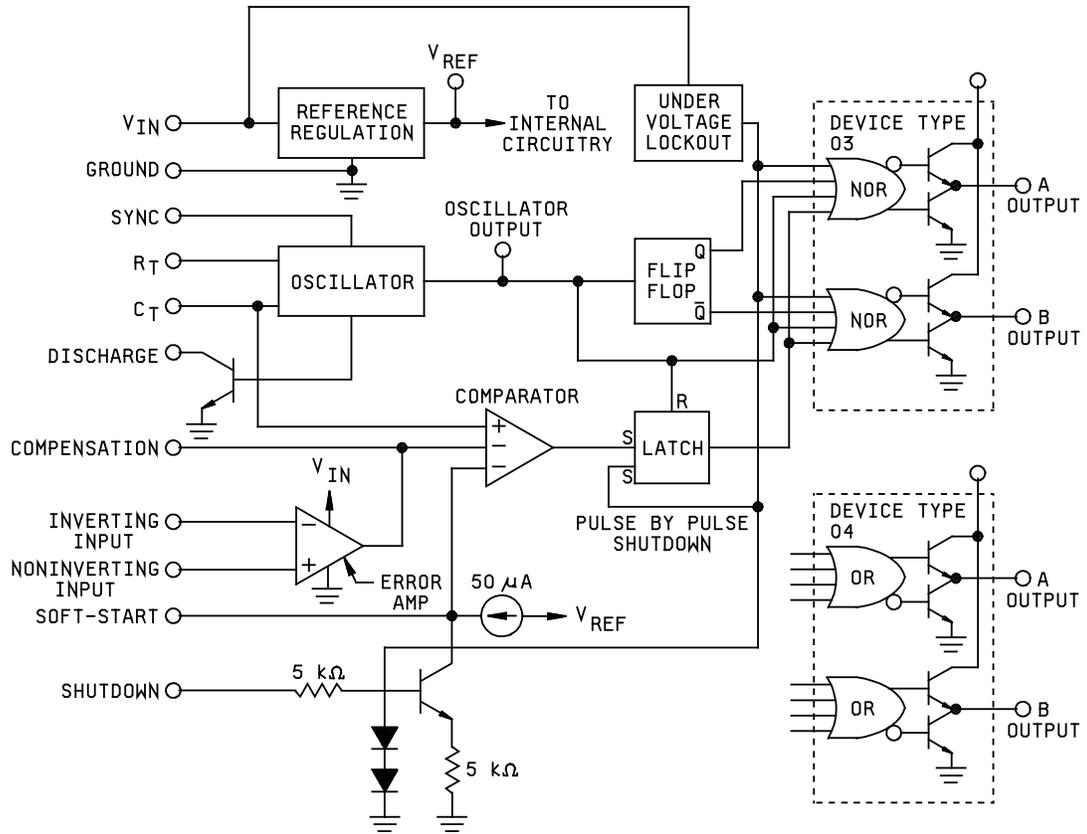


FIGURE 2. Logic diagram – Continued.

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Device types 05 and 06

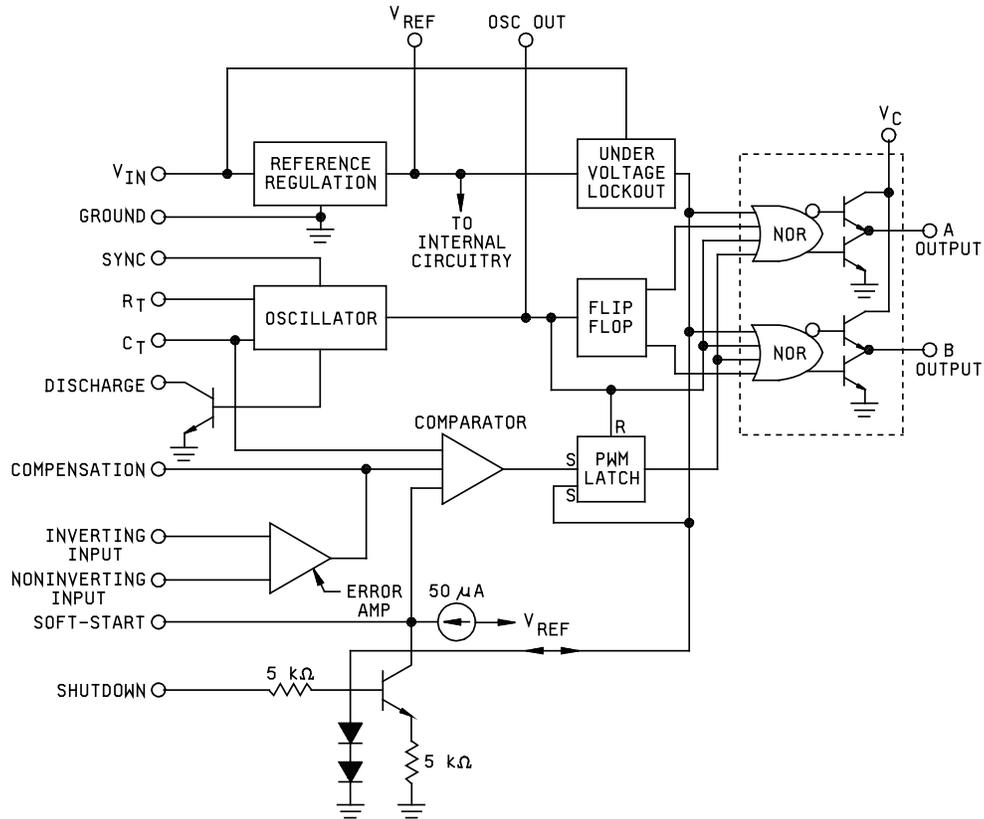


FIGURE 2. Logic diagram - Continued.

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3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 110 (see MIL-PRF-38535, appendix A).

#### 4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

##### 4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

##### 4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1,2,3,4,9 <u>1/</u>	1,2,3,4,9 <u>1/</u>	1,2,3, <u>1/ 2/</u> 4,9
Group A test requirements (see 4.4)	1,2,3,4,5,6,7, 9,10,11	1,2,3,4,5,6,7, 9,10,11	1,2,3,4,5,6,7, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1,2,3 <u>2/</u>
Group D end-point electrical parameters (see 4.4)	1	1	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and delta limits shall be computed with reference to the previous endpoint electrical parameters.

TABLE IIB. Delta limits. T<sub>A</sub> = +25°C

Parameters	Symbol	Conditions	Delta limits	Units
Reference output voltage	V <sub>REF</sub>		±20	mV
Oscillator accuracy	F <sub>OSC</sub>	R <sub>T</sub> = 3.6 kΩ, C <sub>T</sub> = 0.01 μF, R <sub>D</sub> = 0 Ω	±3	%
Error amplifier input bias current	I <sub>IB</sub>		±0.1	μA
Supply current	I <sub>S</sub>		±1	mA

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b.  $T_A = +125^{\circ}\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

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6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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DATE: 15-04-14

Approved sources of supply for SMD 5962-89511 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /	Reference military specification PIN
5962-8951101EA	U3158	IP1525AJ-DESC	M38510/12603BEA
	34333	SG1525AJ/883B	
	<u>3</u> /	UC1525AJ/883B	
	<u>3</u> /	LT1525AJ/883	
5962-8951101FA	34333	SG1525AF/883B	---
5962-89511012A	01295	UC1525AL883B	---
5962-8951102EA	U3158	IP1527AJ-DESC	M38510/12604BEA
	34333	SG1527AJ/883B	
	<u>3</u> /	UC1527AJ/883B	
	<u>3</u> /	LT1527AJ/883	
5962-89511022A	<u>3</u> /	UC1527AL/883B	---
5962-8951103EA	01295	UC1525AJ883B	---
5962-89511032A	01295	UC1525AL883B	---
5962-8951103VEA	<u>3</u> /	UC1525AJQMLV	---
5962-8951103V2A	<u>3</u> /	UC1525ALQMLV	---
5962-8951104EA	01295	UC1527AJ883B	---
5962-89511042A	01295	UC1527AL883B	---

STANDARD MICROCIRCUIT DRAWING BULLETIN - CONTINUED

DATE: 15-04-14

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>	Reference military specification PIN
5962-8951105EA	01295	UC1525BJ883B	---
5962-89511052A	01295	UC1525BL883B	---
5962-8951105VEA	01295	UC1525BJQMLV	---
5962-8951105V2A	01295	UC1525BLQMLV	---
5962-8951106V2A	01295	UC1525BFK-SP	---

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE  
number

Vendor name  
and address

U3158

Semelab PLC  
Coventry Road, Lutterworth  
Leicestershire LE174JB  
United Kingdom

01295

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243  
Point of contact: U.S. Highway 75 South  
P.O. Box 84, M/S 853  
Sherman, TX 75090-9493

34333

Microsemi Analog Mixed Signal Group  
11861 Western Avenue  
Garden Grove, CA 92841-2119

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.