REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline 3. Add vendor CAGE 1ES66. Made changes to tables I and II, and figures 1 and 2	91-09-17	M. A. FRYE
B	Update drawing to current requirements. Editorial changes throughout. – drw	04-07-08	R. MONNIN
C	Make correction to the Mode 1 timing waveform as specified under figure 3. - ro	06-01-18	R. MONNIN
D	Update drawing to current MIL-PRF-38535 requirements. - jch	18-03-05	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
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REV																				
SHEET																				
REV STATUS				REV			D	D	D	D	D	D	D	D	D	D	D	D	D	
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY
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WILLIAM K. HECKMAN

DRAWING APPROVAL DATE
89-08-07

REVISION LEVEL
D

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dla.mil/landandmaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL-LINEAR, 8-BIT A/D CONVERTERS, HIGH SPEED, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88764**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88764	01	L	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Total adjusted error
01	7824T	4-channel 8-bit A/D converter	±1.0 LSB
02	7824U	4-channel 8-bit A/D converter	±0.5 LSB
03	7828T	8-channel 8-bit A/D converter	±1.0 LSB
04	7828U	8-channel 8-bit A/D converter	±0.5 LSB

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
3	CQCC1-N28	28	Square leadless chip carrier
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{DD} to ground range	0 V dc to +7 V dc
Digital input voltage to ground ($\overline{RD}$, $\overline{CS}$, A0, A1 and A2)	-0.3 V dc to V_{DD}
Digital output voltage to ground (DB0, DB7, RDY and $\overline{INT}$)	-0.3 V dc to V_{DD}
$V_{REF}(+)$ to ground	$V_{REF}(-)$ to V_{DD}
$V_{REF}(-)$ to ground	0 V dc to $V_{REF}(+)$
Analog input, any channel	-0.3 V dc to V_{DD}
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D)	450 mW 1/
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}) (all cases)	120°C/W
Junction temperature (T_J)	+175°C

1/ Derate above T_A = +75°C at 6.0 mW/°C for case outlines L, X, and 3.

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+4.75 V dc to +5.25 V dc
Positive reference voltage $V_{REF}(+)$	+5.0 V dc
Negative reference voltage $V_{REF}(-)$	0 V dc
Ground potential (GND)	0 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES	Guaranteed minimum resolution for which no codes are missing	1, 2, 3	All	8.0		Bits
Total unadjusted error 3/	TUE		1, 2, 3	01, 03		±1.0	LSB
			1	02, 04		±1.0	
			2, 3, 12			±0.5	
Analog input leakage current	I_{IN}	Any channel	1, 2, 3	All		±3.0	µA
Reference input 4/ resistance	R_{IN}		1, 2, 3	All	1.0	4.0	kΩ
Digital input high voltage	V_{IH}	$\overline{RD}$, $\overline{CS}$, A0, A1, A2 5/	1, 2, 3	All	2.4		V
Digital input low voltage	V_{IL}	$\overline{RD}$, $\overline{CS}$, A0, A1, A2 5/	1, 2, 3	All		0.8	V
Digital input high current	I_{IH}	$\overline{RD}$, $\overline{CS}$, A0, A1, A2 5/	1, 2, 3	All		1.0	µA
Digital input low current	I_{IL}	$\overline{RD}$, $\overline{CS}$, A0, A1, A2 5/	1, 2, 3	All		-1.0	µA
Digital output high voltage	V_{OH}	$DB_0 – DB_7$, $\overline{INT}$, I_{SOURCE} = 360 µA	1, 2, 3	All	4.0		V
Digital output low voltage	V_{OL}	$DB_0 – DB_7$, $\overline{INT}$, I_{SINK} = 1.6 mA	1, 2, 3	All		0.4	V
		RDY, I_{SINK} = 2.6 mA 6/				0.4	
Floating state leakage current	I_{OUT}	$DB_0 – DB_7$ only	1, 2, 3	All		3.0	µA
Supply current from V_{DD}	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = 2.4 V	1, 2, 3	All		20	mA
Power supply sensitivity	PSS	V_{DD} = +5.0 V ±5.0%	1, 2, 3	All		±0.25	LSB
Analog input capacitance 4/	C_{IN1}	0 V to 5.0 V, T_A = +25°C	4	All		45	pF
Digital input capacitance 4/	C_{IN2}	$\overline{RD}$, $\overline{CS}$, A0, A1, A2 5/ T_A = +25°C	4	All		8.0	pF
Digital output 4/ capacitance	C_{OUT}	T_A = +25°C	4	All		8.0	pF
Slew rate, tracking 4/	SR	T_A = +25°C	4	All		0.157	V/µs
Functional tests		See 4.3.1d and figure 2	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{CS}$ to $\overline{RD}$ setup time	t_{CSS}	See figure 3	9, 10, 11	All	0		ns
$\overline{CS}$ to $\overline{RD}$ hold time	t_{CSH}	See figure 3	9, 10, 11	All	0		ns
$\overline{CS}$ to RDY delay	t_{RDY}	C_L = 50 pF, pull-up resistor = 5.0 kΩ, see figure 3	9	All		40	ns
			10, 11			60	
Conversion time, mode 0	t_{CRD}	See figure 3	9	All		2.0	µs
			10, 11			2.8	
Data access time after $\overline{RD}$, mode 1	t_{ACC1}	See figure 3 7/ 8/	9	All		85	ns
			10, 11			120	
$\overline{RD}$ to $\overline{INT}$ delay	t_{INTH}	C_L = 50 pF	9	All		75	ns
			10, 11			100	
Data hold time	t_{DH}	See figure 3 and 4 9/	9	All		60	ns
			10, 11			70	
Delay time between conversions	t_P	See figure 3	9	All	500		ns
			10, 11		600		
Read pulse width, mode 1	t_{RD}	See figure 3	9	All	60	600	ns
			10, 11		80	400	
Data access time after $\overline{INT}$	t_{ACC2}	See figure 3 7/ 8/	9	All		50	ns
			10, 11			70	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Multiplexer address setup time	t_{AS}	See figure 3	9, 10, 11	All	0		ns
Multiplexer address hold time	t_{AH}	See figure 3	9	All	30		ns
			10, 11		40		

1/ V_{DD} = +5.0 V, $V_{REF}(+)$ = +5.0 V, and $V_{REF}(-)$ = GND = 0 V unless otherwise specified. Specifications apply for mode 0. All input control signals are specified with $t_r = t_f$ = 20 ns (10% to 90% of +5.0 V) and timed from a voltage level of 1.6 V.

2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

3/ Total unadjusted error includes offset, full scale, and linearity errors.

4/ The (C_{IN1}, C_{IN2}, R_{IN}, C_{OUT}, and SR measurements) are measured initially and after any process or design changes which may affect these tests.

5/ A2 applies to device types 03 and 04 only.

6/ RDY is an open drain output.

7/ Measured with load circuits of figure 5 and defined as the time required for an output to cross 0.8 V or 2.4 V.

8/ If not tested, shall be guaranteed to the limits specified in table I herein.

9/ Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of figure 4 and is measured only for the initial test and after process or design changes which may affect t_{DH}.

Device types	01 and 02	03 and 04
Case outlines	L	X and 3
Terminal number	Terminal symbol	
1	AIN 4	AIN 6
2	AIN 3	AIN 5
3	AIN 2	AIN 4
4	AIN 1	AIN 3
5	NC	AIN 2
6	DB0	AIN 1
7	DB1	NC
8	DB2	DB0
9	DB3	DB1
10	$\overline{RD}$	DB2
11	$\overline{INT}$	DB3
12	GND	$\overline{RD}$
13	$V_{REF(-)}$	$\overline{INT}$
14	$V_{REF(+)}$	GND
15	RDY	$V_{REF(-)}$
16	$\overline{CS}$	$V_{REF(+)}$
17	DB4	RDY
18	DB5	$\overline{CS}$
19	DB6	DB4
20	DB7	DB5
21	A1	DB6
22	A0	DB7
23	NC	A2
24	V_{DD}	A1
25	- - -	A0
26	- - -	V_{DD}
27	- - -	AIN 8
28	- - -	AIN 7

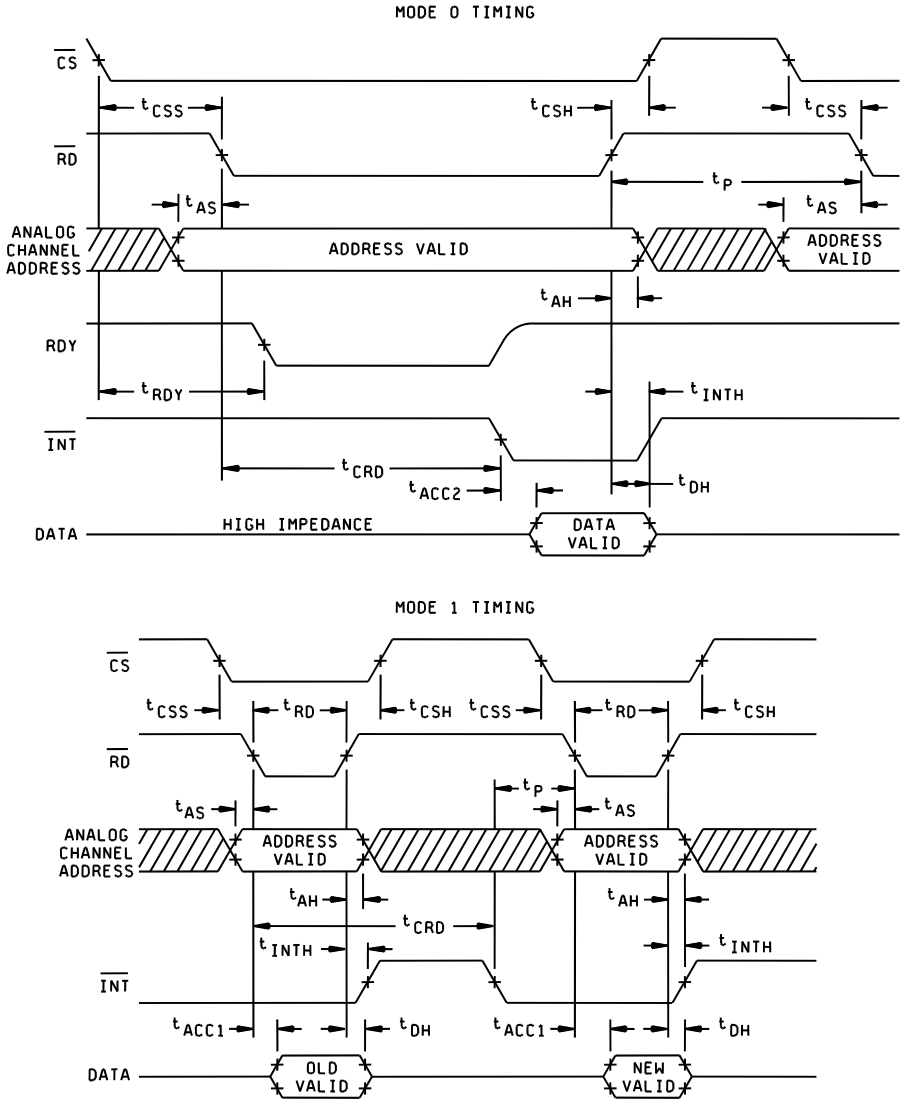
NC = No connection

FIGURE 1. Terminal connections.

Device types 01 and 02		Device types 03 and 04			Channel
A1	A0	A2	A1	A0	
0	0	0	0	0	AIN 1
0	1	0	0	1	AIN 2
1	0	0	1	0	AIN 3
1	1	0	1	1	AIN 4
		1	0	0	AIN 5
		1	0	1	AIN 6
		1	1	0	AIN 7
		1	1	1	AIN 8

0 = Logic low state
1 = Logic high state

FIGURE 2. Truth table.



NOTES:

1. All input signal rise and fall times are measured from 10% to 90% of +5.0 V, $t_r = t_f = 20$ ns.
2. Timing measurements reference level is ($V_{IH} + V_{IL}$) / 2.

FIGURE 3. Timing diagram.

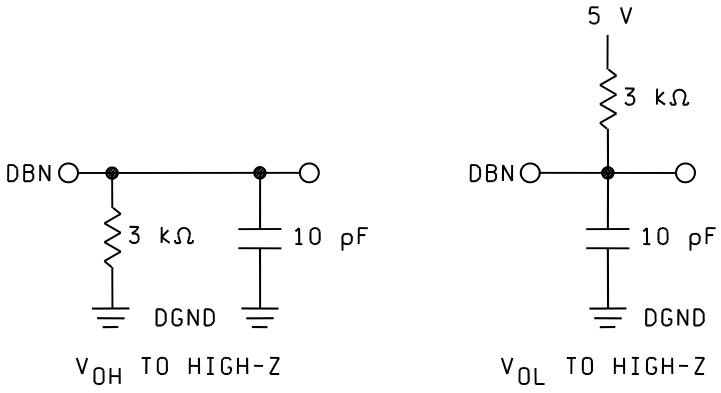


FIGURE 4. Load circuits for data hold time.

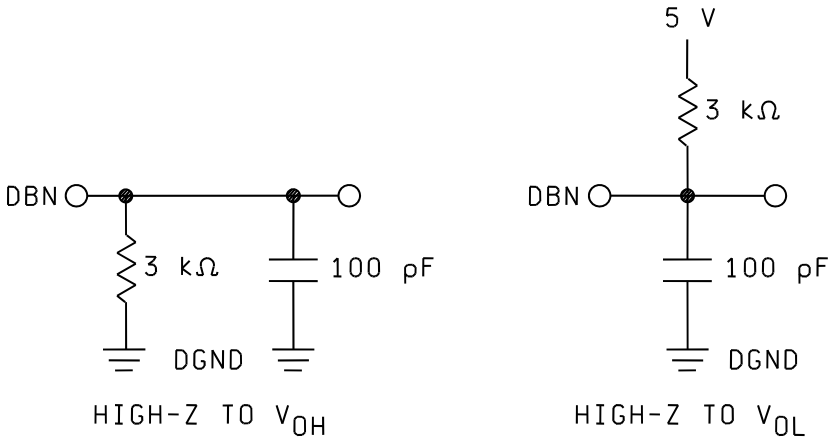


FIGURE 5. Load circuits for data access time.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 12
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10***, 11***, 12****
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** See 4.3.1c.
*** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I herein.
**** See 4.3.1e.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} C_{IN2}, R_{IN}, C_{OUT}, and SR measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

e. Subgroup 12 test is used for grading and part selection at TA = 25°C, and is not included in PDA calculations.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 18-03-05

Approved sources of supply for SMD 5962-88764 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: https://landandmaritimeapps.dla.mil/programs/smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8876401LA	3/	MX7824TQ/883B
	24355	AD7824TQ/883B
5962-8876402LA	3/	MX7824UQ/883B
	24355	AD7824UQ/883B
5962-8876403XA	3/	MX7828TQ/883B
	24355	AD7828TQ/883B
5962-8876404XA	3/	MX7828UQ/883B
	24355	AD7828UQ/883B
5962-88764043A	24355	AD7828UE/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.