REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with Notice of Revision (NOR) 5962-R299-92	92-09-02	Michael A. Frye
B	Update drawing to reflect current requirements. New boilerplate. -les	00-11-27	Raymond Monnin
C	Update drawing to current requirements. Editorial changes throughout. - gap	08-04-04	Robert M. Heber

The original first sheet of this drawing has been replaced.

REV																				
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REV																				
SHEET																				
REV STATUS				REV			C	C	C	C	C	C	C	C	C					
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9					

PMIC N/A

PREPARED BY
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COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. H. Johnson

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-10-11

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED LOW POWER SCHOTTKY TTL, OCTAL D-TYPE EDGE TRIGGERED FLIP-FLOPS, MONOLITHIC SILICON

REVISION LEVEL
C

SIZE	CAGE CODE	
A	**67268**	**5962-88728**

SHEET 1 OF 9

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88728	01	R	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALS564	Octal D-type edge-triggered flip-flops with three-state outputs

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc minimum to +7.0 V dc maximum
Input voltage range ..... -1.2 V dc at -18 mA to +7.0 V dc
Voltage applied to a disabled three-state output ..... +5.5 V dc
Storage temperature ..... -65°C to +150°C
Maximum power dissipation (P_D) 1/ ..... 165 mW
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH}) ..... 2.0 V dc
Maximum low level input voltage (V_{IL}):
T_C = +125°C ..... 0.7 V
T_C = -55°C ..... 0.8 V
T_C = +25°C ..... 0.8 V
High level output current (I_{OH}) ..... -1.0 mA maximum
Low level output current (I_{OL}) ..... 12 mA maximum
Case operating temperature range (T_C) ..... -55°C to +125°C
Pulse duration t_W, CLK high or low ..... 20 ns minimum
Setup time data before CLK, low or high (t_{su}) ..... 15 ns minimum
Hold time data after CLK, low to high (t_h) ..... 4 ns minimum

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to output current test; e.g., I_O.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -0.4 mA, V_{IH} = 2.0 V 2/	V_{IL} = 0.8 V	1, 3	2.5		V
			V_{IL} = 0.7 V	2			
		V_{CC} = 4.5 V, I_{OH} = -1.0 mA, V_{IH} = 2.0 V 2/	V_{IL} = 0.8 V	1, 3	2.4		V
			V_{IL} = 0.7 V	2			
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = 12 mA 2/	V_{IL} = 0.8 V	1, 3		0.4	V
			V_{IL} = 0.7 V	2			
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1, 2, 3		-1.2	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V, All other inputs ≥ 4.5 V		1, 2, 3		-0.2	mA
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V, All other inputs = 0.0 V		1, 2, 3		20	μA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 7.0 V, All other inputs = 0.0 V		1, 2, 3		0.1	mA
Output current	I_O	V_{CC} = 5.5 V, V_{OUT} = 2.25 V 3/		1, 2, 3	-20	-112	mA
Output current, outputs off	I_{OZH}	V_{CC} = 5.5 V, V_{OUT} = 2.7 V		1, 2, 3		20	μA
	I_{OZL}	V_{CC} = 5.5 V, V_{OUT} = 0.4 V		1, 2, 3		-20	μA
Supply current	I_{CC}	V_{CC} = 5.5 V	Outputs high	1, 2, 3		18	mA
			Outputs low			24	
			Outputs disabled			30	
Functional tests		GND ≤ V_{IL} ≤ V_{OL}, V_{OH} ≤ V_{IH} ≤ V_{CC} See 4.3.1c		7, 8			
Clock frequency	f_{max}	V_{CC} = 4.5 to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, See figure 3 4/		9, 10, 11	25		MHz
Propagation delay time from CLK to any $\overline{Q}$	t_{PLH}			9, 10, 11	4	16	ns
	t_{PHL}				4	19	
Output enable time from $\overline{OC}$ to any $\overline{Q}$	t_{PZH}			9, 10, 11	4	21	ns
	t_{PZL}				3	21	
Output disable time from $\overline{OC}$ to any $\overline{Q}$	t_{PHZ}			9, 10, 11	2	12	ns
	t_{PLZ}				3	20	

1/ Unused inputs that do not directly control the pin under test must be ≥ 2.5 V dc or ≤ 0.4 V. No unused inputs shall exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.

2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or V_{IH} minimum input.

3/ The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and the duration of the test condition shall not exceed one second.

4/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V.

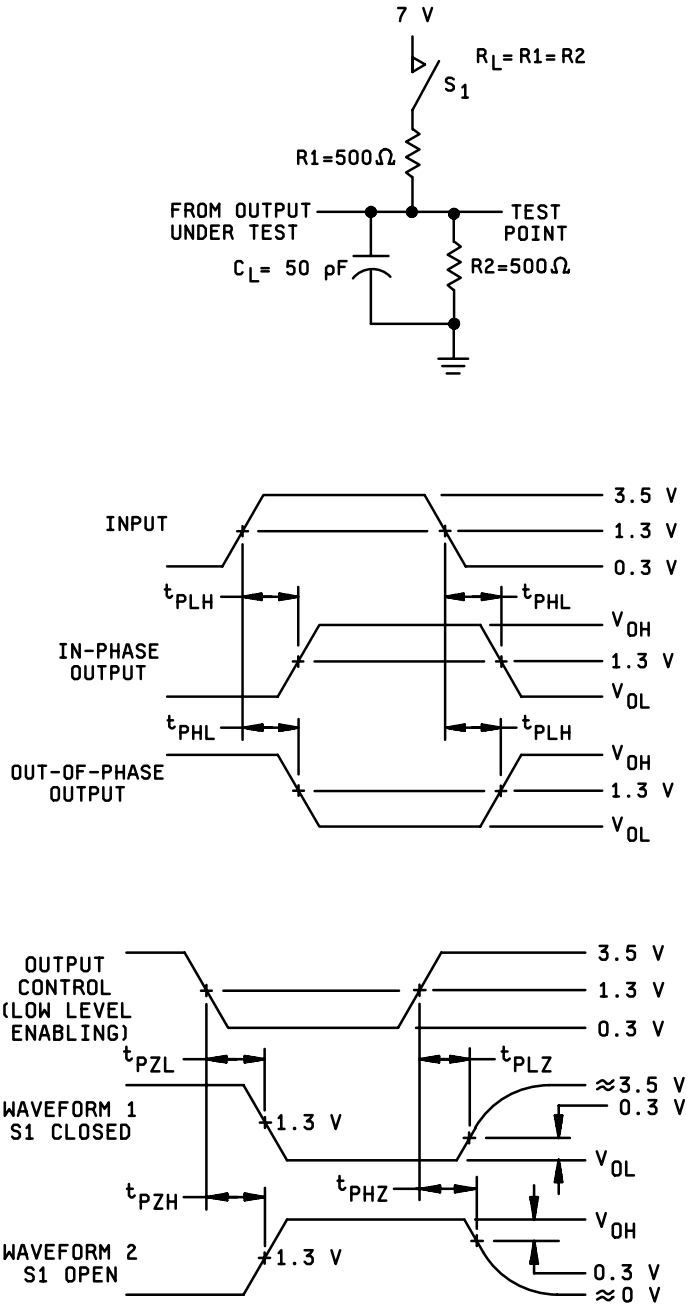
Case outlines	R, S, and 2
Terminal number	Terminal connection
1	$\overline{OC}$
2	1D
3	2D
4	3D
5	4D
6	5D
7	6D
8	7D
9	8D
10	GND
11	CLK
12	8$\overline{Q}$
13	7$\overline{Q}$
14	6$\overline{Q}$
15	5$\overline{Q}$
16	4$\overline{Q}$
17	3$\overline{Q}$
18	2$\overline{Q}$
19	1$\overline{Q}$
20	V_{CC}

FIGURE 1. Terminal connections.

Inputs			Outputs
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low voltage level
H = High voltage level
↑ = Transition from low to high
X = Irrelevant
$\overline{Q}_0$ = $\overline{Q}$ level before steady-state input conditions were established.

FIGURE 2. Truth table.



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses have the following characteristics: PRR ≤ 10 MHz, duty cycle = 50%, $t_r = t_f$ = 3 ns ± 1 ns.
4. When measuring propagation delay times of three-state outputs, switch S1 is open.
5. The outputs are measured one at a time with one input transition per measurement.

FIGURE 3. Switching waveforms and test circuit.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-04-04

Approved sources of supply for SMD 5962-88728 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8872801RA	01295	SNJ54ALS564BJ
5962-8872801SA	01295	SNJ54ALS564BW
5962-88728012A	01295	SNJ54ALS564BFK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane PO Box 660199 Dallas, TX 75243 POC U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.