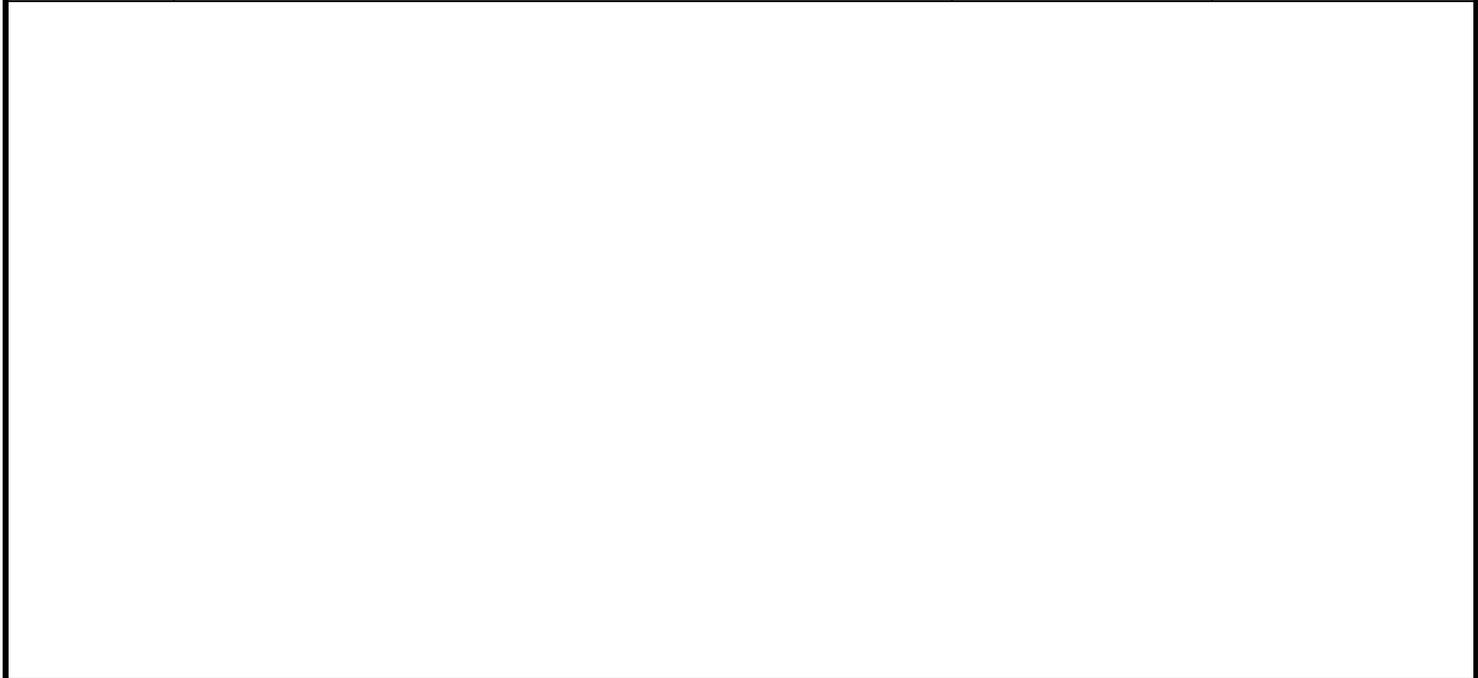


REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R345-92. - tvn	92-10-05	Monica Poelking
B	Changes in accordance with NOR 5962-R137-96. - les	96-06-05	Michael A. Frye
C	Add a new package outline letter F. - tdn	97-08-07	Raymond Monnin
D	Update to current requirements. Editorial changes throughout. - gap	06-06-05	Raymond Monnin
E	Update drawing to current MIL-PRF-38535 requirements. - jt	14-09-18	C. SAFFLE



REV																				
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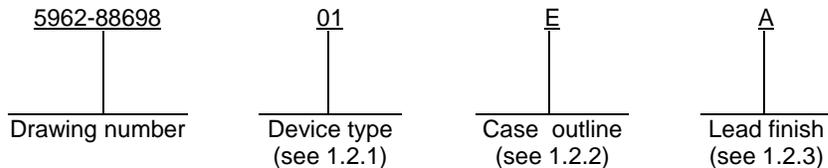
REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E							
	SHEET	1	2	3	4	5	6	7	8	9	10								

PMIC N/A	PREPARED BY Larry Gauder	<p align="center"><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a></p>																	
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Raymond Monnin																		
	APPROVED BY Dan DiCenzo	<p align="center">MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED LOW POWER SCHOTTKY TTL, SYNCHRONOUS 4-BIT UP/DOWN COUNTER, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 88-08-24																		
	REVISION LEVEL E	<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE <b>67268</b></td> <td><b>5962-88698</b></td> </tr> </table>	SIZE A	CAGE CODE <b>67268</b>	<b>5962-88698</b>														
SIZE A	CAGE CODE <b>67268</b>	<b>5962-88698</b>																	
		SHEET	1 OF 10																

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ALS193A	Synchronous 4-bit up/down counters

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	CDIP1-T16 or GDIP1-T16	16	Dual-in-line package
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range .....	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range .....	-1.5 V dc at -18 mA to +7.0 V dc
Storage temperature range .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+300°C
Junction temperature (T <sub>J</sub> ) .....	+175°C
Maximum power dissipation (P <sub>D</sub> ) <sup>1/</sup> .....	121 mW
Thermal resistance, junction-to-case (θ <sub>JC</sub> ) .....	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V <sub>CC</sub> ) .....	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V <sub>IH</sub> ) .....	+2.0 V dc
Maximum low level input voltage (V <sub>IL</sub> ):	
T <sub>C</sub> = +125°C .....	+0.7 V dc
T <sub>C</sub> = -55°C .....	+0.8 V dc
T <sub>C</sub> = +25°C .....	+0.8 V dc
High level output current (I <sub>OH</sub> ) .....	-0.4 mA
Low level output current (I <sub>OL</sub> ) .....	4 mA
Case operating temperature range (T <sub>C</sub> ) .....	-55°C to +125°C
Input setup time t <sub>SU</sub> :	
Data before $\overline{\text{LOAD}}$ ↑ .....	25 ns minimum
Clear inactive before UP ↑ or DOWN ↑ .....	20 ns minimum
$\overline{\text{LOAD}}$ inactive before UP ↑ or DOWN ↑ .....	20 ns minimum

<sup>1/</sup> Maximum power dissipation is defined as V<sub>CC</sub> x I<sub>CC</sub>, and must withstand the added P<sub>D</sub> to short circuit test; e.g., I<sub>O</sub>.

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1.4 Recommended operating conditions - Continued.

Input hold time  $t_h$ :

- Data after  $\overline{\text{LOAD}} \uparrow$  ..... 5 ns minimum
- UP high after DOWN  $\uparrow$  ..... 5 ns minimum
- DOWN high after UP  $\uparrow$  ..... 5 ns minimum

Input pulse width  $t_w$ :

- CLR high ..... 10 ns minimum
- $\overline{\text{LOAD}}$  low ..... 25 ns minimum
- UP or DOWN, high or low ..... 30 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

- MIL-STD-883 - Test Method Standard Microcircuits.
- MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

- MIL-HDBK-103 - List of Standard Microcircuit Drawings.
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

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3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime 's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

#### 4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified		Group A subgroups	Device Type	Limits		Unit
						Min	Max	
High level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -0.4 mA, V <sub>IH</sub> = 2.0 V <sup>2/</sup>	V <sub>IL</sub> = 0.7 V	2	01	2.5		V
			V <sub>IL</sub> = 0.8 V	1, 3	01			
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4.0 mA, V <sub>IH</sub> = 2.0 V <sup>2/</sup>	V <sub>IL</sub> = 0.7 V	2	01		0.4	V
			V <sub>IL</sub> = 0.8 V	1, 3	01			
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA		1, 2, 3	01		-1.5	V
Low level input current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4V, unused inputs ≥ 4.5 V	UP, DOWN	1, 2, 3	01		-0.2	mA
			All others				-0.1	
High level input current	I <sub>IH1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V, unused inputs = 0.0 V		1, 2, 3	01		20	μA
	I <sub>IH2</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 7.0 V, unused inputs = 0.0 V		1, 2, 3	01		0.1	mA
Output current	I <sub>O</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.25 V <sup>3/</sup>		1, 2, 3	01	-20	-112	mA
Supply current	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V <sup>4/</sup>		1, 2, 3	01		22	mA
Functional tests		See 4.3.1c <sup>5/</sup>		7, 8	01			
Clock frequency	f <sub>MAX</sub>	V <sub>CC</sub> = 4.5 to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω, See figure 3 <sup>6/</sup>		9, 10, 11	01	25		MHz
Propagation delay time, from UP to $\overline{CO}$	t <sub>PLH1</sub>			9, 10, 11	01	3	19	ns
	t <sub>PHL1</sub>					3	21	ns
Propagation delay time, from DOWN to $\overline{BO}$	t <sub>PLH2</sub>			9, 10, 11	01	4	19	ns
	t <sub>PHL2</sub>					5	21	ns
Propagation delay time, from UP or DOWN to any Q	t <sub>PLH3</sub>			9, 10, 11	01	3	23	ns
	t <sub>PHL3</sub>					4	20	ns
Propagation delay time, from $\overline{LOAD}$ to any Q	t <sub>PLH4</sub>			9, 10, 11	01	7	38	ns
	t <sub>PHL4</sub>					8	37	ns
Propagation delay time, from CLR to any Q	t <sub>PHL5</sub>			9, 10, 11	01	5	20	ns

See footnotes on next page.

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TABLE I. Electrical performance characteristics - Continued.

- 1/ Unused inputs that do not directly control the pin under test must be  $\geq 2.5$  V or  $\leq 0.4$  V. No unused inputs shall exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.
- 2/ All outputs must be tested. In the case where only one input at  $V_{IL}$  maximum or  $V_{IH}$  minimum produces the proper state, the test must be performed with each input being selected as the  $V_{IL}$  maximum or  $V_{IH}$  minimum input.
- 3/ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current,  $I_{OS}$ . Not more than one output will be tested at one time and duration of test shall not exceed one second.
- 4/  $I_{CC}$  is measured with the CLR and  $\overline{LOAD}$  inputs grounded and all other inputs at 4.5 V.
- 5/ Functional tests shall be conducted at input test conditions of  $GND \leq V_{IL} \leq V_{OL}$  and  $V_{OH} \leq V_{IH} \leq V_{CC}$ .
- 6/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or  $\leq 0.3$  V.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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Case outline	E and F	2
Terminal number	Terminal symbol	
1	B	NC
2	QB	B
3	QA	QB
4	DOWN	QA
5	UP	DOWN
6	QC	NC
7	QD	UP
8	GND	QC
9	D	QD
10	C	GND
11	$\overline{\text{LOAD}}$	NC
12	$\overline{\text{CO}}$	D
13	$\overline{\text{BO}}$	C
14	CLR	$\overline{\text{LOAD}}$
15	A	$\overline{\text{CO}}$
16	V <sub>cc</sub>	NC
17	---	$\overline{\text{BO}}$
18	---	CLR
19	---	A
20	---	V <sub>cc</sub>

FIGURE 1. Terminal connections.

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Inputs				Output
CLR	$\overline{\text{LOAD}}$	UP	DOWN	
H	X	X	X	Clear
L	L	X	X	Data to outputs
L	H	↑	H	Count up
L	H	H	↑	Count down

Inputs		Outputs		
UP	DOWN	Count	$\overline{\text{BO}}$	$\overline{\text{CO}}$
H	L	0	$\overline{\text{L}}$	H
L	H	15	H	$\overline{\text{L}}$
All other conditions			H	H

$\overline{\text{L}}$  = Low level pulse  
 L = Low  
 H = High  
 X = Irrelevant  
 ↑ = Clock transition low to high

FIGURE 2. Truth tables.

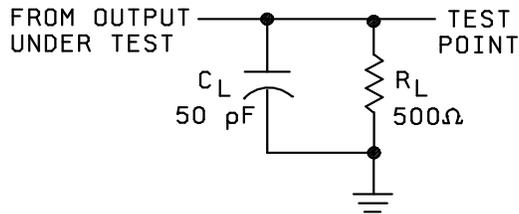
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SIZE  
**A**

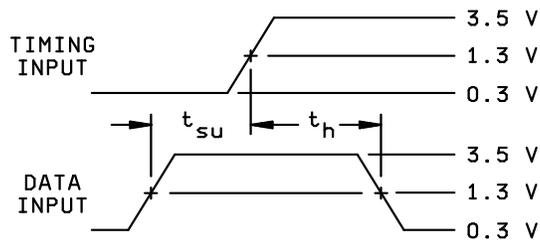
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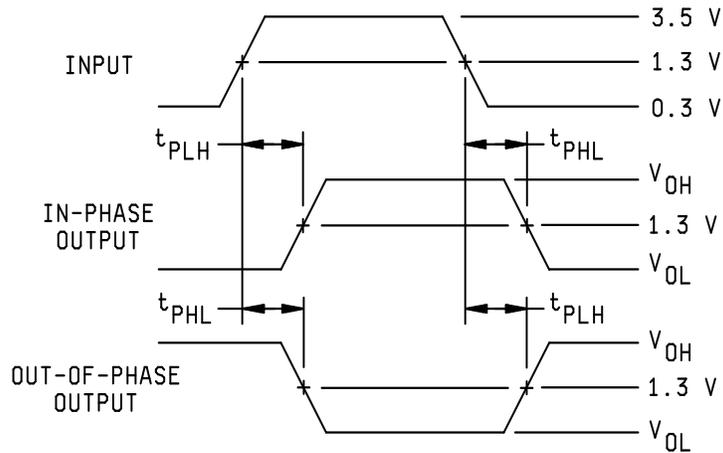
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TEST CIRCUIT



SETUP AND HOLD TIMES



NOTES:

1.  $C_L$  includes probe and jig capacitance.
2. All input pulses have the following characteristics: PRR  $\leq$  10 MHz, duty cycle = 50%,  $t_r = t_f = 3 \text{ ns} \pm 1 \text{ ns}$ .

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3. The outputs are measured one at a time with one input transition per measurement.

FIGURE 3. Test circuit and switching waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

\* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-09-18

Approved sources of supply for SMD 5962-88698 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8869801EA	01295	SNJ54ALS193AJ
5962-8869801FA	01295	SNJ54ALS193AW
5962-88698012A	01295	SNJ54ALS193AFK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

01295

Vendor name  
and address

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Ln  
PO Box 660199  
Dallas, TX 75243

POC: U.S. Highway 75 South  
P.O. Box 84, M/S 853  
Sherman, TX 75090-9493

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