

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. Editorial changes throughout. - drw	00-12-21	Raymond Monnin
B	Redraw. Update drawing to current requirements. - drw	11-08-15	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

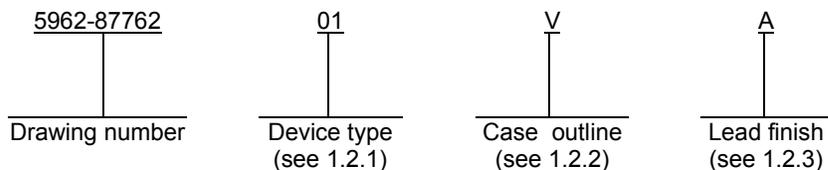
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OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11								

PMIC N/A <p style="text-align: center;">STANDARD MICROCIRCUIT DRAWING</p> <p style="text-align: center;">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p style="text-align: center;">AMSC N/A</p>	PREPARED BY <p style="text-align: center;">Marcia B. Kelleher</p> <hr/> CHECKED BY <p style="text-align: center;">Ray Monnin</p> <hr/> APPROVED BY <p style="text-align: center;">D. A. DiCenzo</p> <hr/> DRAWING APPROVAL DATE <p style="text-align: center;">88-07-25</p> <hr/> REVISION LEVEL <p style="text-align: center;">B</p>	<p>DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p> <hr/> <p>MICROCIRCUIT, LINEAR, 8-BIT, ANALOG-TO-DIGITAL CONVERTER, WITH TRACK/HOLD, MONOLITHIC SILICON</p> <hr/> <table style="width: 100%; border: none;"> <tr> <td style="width: 15%; border: none;">SIZE A</td> <td style="width: 20%; border: none;">CAGE CODE 67268</td> <td style="width: 65%; border: none;">5962-87762</td> </tr> </table> <hr/> <p style="text-align: center;">SHEET 1 OF 11</p>	SIZE A	CAGE CODE 67268	5962-87762
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1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	7575S	Monolithic CMOS 8-bit A/D converter with track/hold amplifier, 5 μs conversion time and 7-bit linearity
02	7575T	Monolithic CMOS 8-bit A/D converter with track/hold amplifier, 5 μs conversion time and 8-bit linearity

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V _{DD} to AGND	-0.3 V dc to +7.0 V dc
V _{DD} to DGND	-0.3 V dc to +7.0 V dc
AGND to DGND	-0.3 V dc to V _{DD}
Digital input voltage to DGND (Pins \overline{CS} , \overline{RD})	-0.3 V dc to V _{DD}
Digital input voltage to DGND: (Pins BUSY, DB0 to DB7)	-0.3 V dc to V _{DD}
CLK input voltage to DGND	-0.3 V dc to V _{DD}
V _{REF} to AGND	-0.3 V dc to V _{DD}
A _{IN} to AGND	-0.3 V dc to V _{DD}
Power dissipation (P _D) cases V and 2: Up to +75°C	450 mW
Derate above +75°C	6 mW/°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ _{JC}) (cases V and 2)	See MIL-STD-1835
Thermal resistance, junction-to-case (θ _{JA}) (cases V and 2)	120°C/W

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1.4 Recommended operating conditions.

Ambient operating temperature range (T _A)	-55°C to +125°C
Power supply voltage (V _{DD})	5 V dc ±5%
Reference voltage (V _{REF})	1.23 V dc
AGND = DGND	0 V dc
External clock frequency (f _{CLK})	4 MHz
Analog input voltage range	0 V to 2 V _{REF} (1 LSB = 2 V _{REF} /256)

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional diagram. The functional diagram shall be as specified on figure 2.

3.2.4 Timing test circuits and diagrams. The timing test circuits and diagrams shall be as specified on figure 3 and 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES			All	8		Bits
Total unadjusted error	TUE		1	All	-2	+2	LSB
			2, 3	01	-2	+2	
				02	-1	+1	
12	02	-1	+1				
Relative accuracy	RA		1	All	-1	+1	LSB
			2, 3	01	-1	+1	
				02	-0.5	+0.5	
12	02	-0.5	+0.5				
Full scale error	AE		1, 2, 3	All	-1	+1	LSB
Offset error <u>2/</u>	EOS		1, 2, 3	All	-0.5	+0.5	LSB
DC input impedance	Z _{IH}		1, 2, 3	All	10		MΩ
Reference input current	I _{REF}		1, 2, 3	All		500	μA
Digital input low voltage	V _{IL}	\overline{CS} , \overline{RD} , CLK	1, 2, 3	All		0.8	V
Digital input high voltage	V _{IH}	\overline{CS} , \overline{RD} , CLK	1, 2, 3	All	2.4		V
Digital input current	I _{IN}	\overline{CS} , \overline{RD} , V _{IN} = 0 V or V _{DD} , V _{DD} = 5.25 V	1	All	-1	+1	μA
			2, 3		-10	+10	
Digital input low current	I _{IL}	CLK; V _{IL} = 0 V	1, 2, 3	All	-800	+800	μA
Digital input high current	I _{IH}	CLK; V _{IH} = V _{DD}	1, 2, 3	All	-800	+800	μA
Digital output low voltage	V _{OL}	\overline{BUSY} , DB0 to DB7, I _{SINK} = 1.6 mA, V _{DD} = 4.75 V	1, 2, 3	All		0.4	V
Digital output high voltage	V _{OH}	\overline{BUSY} , DB0 to DB7, I _{SOURCE} = -40 μA, V _{DD} = 4.75 V	1, 2, 3	All	4.0		V
Floating state leakage current	I _{OUT}	DB0 to DB7, V _{OUT} = 0 V to V _{DD} , V _{DD} = 5.25 V	1, 2, 3	All	-10	+10	μA
Power supply current <u>3/</u>	I _{DD}		1, 2, 3	All		7	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply rejection ratio	PSRR	4.75 V ≤ V _{DD} ≤ 5.25 V	1, 2, 3	All	-0.25	+0.25	LSB
Digital input capacitance	C _{IN}	CS, RD, T _A = +25°C, see 4.3.1c	4	All		10	pF
Floating state output capacitance	C _{OUT}	DB0 to DB7, T _A = +25°C, see 4.3.1c	4	All		10	pF
Conversion time with external clock	t _{CONV}	f _{CLK} = 4 MHz, T _A = +25°C	4	All		5	μs
Slew rate, tracking	SR	T _A = +25°C	4	All		0.386	V/μs
Signal to noise ratio	SNR	V _{IN} = 2.46 V _{P-P} at 10 kHz, T _A = +25°C	4	All	45		dB
Conversion time with internal clock	t _{CONV}	R = 100 kΩ, C _L = 100 pF	9, 10, 11	All	5	15	μs
CS to RD, setup time, t ₁	t _{WSCS}	See figure 4	9, 10, 11	All	0		ns
RD to BUSY propagation delay, t ₂	t _{WPBD}	See figure 4	9	All		100	ns
			10, 11			120	
Data access time after RD, t ₃ <u>4/</u>	t _{DAR}	See figure 4	9	All		100	ns
			10, 11			120	
RD pulse width, t ₄	t _{RD}	See figure 4	9	All	100		ns
			10, 11		120		
CS to RD hold time, t ₅	t _{RHS}	See figure 4	9, 10, 11	All	0		ns
Data access time after BUSY, t ₆ <u>4/</u>	t _{DAB}	See figure 4	9	All		80	ns
			10, 11			100	
Data hold time, t ₇ <u>5/</u>	t _{DH}	See figure 4	9	All	10	80	ns
			10, 11		10	100	
BUSY to CS delay, t ₈	t _{BCD}	See figure 4	9, 10, 11	All	0		ns

1/ The minimum resolution for which no missing code is guaranteed is 8-bits. All input control signals are specified with t_r = t_f = 20 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V (see 1.4). V_{DD} = +5 V, V_{REF} = +1.23 V, unless otherwise specified.

2/ Offset error is measured with respect to an ideal code transition which occurs at 0.5 LSB.

3/ Power supply current is measured when the device is inactive, i.e., when CS = RD = BUSY = logic HIGH.

4/ t₃ and t₆, are measured with the load circuit of figure 3 and defined as the time required for an output to cross 0.8 V or 2.4 V.

5/ t₇ is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of figure 3 and is measured only for the initial test and after process or design changes which may affect t₇.

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Device type	01 and 02	
Case outline	V	2
Terminal number	Terminal symbol	
1	$\overline{\text{CS}}$	$\overline{\text{CS}}$
2	$\overline{\text{RD}}$	$\overline{\text{RD}}$
3	$\overline{\text{TP}}$	$\overline{\text{TP}}$
4	$\overline{\text{BUSY}}$	$\overline{\text{BUSY}}$
5	CLK	CLK
6	DB7 (MSB)	DB7 (MSB)
7	DB6	DB6
8	DB5	DB5
9	DGND	DGND
10	DB4	NC
11	DB3	NC
12	DB2	DB4
13	DB1	DB3
14	DB0 (LSB)	DB2
15	AGND	DB1
16	AIN	DB0 (LSB)
17	V_{REF}	AGND
18	V_{DD}	AIN
19	---	V_{REF}
20	---	V_{DD}

NC = no connection

FIGURE 1. Terminal connections.

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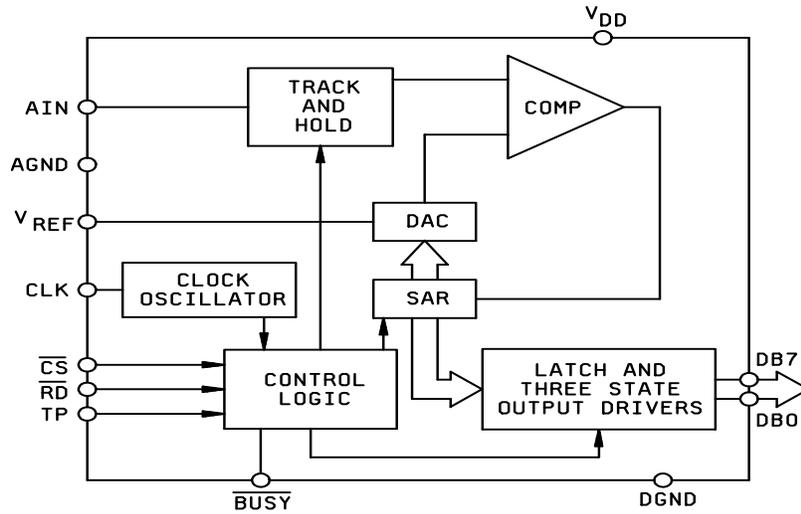
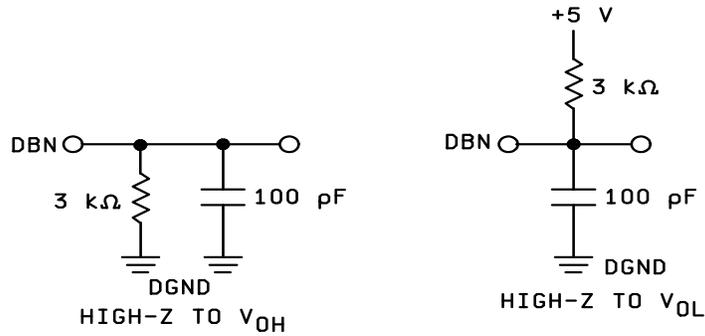


FIGURE 2. Functional diagram.

LOAD CIRCUITS FOR DATA ACCESS TIME TEST



LOAD CIRCUITS FOR DATA HOLD TIME TEST

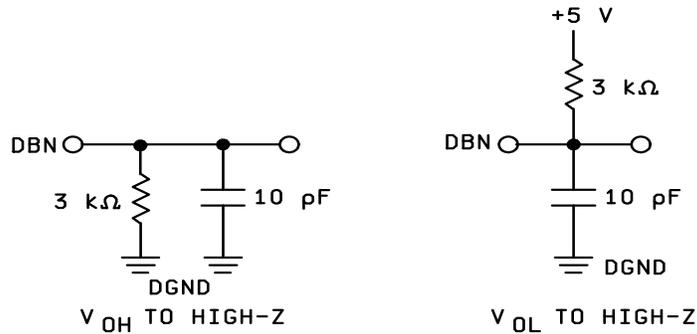


FIGURE 3. Timing test circuits.

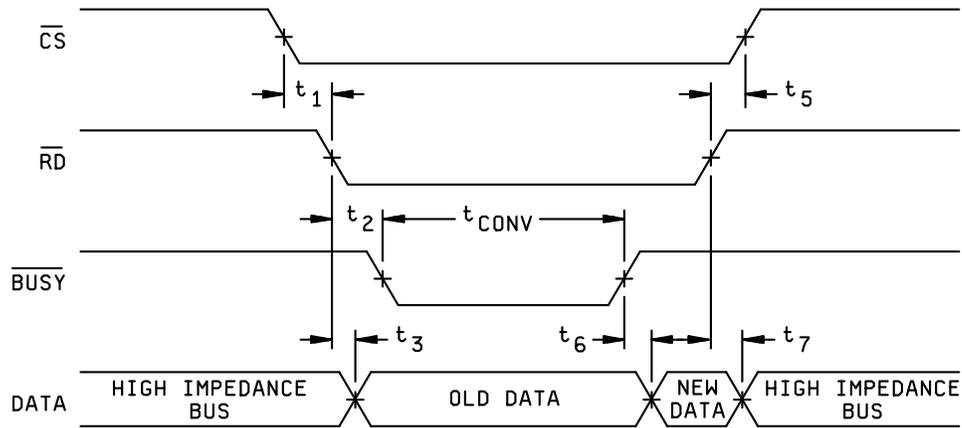
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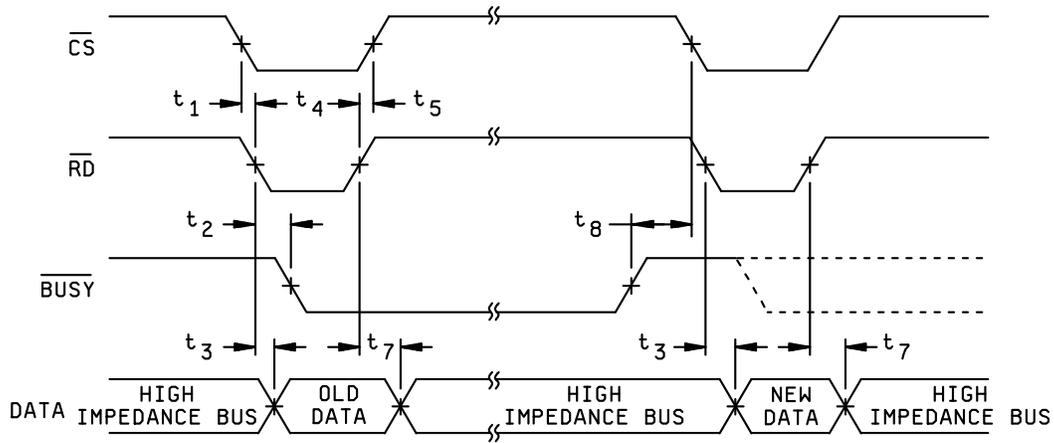
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SLOW MEMORY INTERFACE



ROM INTERFACE

FIGURE 4. Timing diagrams.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- c. Optional subgroup 12 is used for grading and part selection at $+25^{\circ}\text{C}$, not included in PDA.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 12
Group A test requirements (method 5005)	1, 2, 3, 4, 9, (10, 11)**, 12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

** Subgroups 10 and 11 are guaranteed, if not tested, to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.
- d. Optional subgroup 12 is used for grading and part selection at $+25^{\circ}\text{C}$.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-08-15

Approved sources of supply for SMD 5962-87762 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8776201VA	<u>3/</u>	AD7575SQ/883B
5962-87762012A	<u>3/</u>	AD7575SE/883B
5962-8776202VA	24355	AD7575TQ/883B
5962-87762022A	<u>3/</u>	AD7575TE/883B

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE number

24355

Vendor name and address

Analog Devices
 Rt 1 Industrial Park
 PO Box 9106
 Norwood, MA 02062
 Point of contact:
 Raheen Business Park
 Limerick, Ireland

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