REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with N.O.R. 5962-R151-92.	92-04-15	M. A. FRYE
B	Add device class V devices. Redrawn. - ro	00-11-09	R. MONNIN
C	Update boilerplate to reflect current requirements. -rrp	03-04-22	R. MONNIN
D	Update drawing as part of 5 year review. - jt	10-12-08	C. SAFFLE

REV																			
SHEET																			
REV																			
SHEET																			
REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D					
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13					

PMIC N/A

PREPARED BY
MARCIA B. KELLEHER

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COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAY MONNIN

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
88-03-24

MICROCIRCUIT, LINEAR, HIGH EFFICIENCY LINEAR REGULATOR, MONOLITHIC SILICON

REVISION LEVEL
D

SIZE	CAGE CODE	
A	**67268**	**5962-87742**

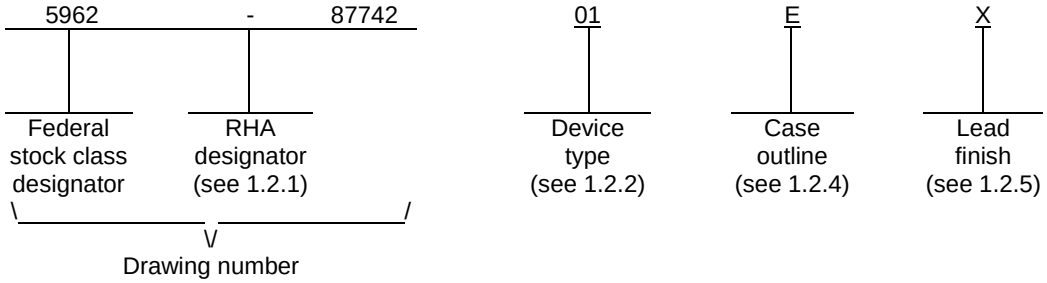
SHEET 1 OF 13

1. SCOPE

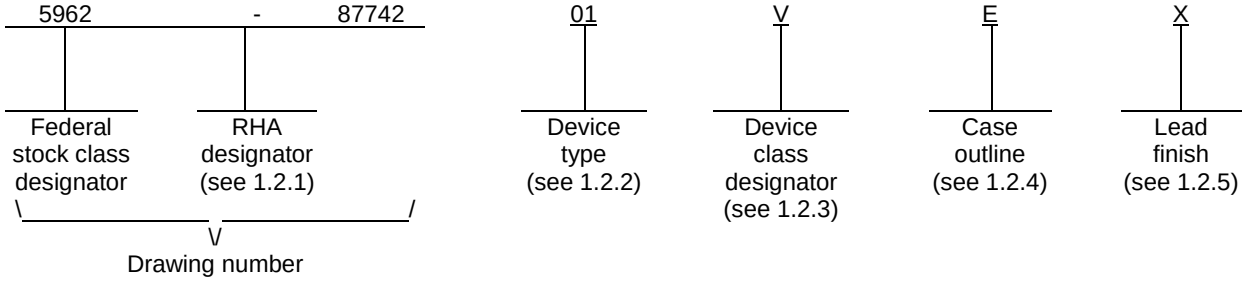
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	1834	High efficiency linear regulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Input supply voltage ($+V_{IN}$) ..... 40 V dc
Driver current ..... 400 mA
Driver source to sink voltage ..... 40 V dc
Crowbar current ..... -200 mA
+1.5 V reference output current ..... -10 mA
Fault alert voltage ..... 40 V dc
Fault alert current ..... 15 mA
Error amplifier inputs ..... -0.5 V dc to +35 V dc
Current sense inputs ..... -0.5 V dc to +40 V dc
0 V latch output voltage ..... -0.5 V dc to +40 V dc
0 V latch output current ..... 15 mA
Power dissipation (P_D):
T_A = +50°C ..... 1000 mW 3/
T_C = +25°C ..... 2000 mW 4/
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Junction temperature (T_J) ..... +150°C
Thermal resistance, junction-to-ambient (θ_{JA}):
Case E ..... 80°C/W
Case 2 ..... 70°C/W
Thermal resistance, junction-to-case (θ_{JC}):
Cases E and 2 ..... See MIL-STD-1835

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Voltages are referenced to pin 5 ($-V_{IN}$). Currents are positive into, negative out of the specified terminals.
3/ Derate above T_A = +50°C at 10 mW/°C for case E and derate above T_A = +40°C at 9 mW/°C for case 2.
4/ Derate above T_C = +25°C at 16 mW/°C for case E and derate above T_C = +120°C at 67 mW/°C for case 2.

SPECIFICATION

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 2 .

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Standby supply current	I_{SBY}		1,2,3	01		7.0	mA
+1.5 V Reference section							
Output voltage	V_{OUT1}	-55°C ≤ T_J ≤ +125°C	1	01	1.485	1.515	V
			2,3		1.47	1.53	
Line regulation	V_{RLINE1}	$+V_{IN}$ = 5.0 V to 35 V	1,2,3	01		10	mV
Load regulation	V_{RLOAD1}	I_{OUT} = 0 mA to 2.0 mA	1,2,3	01		10	mV
-2.0 V Reference section 2/							
Output voltage (referenced to $+V_{IN}$)	V_{OUT2}	-55°C ≤ T_J ≤ +125°C	1	01	2.04	1.96	V
			2,3		2.06	1.94	
Line regulation	V_{RLINE2}	$+V_{IN}$ = 5.0 V to 35 V	1,2,3	01		15	mV
Error amplifier section							
Input offset voltage	V_{OS}	V_{CM} = 1.5 V	1,2,3	01		6.0	mV
Input bias current	I_{IB1}	V_{CM} = 1.5 V	1,2,3	01		-4.0	µA
Input offset current	I_{OS}	V_{CM} = 1.5 V	1,2,3	01		1.0	µA
Small signal open loop gain	AVOL	COMPENSATION / SHUTDOWN pin is output, DIVER SINK pin is $+V_{IN}$, DRIVER SOURCE pin is connected through 20 Ω resistor to $-V_{IN}$	4,5,6	01	50		dB
Common mode rejection ratio	CMRR	V_{CM} = 0.5 V to 33 V, $+V_{IN}$ = 35 V	4,5,6	01	60		dB
Power supply rejection ratio	PSRR	$+V_{IN}$ = 5.0 V to 35 V, V_{CM} = 1.5 V	4,5,6	01	70		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Driver section 3/							
Maximum output current	I_{OUT} (max)		1,2,3	01	200		mA
Saturation voltage	V_{SAT}	I_{OUT} = 100 mA	1,2,3	01		1.2	V
Output leakage current	I_{LO}	DRIVER SINK pin is 35 V, DRIVER SOURCE pin is -V_{IN}, COMPENSATION / SHUTDOWN pin is -V_{IN}	1,2,3	01		50	μA
Shutdown input voltage at COMPENSATION / SHUTDOWN pin	V_{IN} (SHTDN)	I_{OUT} ≤ 100 μA, DRIVER SOURCE pin is -V_{IN}, DRIVER SINK pin is +V_{IN}	1,2,3	01	0.4		V
Shutdown input current at COMPENSATION / SHUTDOWN pin	I_{IN} (SHTDN)	I_{OUT} ≤ 100 μA, COMPENSATION / SHUTDOWN pin is -V_{IN}, DRIVER SINK pin is +V_{IN}, DRIVER SOURCE pin is -V_{IN}	1,2,3	01		-150	μA
Fault amplifier section							
Under-and over-voltage fault threshold	V_{TH1}	V_{CM} = 1.5 V, at E/A inputs	1,2,3	01	120	180	mV
Common-mode sensitivity	V_{CMS}	+V_{IN} = 35 V, V_{CM} = 1.5 V to 33 V	1,2,3	01		-0.8	%/V
Supply sensitivity	V_{SS}	V_{CM} = 1.5 V, +V_{IN} = 5.0 V to 35 V	1,2,3	01		-1.0	%/V
Fault delay	tFD		9,10,11	01	30	60	ms/μF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Fault amplifier section – continued.							
Fault alert output current at FAULT ALERT pin	I_{OUT}		1,2,3	01	2.0		mA
Fault alert saturation voltage at FAULT ALERT pin	V_{SAT}	I_{OUT} = 1.0 mA	1,2,3	01		0.5	V
0 V latch current at 0 V LATCH OUTPUT / RESET pin	I_{OUT}		1,2,3	01	2.0		mA
0 V latch saturation voltage at 0 V LATCH OUTPUT / RESET pin	V_{SAT}	I_{OUT} = 1.0 mA	1,2,3	01		1.3	V
0 V latch output reset voltage	V_{RESET}		1,2,3	01	0.3	0.6	V
Crowbar gate current at CROWBAR GATE pin	I_{OUT}		1,2,3	01	-100		mA
Crowbar gate leakage current at CROWBAR GATE pin	I_{LO}	$+V_{IN}$ = 35 V, CROWBAR GATE pin is $-V_{IN}$	1,2,3	01		-50	µA
Current sense amplifier section							
Threshold voltage	V_{TH2}	THRESHOLD ADJ pin is open, V_{CM} = $+V_{IN}$ or $-V_{IN}$	1,2,3	01	130	170	mV
		THRESHOLD ADJ pin is 0.5 V, V_{CM} = $+V_{IN}$ or $-V_{IN}$			40	60	
Threshold supply sensitivity	ΔV_{TH2} / $\Delta +V_{IN}$	$+V_{IN}$ = 5.0 V to 35 V, THRESHOLD ADJ pin is open, V_{CM} = $-V_{IN}$	1,2,3	01		-0.3	%/V
Adjustment input current	I_{IN}	THRESHOLD ADJ pin is 0.5 V	1,2,3	01		-10	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Current sense amplifier section – continued.							
Sense input bias current	I_{IB2}	$V_{CM} = +V_{IN}$	1,2,3	01		200	µA
		$V_{CM} = -V_{IN}$				-200	

1/ Unless otherwise specified, $+V_{IN}$ = 15 V, $-V_{IN}$ = 0 V, and T_A = -55°C to +125°C.

2/ When using both the 1.5 V and –2.0 V reference, the current out of +1.5 V REF pin should be balanced by an equivalent current into –2.0 V REF pin. The –2.0 V output will change –2.3 mV per µA imbalance.

3/ The driver section contains a thermal shutdown which turns the driver off at approximately +165°C. If 0 V LATCH OUTPUT pin is tied to the COMPENSATION / SHUTDOWN pin, the 0 V latch will be reset.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime 's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 52 (see MIL-PRF-38535, appendix A).

Device type	01	
Case outlines	E	2
Terminal number	Terminal symbol	
1	$+V_{IN}$	NC
2	-2.0 V REF	$+V_{IN}$
3	+1.5 V REF	-2.0 V REF
4	THRESHOLD ADJ	+1.5 V REF
5	$-V_{IN}$	THRESHOLD ADJ
6	-SENSE	NC
7	+SENSE	$-V_{IN}$
8	N INV INPUT	-SENSE
9	INV INPUT	+SENSE
10	FAULT ALERT	N INV INPUT
11	FAULT DELAY	NC
12	DRIVER SINK	INV INPUT
13	DRIVER SOURCE	FAULT ALERT
14	COMPENSATION / SHUTDOWN	FAULT DELAY
15	0 V LATCH OUTPUT / RESET	DRIVER SINK
16	CROWBAR GATE	NC
17	---	DRIVER SOURCE
18	---	COMPENSATION / SHUTDOWN
19	---	0 V LATCH OUTPUT / RESET
20	---	CROWBAR GATE

NC = No connection

FIGURE 1. Terminal connections.

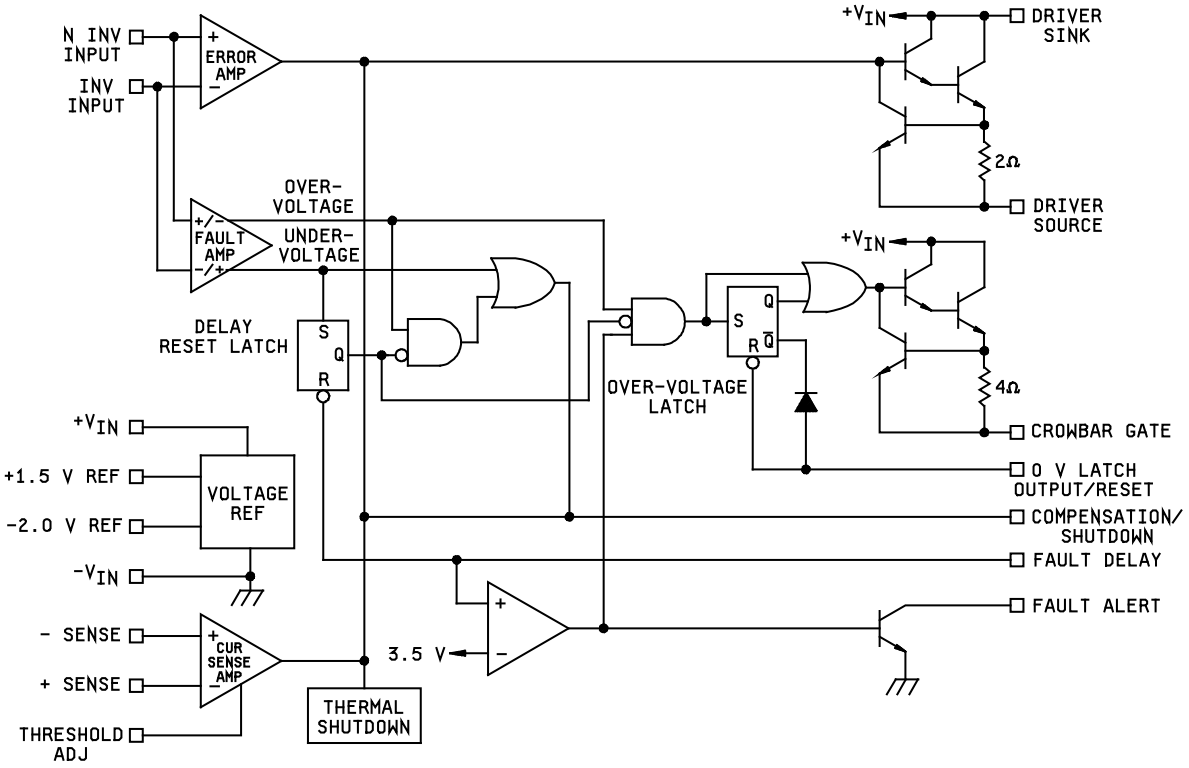


FIGURE 2. Logic diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 4, 9 1/	1, 2, 3, 4, 9 1/	1, 2, 3, 4, 9, 1/, 2/
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-12-08

Approved sources of supply for SMD 5962-87742 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8774201EA	01295	UC1834J/883B
5962-87742012A	01295	UC1834L/883B
5962-8774201VEA	01295	UC1834JQMLV
5962-8774201V2A	01295	UC1834LQMLV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.