

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add case outline C. Made corrections to timing test limits. Editorial changes throughout.	90-02-02	M. A. Frye
B	Drawing updated to reflect current requirements. - ro	02-08-23	R. Monnin
C	Redrawn. Paragraphs updated to MIL-PRF-38535 requirements. - drw	15-01-28	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.



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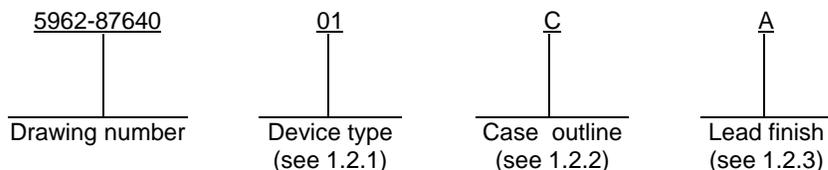
REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12				

PMIC N/A	PREPARED BY Joseph A. Kerby	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil													
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Ray Monnin														
	APPROVED BY Michael A. Frye	MICROCIRCUIT, LINEAR, BIMOS II LATCHED DRIVERS, MONOLITHIC SILICON													
	DRAWING APPROVAL DATE 88-04-08														
	REVISION LEVEL C		SIZE A	CAGE CODE 67268	5962-87640										
		SHEET 1 OF 12													

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	5801	BIMOS II 8-bit latched drivers
02	5800	BIMOS II 4-bit latched drivers

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
W	GDIP1-T22 or CDIP2-T22	22	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (V_{DD})	15 V dc
Continuous collector current (I_C)	500 mA
Input voltage range (V_{IN})	-0.3 V dc to $V_{DD} + 0.3$ V dc
Output voltage (V_{CE})	50 V dc
Maximum power dissipation (P_D)	1.75 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction to case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction to ambient (θ_{JA})	65°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	5 V dc to 12 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.4 Functional diagram. The functional diagram shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Timing diagram. The timing diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output leakage current	I _{CEX}	V _{CE} = 50 V, V _{DD} = 5 V	1	All		50	μA
			2, 3			100	
Collector emitter saturation voltage	V _{CE} (SAT)	I _C = 100 mA, V _{DD} = 5 V	1	All		1.1	V
		I _C = 200 mA, V _{DD} = 5 V				1.3	
		I _C = 350 mA, V _{DD} = 7 V				1.6	
		I _C = 100 mA, V _{DD} = 5 V	2, 3			1.3	
		I _C = 200 mA, V _{DD} = 5 V				1.5	
		I _C = 350 mA, V _{DD} = 7 V				1.8	
Input voltage	V _{IN(0)}	V _{DD} = 5 V	4, 5, 6	All		1.0	V
	V _{IN(1)}	V _{DD} = 12 V <u>1/</u>	4, 5		10.5		
		V _{DD} = 10 V <u>1/</u>			8.5		
		V _{DD} = 5 V <u>1/</u>			3.5		
	V _{IN(1)}	V _{DD} = 12 V <u>1/</u>	6		11		
		V _{DD} = 10 V <u>1/</u>			9		
		V _{DD} = 5 V <u>1/</u>			3.6		
Input resistance	R _{IN}	V _{DD} = 12 V	1, 2	All	50		kΩ
		V _{DD} = 10 V			50		
		V _{DD} = 5 V			50		
		V _{DD} = 12 V	3		35		
		V _{DD} = 10 V			35		
		V _{DD} = 5 V			35		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Supply current	I _{DD(on)} (each stage)	V _{DD} = 12 V, outputs open	1, 2	All		2.0	mA	
		V _{DD} = 10 V, outputs open				1.7		
		V _{DD} = 5 V, outputs open				1.0		
	I _{DD(off)} (total)	V _{DD} = 12 V, outputs open, inputs = 0 V	3			2.5		
					V _{DD} = 10 V, outputs open			2.1
					V _{DD} = 5 V, outputs open			1.0
Clamp diode leakage current	I _R	V _{DD} = 5 V, V _R = 50 V	1, 3	All		50	μA	
			2			100		
Clamp diode forward voltage	V _F	V _{DD} = 5 V, I _F = 350 mA	1, 2	All		2.0	V	
			3			2.1		
Functional tests		See 4.3.1c	7	All				
Timing conditions 2/								
Minimum data active time before strobe enabled (data setup time)	t _S	V _{DD} = 5 V	9	All	50		ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing conditions – continued. <u>2/</u>							
Minimum data active time after strobe disabled (data hold time)	t _H	V _{DD} = 5 V	9	All	50		ns
Minimum strobe pulse width	t _{SPW}	V _{DD} = 5 V	9	All	125		ns
Minimum clear pulse width	t _{CPW}	V _{DD} = 5 V	9	All	300		ns
Minimum data pulse width	t _{DPW}	V _{DD} = 5 V	9	All	225		ns

1/ Operation of these devices with standard TTL or DTL may require the use of appropriate pullup resistors to insure a minimum logic "1".

2/ See figure 4.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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Device types	01	02
Case outlines	W	C
Terminal number	Terminal symbol	
1	CLEAR	CLEAR
2	STROBE	STROBE
3	IN ₁	IN ₁
4	IN ₂	IN ₂
5	IN ₃	IN ₃
6	IN ₄	IN ₄
7	IN ₅	GROUND
8	IN ₆	COMMON
9	IN ₇	OUT ₄
10	IN ₈	OUT ₃
11	GROUND	OUT ₂
12	COMMON	OUT ₁
13	OUT ₈	V _{DD}
14	OUT ₇	OUTPUT ENABLE
15	OUT ₆	---
16	OUT ₅	---
17	OUT ₄	---
18	OUT ₃	---
19	OUT ₂	---
20	OUT ₁	---
21	V _{DD}	---
22	OUTPUT ENABLE	---

FIGURE 2. Terminal connections.

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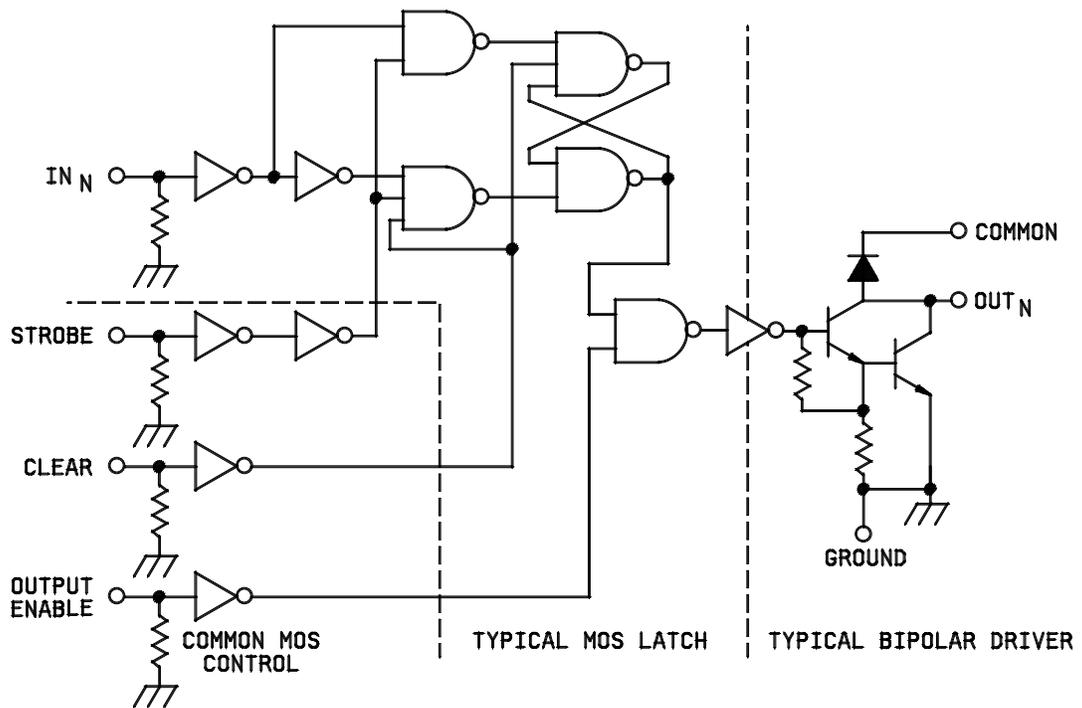


FIGURE 2. Functional diagram.

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IN _N	STROBE	CLEAR	OUTPUT ENABLE	OUT _N	
				t - 1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = Irrelevant.

t - 1 = Previous output state.

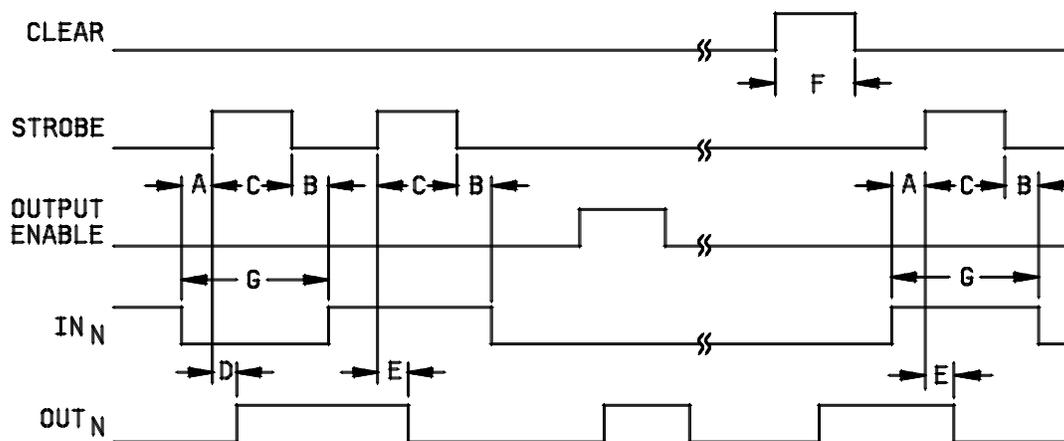
t = Present output state.

NOTES:

1. Information present at an input is transferred to its latch when the "strobe" input is high.
2. A high "clear" input will set all latches to the output off condition regardless of the data or strobe input levels.
3. A high "output enable" will set all outputs to the off condition regardless of any other input conditions.
4. When "output enable" is low, the outputs depend on the state of their respective latches.

FIGURE 3. Truth table.

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- A. Minimum data active time before strobe enabled (data setup time) 50 ns
- B. Minimum data active time after strobe disabled (data hold time) 50 ns
- C. Minimum strobe pulse width 125 ns
- D. Typical time between strobe activation and output on to off transition 500 ns
- E. Typical time between strobe activation and output off to on transition 500 ns
- F. Minimum clear pulse width 300 ns
- G. Minimum data pulse width 225 ns

FIGURE 4. Timing diagram.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 7, 9
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 8, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 shall include verification of the truth table.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-01-28

Approved sources of supply for SMD 5962-87640 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8764001WA	60496	MIC5801AJBQ
	<u>3/</u>	UCS-5801H-883
5962-8764002CA	<u>3/</u>	MIC5800AJBQ
	<u>3/</u>	UCS-5800H-883

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE number

60496

Vendor name and address

Micrel, Inc.
1849 Fortune Drive
San Jose, CA 95131-1724

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.