

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make changes to table I, 1.4, figure 1 and throughout. Add a new figure to the drawing. Editorial changes throughout.	90-03-06	M. A. Frye
B	Drawing updated to reflect current requirements. - ro	02-08-20	R. Monnin
C	Redrawn. Update paragraphs to MIL-PRF-38535 requirements. - drw	14-12-11	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

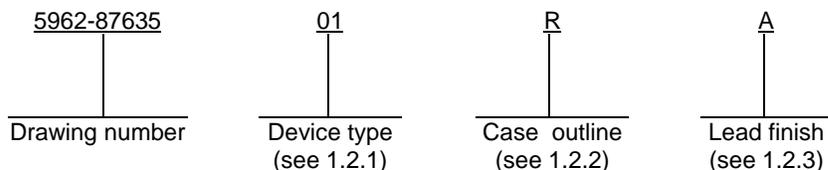
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REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A	PREPARED BY Rick C. Officer	<p align="center"><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a></p>															
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Charles E. Besore																
	APPROVED BY Michael A. Frye	<p align="center">MICROCIRCUIT, LINEAR, 8-BIT A/D CONVERTER WITH INPUT AMPLIFIER, MONOLITHIC SILICON</p>															
	DRAWING APPROVAL DATE 88-11-23																
	REVISION LEVEL C	SIZE A	CAGE CODE <b>67268</b>	<b>5962-87635</b>													
		SHEET		1 OF 14													

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identifies the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	AD670	8-bit A/D converter with input amplifier

1.2.2 Case outline. The case outline are as designated in MIL-STD-1835 as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V <sub>CC</sub> to ground .....	0 V dc to +7.5 V dc
Digital inputs:	
BPO/ $\overline{UPO}$ , FORMAT, R/ $\overline{W}$ , $\overline{CS}$ , $\overline{CE}$ pins .....	-0.5 V dc to V <sub>CC</sub> +0.5 V dc
Digital outputs:	
DB0 – DB7, STATUS OUTPUT pins .....	Momentary short to V <sub>CC</sub> or ground
Analog inputs:	
V <sub>IN-</sub> (HIGH), V <sub>IN-</sub> (LOW), V <sub>IN+</sub> (HIGH), V <sub>IN+</sub> (LOW) pins .....	-30 V dc to +30 V dc
Power dissipation (P <sub>D</sub> ) .....	450 mW
Storage temperature range .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	See MIL-STD-1835
Thermal resistance, junction-to-ambient ( $\theta_{JA}$ ) .....	85°C/W

1.4 Recommended operating conditions.

Supply voltage range (V <sub>CC</sub> ) .....	4.75 V dc to 5.5 V dc
Operating ambient temperature range (T <sub>A</sub> ) .....	-55°C to +125°C

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figures 2, 3, and 4.

3.2.4 Block diagram. The block diagram shall be as specified on figure 5.

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3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C V <sub>CC</sub> = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Relative accuracy <u>1/</u>	RA		1	01		1 / 2	LSB
			2, 3			1	
Differential nonlinearity <u>2/</u> , <u>3/</u>	DNL		1, 2, 3	01		8	Bits
Gain error <u>1/</u>	AE		1	01		±1.5	LSB
			2, 3			±2.5	
Unipolar offset error	OE	0 V to +2.56 V input range FS	1	01		±1	LSB
			2, 3			±2	
Bipolar offset error	BOE	-1.28 V to +1.27 V FS	1	01		±1	LSB
			2, 3			±2	
Input resistance <u>3/</u>	R <sub>IN</sub>	2.55 V input range	1	01	8	12	kΩ
Input bias current <u>3/</u>	I <sub>B</sub>	255 mV input range	1, 2, 3	01		500	nA
Input offset current <u>3/</u>	I <sub>OS</sub>	255 mV input range	1, 2, 3	01		200	nA
Absolute input signal range <u>3/</u> , <u>4/</u> , <u>5/</u>	V <sub>ABS</sub>	Low range	1	01	-0.34	V <sub>CC</sub> - 3.3	V
			2, 3			-0.15	
		High range	1		-3.4	V <sub>CC</sub>	
			2, 3			-1.5	
Power supply rejection ratio	PSRR	2.55 V FS, V <sub>CC</sub> = +4.75 V to +5.5 V	1, 2, 3	01		±0.015	%FS / %

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C V <sub>CC</sub> = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply current	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, (DB0 – DB7, R/ $\overline{W}$ high);  (STATUS, $\overline{CE}$ , $\overline{CS}$ , FORMAT, BPO, $\overline{UPO}$ - low)	1, 2, 3	01		45	mA
Digital input high voltage <u>3/</u>	V <sub>IH</sub>		1, 2, 3	01	2.0		V
Digital input low voltage <u>3/</u>	V <sub>IL</sub>		1	01		0.8	V
			2, 3			0.7	
Digital input high current <u>3/</u>	I <sub>IH</sub>	V <sub>IH</sub> = 5 V	1, 2, 3	01		100	μA
Digital input low current <u>3/</u>	I <sub>IL</sub>	V <sub>IL</sub> = 0 V	1, 2, 3	01		-100	μA
Digital output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.6 mA, V <sub>CC</sub> = 5.5 V	1, 2, 3	01		0.4	V
Digital output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = 0.5 mA, V <sub>CC</sub> = 4.5 V	1, 2, 3	01	2.4		V
Digital output low current	I <sub>OL</sub>	V <sub>OL</sub> = 0.4 V, V <sub>CC</sub> = 5.5 V	1, 2, 3	01	-1.6		mA
Digital output high current	I <sub>OH</sub>	V <sub>OL</sub> = 2.4 V, V <sub>CC</sub> = 4.5 V	1, 2, 3	01	0.5		mA
Common mode rejection ratio <u>3/</u>	CMRR	V <sub>CM</sub> = -0.15 V to V <sub>CC</sub> – 3.8 V	1	01		±1	LSB
			2, 3			±2	
Three-state leakage current <u>3/</u>	I <sub>OZ</sub>	V <sub>applied</sub> = 5 V, V <sub>applied</sub> = 0 V	1, 2, 3	01		±40	μA
Functional tests		See 4.3.1c	7, 8	01			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C V <sub>CC</sub> = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Bus access time <u>3/</u>	t <sub>TD</sub>	R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 90 pF, see figure 6, T <sub>A</sub> = +25°C	9	01		250	ns
Output float delay <u>3/</u>	t <sub>DT</sub>	R <sub>L</sub> = 3 kΩ, see figure 6, T <sub>A</sub> = +25°C	9	01		150	ns
Write / start pulse width <u>3/</u>	t <sub>W</sub>	R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 90 pF, <u>6/</u> see figure 6, T <sub>A</sub> = +25°C	9	01	300		ns
Input data setup time	t <sub>DS</sub>	R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 90 pF, <u>6/</u> see figure 6, T <sub>A</sub> = +25°C	9	01	200		ns
Input data hold time	t <sub>DH</sub>	R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 90 pF, <u>6/</u> see figure 6, T <sub>A</sub> = +25°C	9	01	10		ns
R/ $\overline{W}$ setup before control	t <sub>RWC</sub>	R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 90 pF, <u>6/</u> see figure 6, T <sub>A</sub> = +25°C	9	01	0		ns
Delay to convert start	t <sub>DC</sub>	R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 90 pF, <u>6/</u> see figure 6, T <sub>A</sub> = +25°C	9	01		700	ns
Delay from STATUS OUTPUT to data read	t <sub>SD</sub>	R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 90 pF, <u>6/</u> see figure 6, T <sub>A</sub> = +25°C	9	01		250	ns
Data hold time	t <sub>DH</sub>	R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 90 pF, <u>6/</u> see figure 6, T <sub>A</sub> = +25°C	9	01	25		ns
Conversion time <u>3/</u>	t <sub>C</sub>	V <sub>CC</sub> = +5 V	9	01		10	μs
			10, 11 <u>7/</u>			13	

- 1/ Tested on both 2.55 V full scale and -1.28 V to 1.27 V full scale.
- 2/ Minimum resolution for which there are no missing codes.
- 3/ Parameter is tested at V<sub>CC</sub> = 5 V but is guaranteed from V<sub>CC</sub> = 4.5 V to V<sub>CC</sub> = 5.5 V.
- 4/ The absolute input signal range defines the limits of input signal value from either the (+) or (-) input to ground (as a function of V<sub>CC</sub>) over which the device will produce distinct output codes.
- 5/ The differential input signal range defines the input signal span over which distinct output codes are produced. As this range is exceeded, the device ceases to change output state (see figure 4).
- 6/ Guaranteed, if not tested, to the limits specified in table I herein.
- 7/ 255 mV range. CMRR tested with 0 V and full scale applied to analog inputs output change measured from 0 to V<sub>CM</sub> maximum and 0 to V<sub>CM</sub> minimum and will not exceed specified limits.

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Device type	01
Case outline	R
Terminal number	Terminal symbol
1	DB0 (LSB)
2	DB1
3	DB2
4	DB3
5	DB4
6	DB5
7	DB6
8	DB7 (MSB)
9	STATUS OUTPUT
10	POWER GROUND
11	BPO/ $\overline{UPO}$
12	FORMAT (SEE NOTE)
13	R/ $\overline{W}$
14	$\overline{CS}$
15	$\overline{CE}$
16	V <sub>IN-</sub> (HIGH)
17	V <sub>IN-</sub> (LOW)
18	V <sub>IN+</sub> (HIGH)
19	V <sub>IN+</sub> (LOW)
20	V <sub>CC</sub>

NOTE: Twos complement /  $\overline{\hspace{1cm}}$  straight binary

FIGURE 1. Terminal connections.

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R/ $\overline{W}$	$\overline{CS}$	$\overline{CE}$	Operation	Output
X	X	X	Converting (see note 1)	Three-state
0	0	0	Write/convert (see note 2)	Three-state
1	0	0	Read (see note 2)	Data valid
X	X	1	None (see note 3)	Three-state
X	1	X	None (see note 3)	Three-state

NOTES:

1. Status output high.
2. Status output low.
3. Status output don't care.

FIGURE 2. Control signal truth table.

Mode	Range	Min	Max	Unit
Unipolar	Low	0	255	mV
Unipolar	High	0	2.55	V
Bipolar	Low	-128	127	mV
Bipolar	High	-1.28	1.27	V

FIGURE 3. Differential input signal range truth table.

BPO/ $\overline{UPO}$	FORMAT	Input range / output format
0	0	Unipolar / straight binary
1	0	Bipolar / offset binary
0	1	Unipolar / 2s complement
1	1	Bipolar / 2s complement

FIGURE 4. Input selection / output format truth table.

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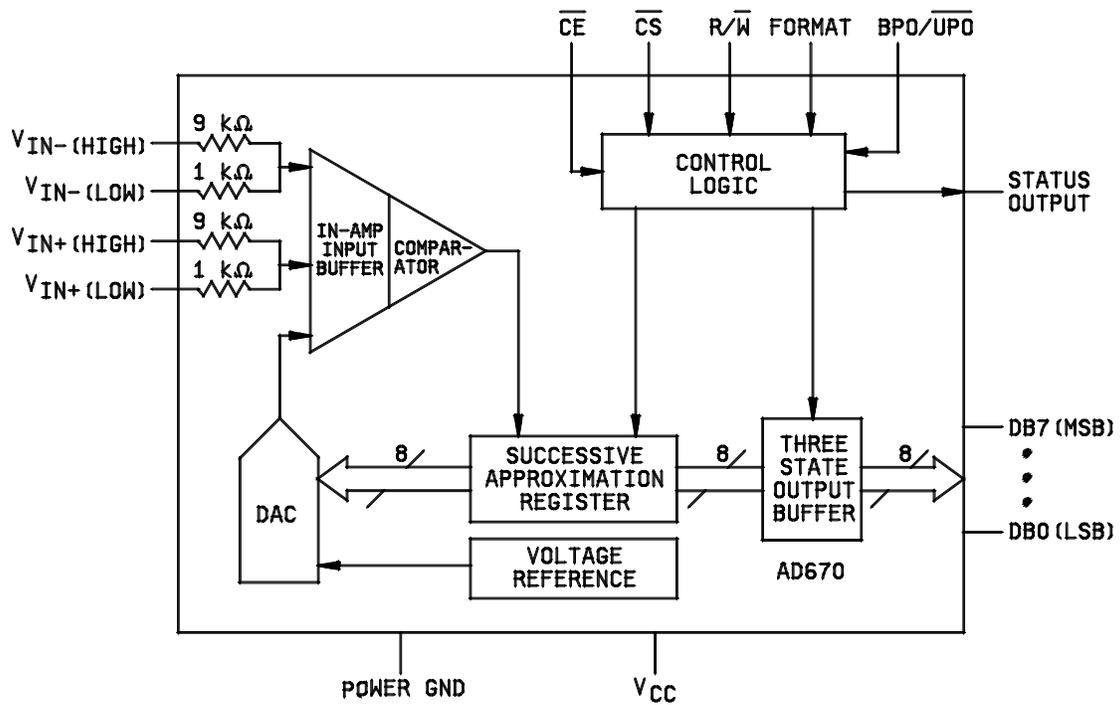


FIGURE 5. Block diagram.

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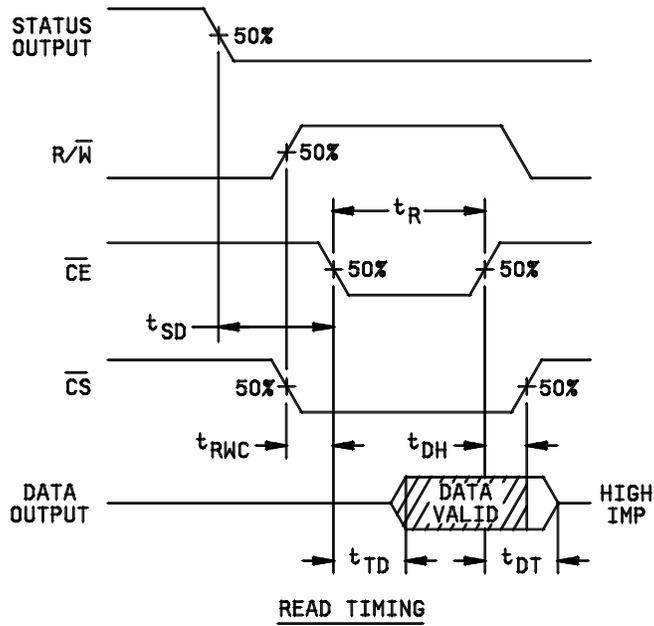
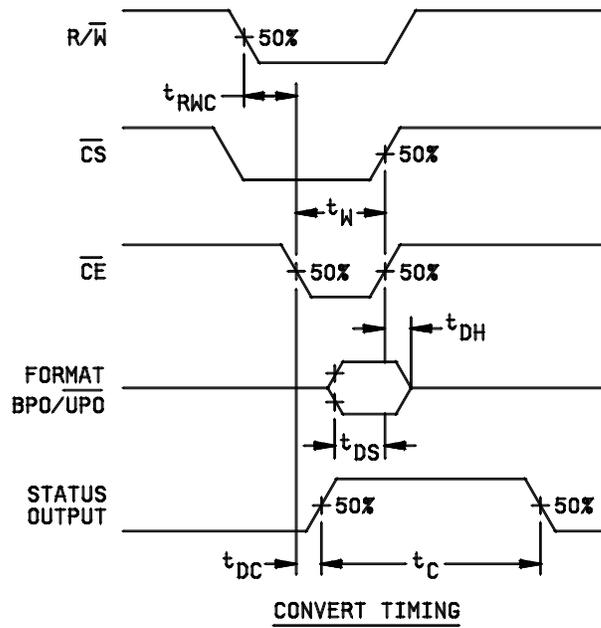


FIGURE 6. Timing waveforms.

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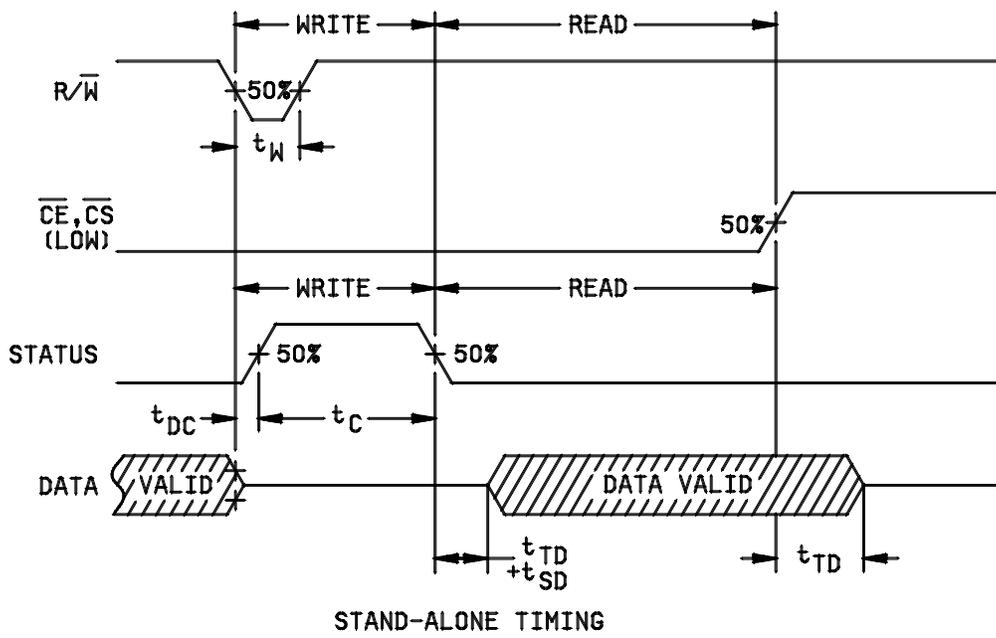


FIGURE 6. Timing waveforms - continued.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1

\* PDA applies to subgroup 1.

\*\* Subgroups 10 and 11 are guaranteed, if not tested, to the limits specified in table I herein.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-12-11

Approved sources of supply for SMD 5962-87635 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8763501RA	24355	AD670SD/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

24355

Vendor name  
and address

Analog Devices  
Route 1 Industrial Park  
P.O. Box 9106  
Norwood, MA 02062  
Point of contact: 804 Woburn Street  
Wilmington, MA 01887-3462

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.