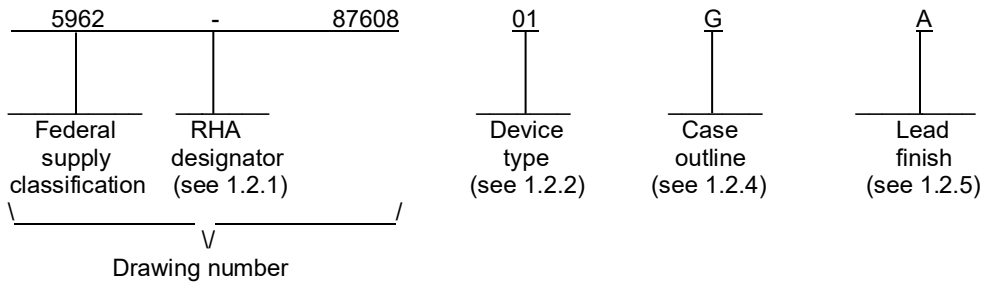


1. SCOPE

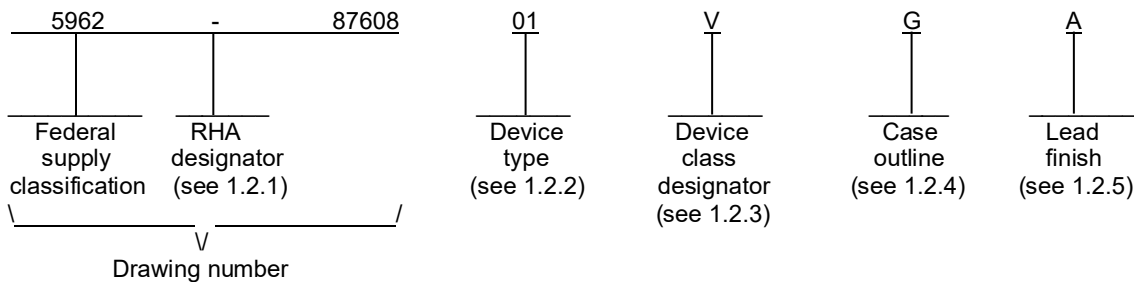
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	LF198	Sample and hold
02	5537	Sample and hold

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

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1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
G	MACY1-X8	8	Can
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
Z	GDFP1-G14	14	Flat pack with gullwing leads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. ^{1/}

Supply voltage ($\pm V_{CC}$)	± 18 V
Power dissipation (PD)	500 mW ^{2/}
Input voltage (V_{IN})	± 18 V ^{3/}
Logic to logic differential voltage	+7 V, -30 V ^{4/}
Output short circuit duration	Indefinite
Hold capacitor short circuit duration	10 seconds
Lead temperature (soldering, 10 seconds)	300°C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case G	48°C/W
Case P	See MIL-STD-1835
Case Z	20°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case G	160°C/W, still air at 0.5 W 84°C/W, 500 LFPM air flow 0.5 W
Case P	120°C/W
Case Z	140°C/W, still air at 0.5 W 95°C/W, 500 LFPM air flow 0.5 W

1.4 Recommended operating conditions.

Supply voltage ($\pm V_{CC}$)	± 15 V
Ambient operating temperature range (T_A)	-55°C to +125°C

- ^{1/} Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- ^{2/} The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} and T_A . The maximum allowable power dissipation at any temperature is $P_{DMAX} - (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in the absolute maximum ratings, whichever is lower.
- ^{3/} The maximum input voltage shall not exceed the power supply voltage.
- ^{4/} Although the differential voltage may not exceed the limits given, the common-mode voltage the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at 2 V below the positive supply and 3 V above the negative supply.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram The logic diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit	
					Min	Max		
Input offset voltage	VOS	+VCC = 3 V, -VCC = -7 V	1	01	-3	3	mV	
			2,3		-5	5		
		±VCC = 15 V	1		-3	3		
			2,3		-5	5		
		+VCC = 3.5 V, -VCC = -26.5 V	1		-3	3		
			2,3		-5	5		
		±VCC = ±18 V	1		-3	3		
			2,3		-5	5		
		+VCC = 3.5 V, -VCC = -32.5 V	1		-3	3		
			2,3		-5	5		
		+VCC = 26.5 V, -VCC = -3.5 V	1		-3	3		
			2,3		-5	5		
		+VCC = 32.5 V, -VCC = -3.5 V	1		-3	3		
			2,3		-5	5		
		+VCC = 7 V, -VCC = -3 V	1		-3	3		
			2,3		-5	5		
		±VCC = ±5 V to ±18 V	1		02	-3		3
			2,3		-5	5		
Positive supply current	+ICC	VCC = ±15 V	1,2	01		5.5	mA	
			3		6.5			
		VCC = ±18 V	1,2	02		6.5		
			3		7.5			
		VCC = ±18 V, mode = sample	1,2	01		5.5		
			3		6.5			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit			
					Min	Max				
Positive supply current	+ICC	VCC = ±18 V, mode = hold	1,2	01		5.5	mA			
			3			6.5				
Negative supply current	-ICC	VCC = ±15 V	1,2	01	-5.5		mA			
			3			-6.5				
		VCC = ±18 V	1,2	02	-6.5					
			3			-7.5				
		VCC = ±18 V, mode = sample	1,2	01	-5.5					
			3			-6.5				
		VCC = ±18 V, mode = hold	1,2	01	-5.5					
			3			-6.5				
		Input bias current	IIB	+VCC = 3 V, -VCC = -7 V	1	01		-25	25	nA
					2,3			-75	75	
±VCC = 15 V	1				-25		25			
	2,3				-75		75			
+VCC = 3.5 V, -VCC = -32.5 V	1				-25		25			
	2,3				-75		75			
+VCC = +32.5 V, -VCC = -3.5 V	1				-25		25			
	2,3				-75		75			
+VCC = 7 V, -VCC = -3 V	1				-25		25			
	2,3				-75		75			
±VCC = ±5 V to ±18 V	1	02	-25	25						
	2,3			-75	75					

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits ^{2/}		Unit
					Min	Max	
Leakage current into ^{3/} hold capacitor	ILEAK	+VCC = 3 V, -VCC = -7 V, TA = +25°C	1	01	-100	100	pA
		+VCC = 3.5 V, -VCC = -32.5 V, TA = +25°C			-100	100	
		+VCC = 32.5 V, -VCC = -3.5 V, TA = +25°C			-100	100	
		+VCC = 7 V, -VCC = -3 V, TA = +25°C			-100	100	
		Hold mode	1	02		.05	nA
	2,3		25				
Hold step ^{4/}	VHS	±VCC = 15 V	1	01	-2	2	mV
			2,3		-5.6	5.6	
		+VCC = 3.5 V, -VCC = -26.5 V	1		-2.5	2.5	
			2,3		-5.6	5.6	
		+VCC = 26.5 V, -VCC = -3.5 V	1		-2.5	2.5	
			2,3	-5.6	5.6		
		VOUT = 0 V, TA = +25°C, CH = 0.01 μF	1	02		2.0	
Input impedance	ZIN	+VCC = 8 V, -VCC = -28 V	1	01	10		GΩ
			2,3		0.8		
		+VCC = 28 V, -VCC = -8 V	1		10		
			2,3		0.8		
Output impedance	ZOUT	±VCC = ±18 V	1	01		2	GΩ
			2,3			4	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit	
					Min	Max		
Output impedance	ZOUT	Hold mode	1	02		2	Ω	
			2,3			4		
Capacitor charging current	ICHRG	+VCC = 8 V, -VCC = -28 V	1	01		-25	-4.5	mA
			2,3			-25	-3	
		+VCC = 28 V, -VCC = -8 V	1			4.5	25	
			2,3			3	25	
Logic pin current	LOGIC	±VCC = ±18 V, mode = sample	1,2,3	01		10		μA
		±VCC = ±18 V, mode = hold	1			1		
			2,3			0.5		
Input offset voltage	VOS	±VCC = ±15 V, 1Drive = +1 mA	1	01		-3.5	3.5	mV
			2,3			-6	6	
Delta input offset voltage	ΔVOS	±VCC = ±15 V, 1Drive = +1 mA to -1 mA	1	01		-1.1	1.1	mV
			2,3			-2	2	
Output short circuit current	+IOS	±VCC = ±18 V, TA = +25°C	1	01		7	20	mA
	-IOS	±VCC = ±18 V, TA = +25°C				-25	7	
Logic reference pin current	ILOG	±VCC = ±18 V, mode = sample	1	01		-1	1	μA
			2,3			-0.5	5	
		±VCC = ±18 V, mode = hold	1,2,3				10	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Logic and logic reference input current	ILOG	VIN = 2.4 V	1	02		10	μA
			2,3			20	
		VIN = 0 V	1		-10		
			2,3		-20		
Power supply rejection ratio	PSRR	+VCC = 10 V, -VCC = -15 V	1	01	80		dB
			2,3		74		
		+VCC = 15 V, -VCC = -10 V	1		80		
			2,3		74		
		+VCC = 15 V, VOUT = 0 V, -VCC = -10 V	1,2,3		02	80	
Feed through rejection ratio	FTRR	+VCC = 3.5 V, -VCC = -32.5 V	1	01	86		dB
			2,3		74		
		+VCC = 32.5 V, -VCC = -3.5 V	1		86		
			2,3		74		
Feed through attenuation ratio	FTAR	CH = 0.01 μF, TA = +25°C	1	02	86		dB
Differential logic level <u>5/</u>	VTH	TA = +25°C	1	All	0.8	2.4	V
Second stage VOS	VOS (2 nd stage)	+VCC = 3.5 V, -VCC = -32.5 V	1	01	-35	35	mV
			2,3		-50	50	
		+VCC = 3.0 V, -VCC = -7 V	1		-35	35	
			2,3		-50	50	
		+VCC = 32.5 V, -VCC = -3.5 V	1		-35	35	
			2,3		-50	50	
		+VCC = 7 V, -VCC = -3 V	1		-35	35	
2,3	-50	50					

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits <u>2/</u>		Unit
					Min	Max	
Acquisition time <u>6/</u>	tAQ	ΔVOUT = 10 V, TA = +25°C, CHOLD = 1000 pF	4	01		6	μs
		ΔVOUT = 10 V, TA = +25°C, CHOLD = 0.01 μF				25	
Gain error	AE	+VCC = 7 V, -VCC = -3 V	1	01		.02	%
			2,3			.06	
		+VCC = 3.5 V, -VCC = -26.5 V	1			.005	
			2,3			.02	
		+VCC = 32.5 V, -VCC = -3.5 V	1			.005	
			2,3			.06	
		+VCC = 26.5 V, -VCC = -3.5 V	1			.005	
			2,3			.02	
		VIN = -10 V to 10 V, RL = 2 kΩ	1	02		.007	
			2,3			.01	
VIN = -11.5 V to 11.5 V, RL = 10 kΩ	1		.007				
	2,3		.01				

- 1/ Unless otherwise specified, VCC = ±15 V, CHOLD = 0.01 μF, and logic reference pin = 0 V. For device type 01, RL = 10 kΩ and VIN = 0 V. For device type 02, RL = 2 kΩ, VIN = -11.5 V to +11.5 V and logic voltage = 2.5 V.
- 2/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
- 3/ Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation of elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
- 4/ Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. One pF, for instance, will create an additional 0.5 mV step with 5 V logic swing and a 0.01 μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
- 5/ Parameter tested go-no-go only.
- 6/ If not tested, shall be guaranteed to the limits specified in table I herein.

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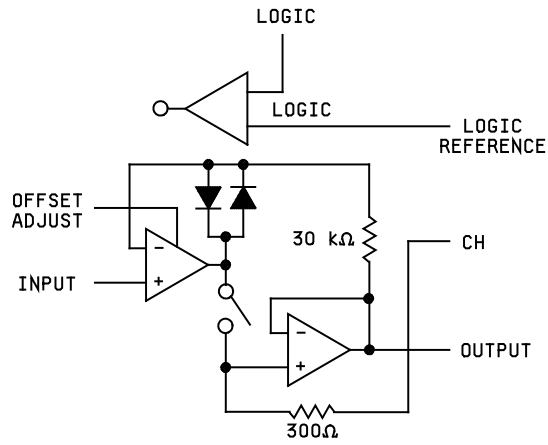
Device types	01		02
Case outlines	G	Z	P
Terminal number	Terminal symbol		
1	+VCC	INPUT	+VCC
2	OFFSET ADJUST	NC	OFFSET ADJUST
3	+INPUT	-VCC	+INPUT
4	-VCC	NC	-VCC
5	OUTPUT	NC	OUTPUT
6	CH	NC	CH
7	LOGIC REFERENCE	OUTPUT	LOGIC REFERENCE
8	LOGIC	CH	LOGIC
9	---	NC	---
10	---	LOGIC REFERENCE	---
11	---	LOGIC	---
12	---	+VCC	---
13	---	NC	---
14	---	OFFSET ADJUST	---

NC = No connection

FIGURE 1. Terminal connections.

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DEVICE TYPE 01



DEVICE TYPE 02

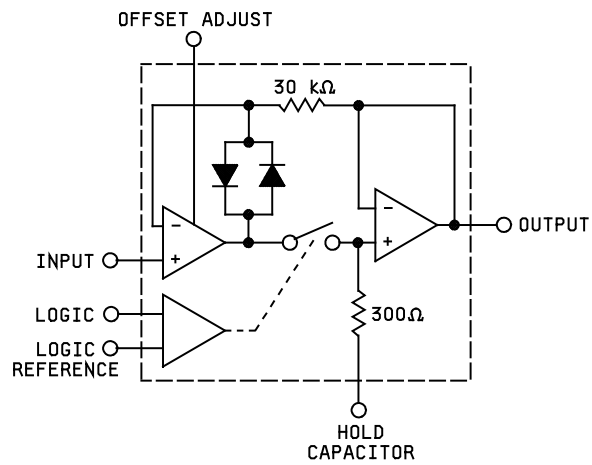


FIGURE 2. Logic diagram.

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3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 60 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q, and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,4 <u>1/</u>	1,2,3,4 <u>1/</u>	1,2,3,4 <u>1/</u>
Group A test requirements (see 4.4)	1,2,3,4	1,2,3,4	1,2,3,4
Group C end-point electrical parameters (see 4.4)	1	1	1,2,3 <u>2/</u>
Group D end-point electrical parameters (see 4.4)	1	1	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous endpoint electrical parameters.

Table IIB. Operating life test delta parameters. TA = 25°C

Parameter	Device type 01	Delta limit	
	Conditions	Min	Max
VIO	+VCC = 15 V, -VCC = -15 V	-0.5 mV	0.5 mV
IIB	+VCC = 15 V, -VCC = -15 V	-2.5 nA	2.5 nA

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5, 6, 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

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6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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DATE: 24-01-26

Approved sources of supply for SMD 5962-87608 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>	Reference military specification PIN
5962-8760801GA	01295	LF198H/883	M38510/12501BGA
5962-8760801QZA	<u>3/</u>	LF198WG/883	---
5962-8760801VZA	01295	LF198WG-QMLV	---
5962-8760802PA	<u>3/</u>	5537/BPA	M38510/12502BPA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE
number

01295

Vendor name
and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.