

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add vendor CAGE 01295. Add case outlines L and 3. Change drawing CAGE code to 67268. Technical changes in 1.4, table I, and figure 3. Editorial changes throughout.	89-08-14	M. A. Frye
B	Make corrections to figure 4. Update boilerplate. Editorial changes throughout. - JAK	00-10-25	Thomas M. Hess
C	Add vendor CAGE F8859. Add device class V criteria. Correct data limits in paragraph 1.3. Add case outline X. Add device type 03. Add table III, delta limits. Update boilerplate to MIL-PRF-38535 requirements. - JAK	02-06-19	Thomas M. Hess
D	Add section 1.5, radiation features. Add waveforms for pulse width, setup and hold times in figure 5. Update the boilerplate to include radiation hardness assured requirements. Editorial changes throughout. - TVN	05-05-25	Thomas M. Hess
E	Add dual-in line package for Rad Hard devices. Update radiation features in section 1.5. Add SEP table IB and paragraph 4.4.4.2. Update the boilerplate paragraphs to current MIL-PRF-38535 requirements. -- MAA	11-09-21	Thomas M. Hess
F	Change case outline X (flat pack) dimension A and add dimensions E2 and E3 to figure 1. Update radiation features in section 1.5 and SEP table IB. - MAA	13-07-24	Thomas M. Hess
G	Add RHA die for device type 03 with die appendix A. - MAA	16-04-12	Muhammad Akbar



REV																				
SHEET																				
REV	G	G	G	G	G	G	G	G	G	G	G									
SHEET	15	16	17	18	19	20	21	22	23	24	25									
REV STATUS OF SHEETS	REV			G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

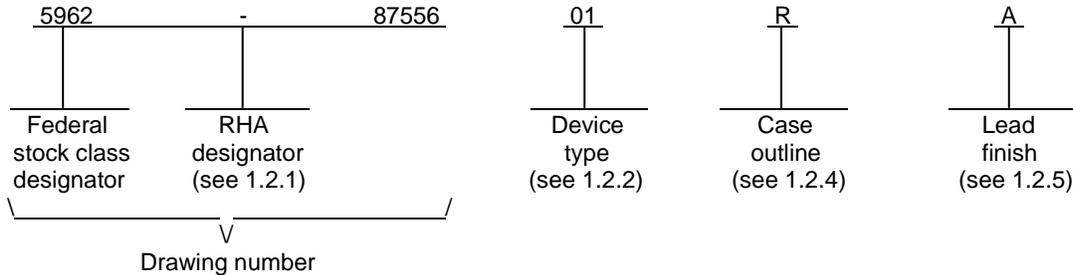
PMIC N/A	PREPARED BY James Nicklaus	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY D. A. DiCenzo																		
	APPROVED BY N. A. Hauck	<p>MICROCIRCUIT, DIGITAL, ADVANCED CMOS, RADIATION HARDENED, OCTAL TRANSPARENT LATCH WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 87-04-27																		
	REVISION LEVEL G	<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-87556</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-87556														
SIZE A	CAGE CODE 67268	5962-87556																	
		SHEET 1 OF 25																	

1. SCOPE

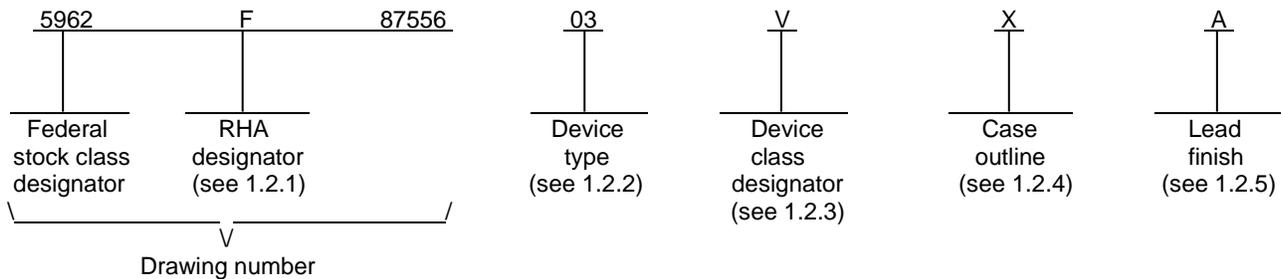
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ACT373	Octal transparent latch with three-state outputs, TTL compatible inputs
02	54ACT11373	Octal transparent latch with three-state outputs, TTL compatible inputs
03	54ACT373	Octal transparent latch with three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

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1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
X	See figure 1	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}).....	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}).....	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage range (V_{OUT}).....	-0.5 V dc to $V_{CC} + 0.5$ V dc
Clamp diode current (I_{IK}, I_{OK}).....	± 20 mA
DC output current (I_{OUT}).....	± 50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}).....	± 100 mA
Maximum power dissipation (P_D).....	500 mW 4/
Storage temperature range (T_{STG}).....	-65°C to +150°C
Lead temperature (soldering, 10 seconds).....	+260°C
Thermal resistance, junction-to-case (θ_{JC}).....	See MIL-STD-1835
Junction temperature (T_J).....	175°C 5/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC}).....	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}).....	0.0 V dc to V_{CC}
Output voltage range (V_{OUT}).....	0.0 V dc to V_{CC}
Input rise or fall time rate ($\Delta t/\Delta V$):	
$V_{CC} = 4.5$ V to 5.5 V.....	0 to 8 ns/V
Case operating temperature range (T_C).....	-55°C to +125°C
Minimum setup time, Dn to LE (t_s):	
$V_{CC} = 4.5$ V, $T_C = +25^\circ\text{C}$	7.0 ns
$V_{CC} = 4.5$ V, $T_C = -55^\circ\text{C}$ and +125°C.....	8.5 ns
Minimum hold time, Dn to LE (t_h):	
$V_{CC} = 4.5$ V, $T_C = +25^\circ\text{C}$:	
Device types 01 and 03.....	0.0 ns
Device type 02.....	3.5 ns
$V_{CC} = 4.5$ V, $T_C = -55^\circ\text{C}$ and +125°C:	
Device types 01 and 03.....	1.0 ns
Device type 02.....	3.5 ns
Minimum pulse width, LE (t_w):	
$V_{CC} = 4.5$ V, $T_C = +25^\circ\text{C}$	7.0 ns
$V_{CC} = 4.5$ V, $T_C = -55^\circ\text{C}$ and +125°C.....	8.5 ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ For $T_C = +100^\circ\text{C}$ to +125°C, derate linearly at 12 mW/°C.

5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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1.5 Radiation features.

Device type 03:

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s) 300 krads (Si)

Single event phenomenon (SEP):

No SEU occurs at effective LET (see 4.4.4.2) ≤ 93 MeV/(mg/cm²)

No SEL occurs at effective LET (see 4.4.4.2) ≤ 93 MeV/(mg/cm²)

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <http://www.astm.org> or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD78 - IC Latch-up Test

JESD20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High Speed CMOS Devices.

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

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TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class	V _{CC}	Group A subgroups	Limits <u>4/</u>		Unit				
						Min	Max					
Positive input clamp voltage 3022	V _{IC+}	For input under test, I _{IN} = 1.0 mA	All V	0.0 V	1	0.4	1.5	V				
Negative input clamp voltage 3022	V _{IC-}	For input under test, I _{IN} = -1.0 mA	All V	Open	1	-0.4	-1.5	V				
High level output voltage 3006	V _{OH} <u>5/</u>	V _{IN} = V _{IH} minimum = 2.0 V or V _{IL} maximum = 0.8 V, I _{OH} = -50 μA	All	4.5 V	1, 2, 3	4.4		V				
			All	5.5 V		5.4						
		V _{IN} = V _{IH} minimum = 2.0 V or V _{IL} maximum = 0.8 V, I _{OH} = -24 mA	All	4.5 V	1, 2, 3	3.70						
			All	5.5 V		1, 2, 3	4.70					
Low level output voltage 3007	V _{OL} <u>5/</u>	V _{IN} = V _{IH} minimum = 2.0 V or V _{IL} maximum = 0.8 V, I _{OL} = 50 μA	All	4.5 V	1, 2, 3		0.1	V				
			All	5.5 V			0.1					
		V _{IN} = V _{IH} minimum = 2.0 V or V _{IL} maximum = 0.8 V, I _{OL} = 24 mA	All	4.5 V	1, 2, 3		0.50					
			All	5.5 V		1, 2, 3			0.50			
High level input voltage	V _{IH} <u>6/</u>		All	4.5 V	1, 2, 3	2.0		V				
			All	5.5 V			2.0					
			Low level input voltage	V _{IL} <u>6/</u>		All	4.5 V		1, 2, 3		0.8	V
						All	5.5 V				0.8	
Input leakage current high 3010	I _{IH}	For input under test, V _{IN} = V _{CC} For all other inputs, V _{IN} = V _{CC} or GND	All All	5.5 V	1, 2, 3		1.0	μA				
Input leakage current low 3009	I _{IL}	For input under test, V _{IN} = GND For all other inputs, V _{IN} = V _{CC} or GND	All All	5.5 V	1, 2, 3		-1.0	μA				
Quiescent supply current, output high 3005	I _{CCH}	V _{IN} = V _{CC} or GND	01, 02 All	5.5 V	1, 2, 3		160.0	μA				
			03 All			1	2.0					
						2, 3			80.0			
			M, D, P, L, R, F <u>7/</u>	03 Q, V	5.5 V	1			50.0			

See footnotes at end of table

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class	V _{CC}	Group A subgroups	Limits <u>4/</u>		Unit	
						Min	Max		
Quiescent supply current, output low 3005	I _{CCL}	V _{IN} = V _{CC} or GND	01, 02 All	5.5 V	1, 2, 3		160.0	μA	
			03 All		1		2.0		
					2, 3		80.0		
M, D, P, L, R, F <u>7/</u>	03 Q, V	5.5 V	1		50.0				
Quiescent supply current, output three-state 3005	I _{CCZ}	V _{IN} = V _{CC} or GND	01, 02 All	5.5 V	1, 2, 3		160.0	μA	
			03 All		1		2.0		
					2, 3		80.0		
M, D, P, L, R, F <u>7/</u>	03 Q, V	5.5 V	1		50.0				
Quiescent supply current delta, TTL input levels 3005	ΔI _{CC} <u>8/</u>	For input under test, V _{IN} = V _{CC} - 2.1 V For all other inputs, V _{IN} = V _{CC} or GND	All All	5.5 V	1, 2, 3		1.6	mA	
Three-state output leakage current high 3021	I _{OZH}	V _{IN} = V _{CC} or GND V _{OUT} = V _{CC}	01, 02 All	5.5 V	1, 2, 3		10.0	μA	
			03 All		1		0.5		
					2, 3		10.0		
M, D, P, L, R, F	03 Q, V	5.5 V	1		5.0				
Three-state output leakage current low 3020	I _{OZL}	V _{IN} = V _{CC} or GND V _{OUT} = GND	01, 02 All	5.5 V	1, 2, 3		-10.0	μA	
			03 All		1		-0.5		
					2, 3		-10.0		
M, D, P, L, R, F	03 Q, V	5.5 V	1		-5.0				
Input capacitance 3012	C _{IN}	T _C = 25°C See 4.4.1c	01, 03 All	GND	4		8.0	pF	
			02 All				10.0		
Power dissipation capacitance	C _{PD} <u>9/</u>	T _C = 25°C See 4.4.1c	01, 03 All	5.0 V	4		75.0	pF	
			02 All				Outputs enabled		82.0
							Outputs disabled		68.0
Functional tests 3014	<u>10/</u>	V _{IN} = V _{IH} or V _{IL} Verify output V _{OUT} See 4.4.1b	All All	4.5 V	7, 8	L	H		
				5.5 V	7, 8	L	H		

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class	V _{CC}	Group A subgroups	Limits <u>4/</u>		Unit
						Min	Max	
Propagation delay time, Dn to Qn 3003	t _{PHL1} , t _{PLH1} <u>11/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 5	01, 03 All	4.5 V	9	1.0	10.5	ns
					10, 11	1.0	12.5	
			02 All		9	1.0	10.5	
					10, 11	1.0	12.7	
Propagation delay time, LE to Qn 3003	t _{PHL2} <u>11/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 5	01, 03 All	4.5 V	9	1.0	10.0	ns
					10, 11	1.0	11.5	
			02 All		9	1.0	10.9	
					10, 11	1.0	13.0	
	t _{PLH2} <u>11/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 5	01, 03 All	4.5 V	9	1.0	10.5	ns
					10, 11	1.0	12.5	
			02 All		9	1.0	11.3	
					10, 11	1.0	14.1	
Propagation delay time, output enable, \overline{OE} to Qn 3003	t _{PZH} <u>11/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 5	01, 03 All	4.5 V	9	1.0	9.5	ns
					10, 11	1.0	11.5	
			02 All		9	1.0	10.7	
					10, 11	1.0	13.6	
	t _{PZL} <u>11/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 5	01 All	4.5 V	9	1.0	9.0	ns
					10, 11	1.0	11.0	
			02 All		9	1.0	10.9	
					10, 11	1.0	12.9	
			03 All		9	1.0	9.5	
					10, 11	1.0	11.0	
Propagation delay time, output disable, \overline{OE} to Qn 3003	t _{PHZ} <u>11/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 5	01, 03 All	4.5 V	9	1.0	11.0	ns
					10, 11	1.0	14.0	
			02 All		9	1.0	12.1	
					10, 11	1.0	14.0	
	t _{PLZ} <u>11/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 5	01 All	4.5 V	9	1.0	9.0	ns
					10, 11	1.0	11.0	
			02 All		9	1.0	9.5	
					10, 11	1.0	11.0	
			03 All		9	1.0	11.0	
					10, 11	1.0	12.5	

See footnotes on next sheet.

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TABLE IA. Electrical performance characteristics - Continued.

- 1/ For tests not listed in the referenced MIL-STD-883, [e.g. V_{IH} , V_{IL}], utilize the general test procedure under the conditions listed herein.
- 2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.
- 3/ RHA parts for device type 03 meet all levels M, D, P, L, R, and F of irradiation. However, these parts are only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = 25^\circ\text{C}$.
- 4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table IA, as applicable, at $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$.
- 5/ The V_{OH} and V_{OL} tests shall be tested at $V_{CC} = 4.5\text{ V}$. The V_{OH} and V_{OL} tests are guaranteed, if not tested, for $V_{CC} = 5.5\text{ V}$. Limits shown apply to operation at $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$. Transmission driving tests are performed at $V_{CC} = 5.5\text{ V}$ with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN} = V_{IH}$ minimum and V_{IL} maximum.
- 6/ The V_{IH} and V_{IL} tests are not required if applied as forcing functions for V_{OH} and V_{OL} tests.
- 7/ The maximum limit for this parameter at 100 krad/s (Si) is 2 μA .
- 8/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1\text{ V}$ (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times ΔI_{CC} maximum limit; and the preferred method and limits are guaranteed.
- 9/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and dynamic current consumption (I_S). Where:

$$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$$

$$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC} + (n \times d \times \Delta I_{CC})$$
 For both P_D and I_S , n is number of device inputs at TTL levels; f is the frequency of the input signal; d is duty cycle of the input signal; and C_L is the external output load capacitance.
- 10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances in accordance with MIL-STD-883 for the input voltage levels may be incorporated. For outputs, $H \geq 2.5\text{ V}$, $L < 2.5\text{ V}$.
- 11/ AC limits at $V_{CC} = 5.5\text{ V}$ are equal to the limits at $V_{CC} = 4.5\text{ V}$ and guaranteed by testing at $V_{CC} = 4.5\text{ V}$. Minimum AC limits for $V_{CC} = 5.5\text{ V}$ are 1.0 ns and guaranteed by guardbanding the $V_{CC} = 4.5\text{ V}$ minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

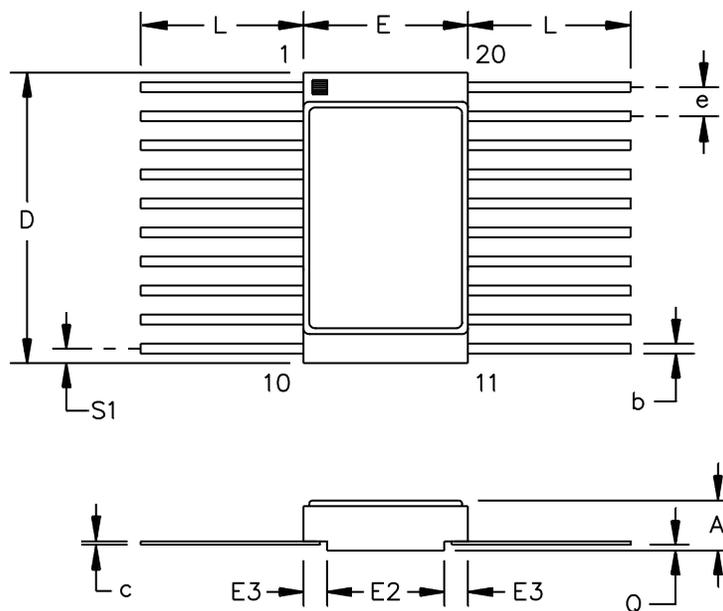
TABLE IB. SEP test limits. 1/ 2/

Device type	Single event upset (SEU) test; operating voltage at bias $V_{CC} = 4.5\text{ V}$ No SEU at effective LET = 3/	Single event latch-up (SEL) test; maximum operating voltage at bias $V_{CC} = 5.5\text{ V}$ No SEL at effective LET = 3/ 4/
03	LET $\leq 93\text{ MeV}/(\text{mg}/\text{cm}^2)$	LET $\leq 93\text{ MeV}/(\text{mg}/\text{cm}^2)$

- 1/ For SEP test conditions, see 4.4.4.2 herein.
- 2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
- 3/ Tested for latch-up at worst case operating temperature, $T_A = +125^\circ\text{C} \pm 10^\circ\text{C}$ and for upset at worst case operating temperature, $T_A = +25^\circ\text{C} \pm 10^\circ\text{C}$
- 4/ For device type 03 tested SEL and SEU effective LET $\leq 93\text{ MeV}/(\text{mg}/\text{cm}^2)$ and no latch-up and SEU occurs.

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Case X



Symbol	Dimensions					
	Inches			Millimeters		
	Typical	Min	Max	Typical	Min	Max
A		0.075	0.087		1.91	2.21
b		0.015	0.019		0.38	0.48
c		0.003	0.006		0.076	0.152
D		0.505	0.515		12.83	13.08
E		0.275	0.285		6.99	7.24
E2		0.199	0.211		5.05	5.36
E3	0.037			0.95		
e		0.045	0.055		1.14	1.40
L		0.250	0.370		6.35	9.39
Q		0.010	---		0.25	---
S1	0.021			0.55		

Note: Deviation from MIL-STD-1835 REF. F-9, CONFIG. B the dimension c is 0.003 inches minimum instead of 0.004 inches minimum and dimension Q is 0.010 inches minimum instead of 0.026 inches minimum.

FIGURE 1. Case outline X.

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Device types	01, 03	02	
Case outlines	R, S, X, 2	L	3
Terminal number	Terminal symbol	Terminal symbol	Terminal symbol
1	\overline{OE}	Q0	NC
2	Q0	Q1	V _{CC}
3	D0	Q2	D3
4	D1	Q3	D2
5	Q1	GND	D1
6	Q2	GND	D0
7	D2	GND	\overline{OE}
8	D3	GND	NC
9	Q3	Q4	Q0
10	GND	Q5	Q1
11	LE	Q6	Q2
12	Q4	Q7	Q3
13	D4	LE	GND
14	D5	D7	GND
15	Q5	D6	NC
16	Q6	D5	GND
17	D6	D4	GND
18	D7	V _{CC}	Q4
19	Q7	V _{CC}	Q5
20	V _{CC}	D3	Q6
21	---	D2	Q7
22	---	D1	NC
23	---	D0	LE
24	---	\overline{OE}	D7
25	---	---	D6
26	---	---	D5
27	---	---	D4
28	---	---	V _{CC}

NC = No internal connection

FIGURE 2. Terminal connections.

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Inputs			Outputs
\overline{OE}	LE	Dn	Qn
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	Q0

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance
Q0 = Output prior to last high-to-low transition of LE

FIGURE 3. Truth table.

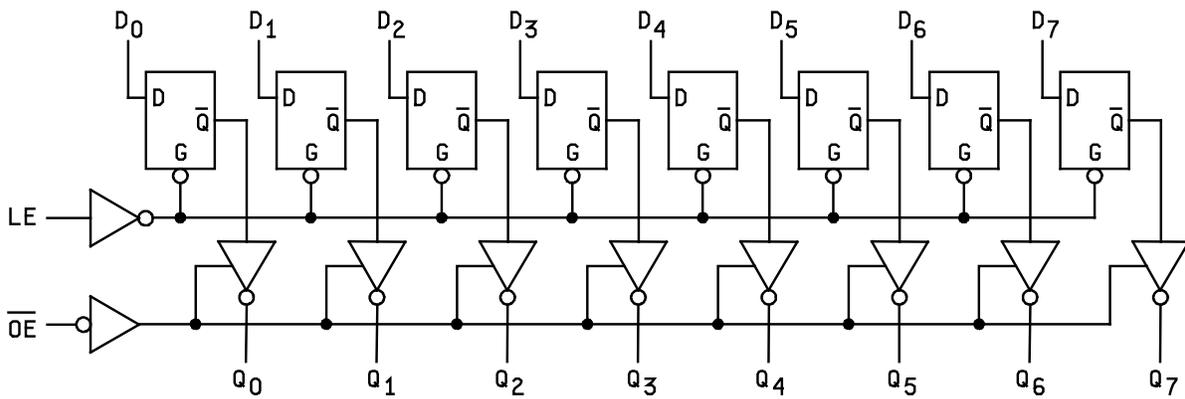


FIGURE 4. Logic diagram.

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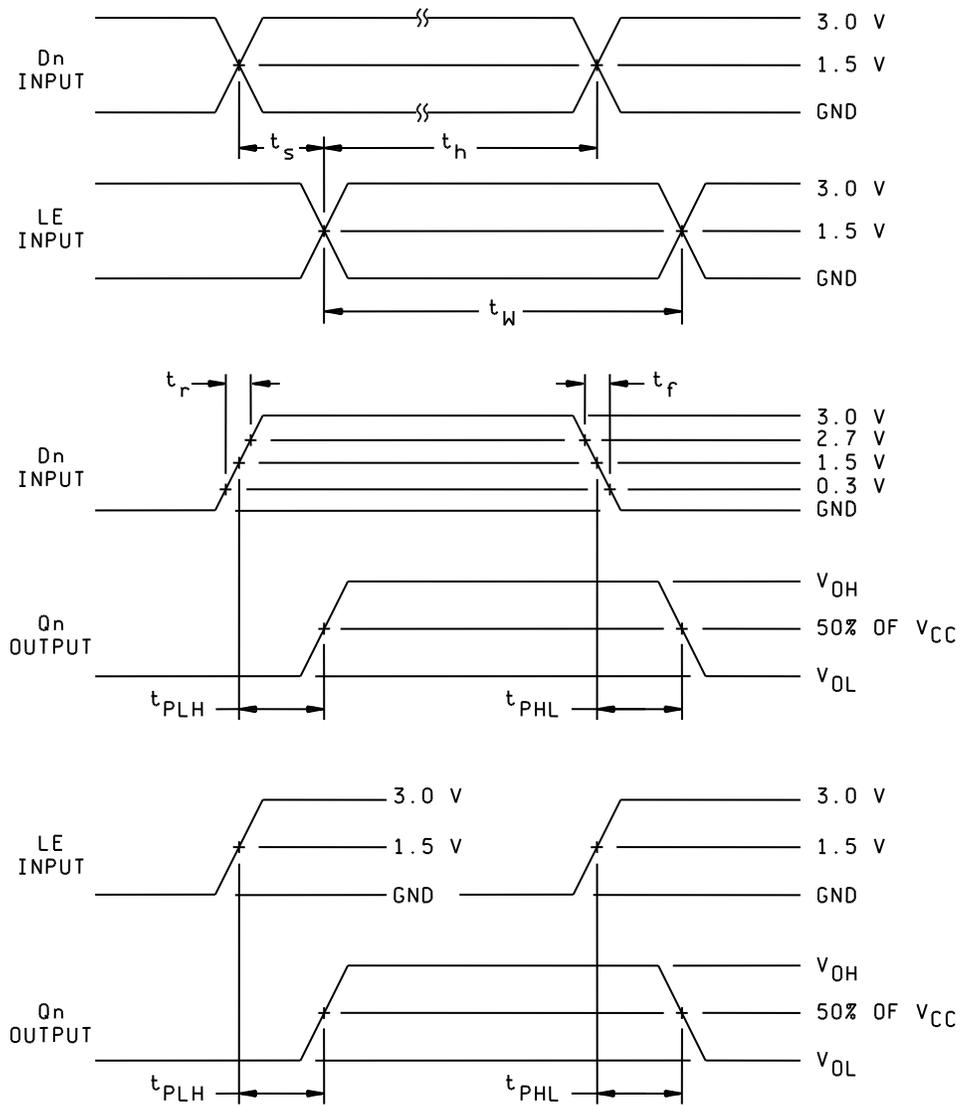


FIGURE 5. Switching waveforms and test circuit.

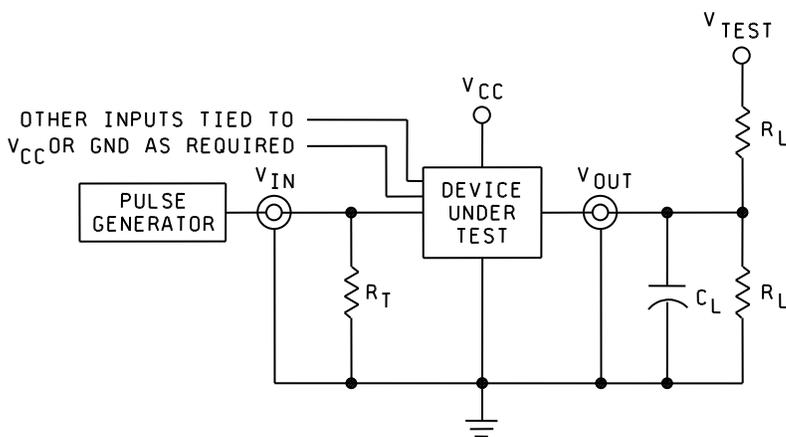
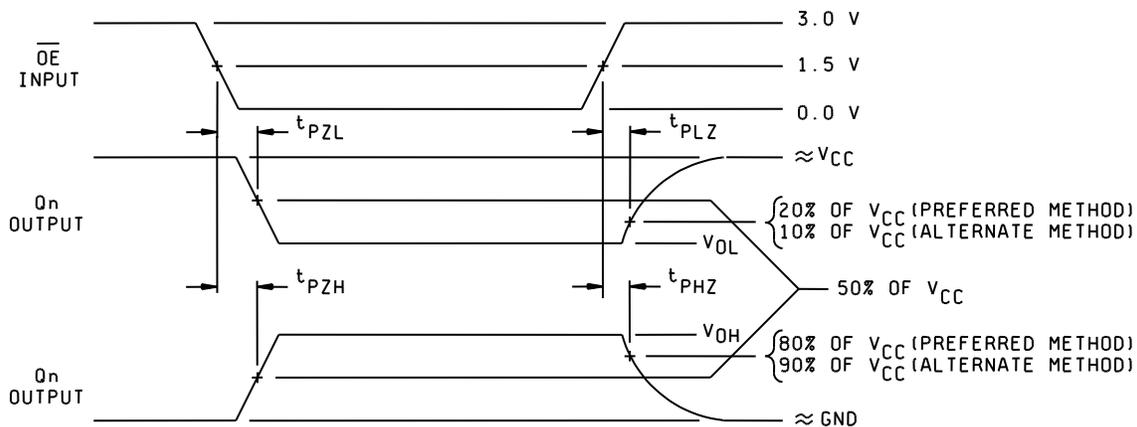
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NOTES:

1. Preferred method:
 When measuring t_{PHZ} and t_{PZH} : $V_{TEST} = GND$.
 When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 2 \times V_{CC}$.
 When measuring t_{PLH} and t_{PHL} : $V_{TEST} = open$.
 Alternate method:
 When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 2 \times V_{CC}$.
 When measuring t_{PHZ} , t_{PZH} , t_{PLH} , and t_{PHL} : $V_{TEST} = open$.
2. $C_L = 50 \text{ pF}$ minimum or equivalent (includes test jig and probe capacitance).
3. $R_T = 50\Omega$ or equivalent, $R_L = 500\Omega$ or equivalent.
4. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to 3.0 V ; $PRR \leq 10 \text{ MHz}$; $t_r \leq 3.0 \text{ ns}$; $t_f \leq 3.0 \text{ ns}$; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V , respectively; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
6. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard JESD20 and table IA herein. For C_{IN} and C_{PD} , test all applicable pins on five devices with zero failures.

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. RHA tests for device classes M, Q, and V for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table IA for subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

Device type 03:

- a. Inputs tested high, $V_{CC} = 5.5 \text{ V dc} \pm 5\%$, $V_{IN} = 5.0 \text{ V dc} + 10\%$, $R_{IN} = 1 \text{ k}\Omega \pm 20\%$, and all outputs are open.
- b. Inputs tested low, $V_{CC} = 5.5 \text{ V dc} \pm 5\%$, $V_{IN} = 0.0 \text{ V}$, $R_{IN} = 1 \text{ k}\Omega \pm 20\%$, and all outputs are open.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing test shall be performed on classes M, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

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4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The upset test temperature shall be +25°C. The latch-up test temperature shall be at the maximum rated operating temperature $\pm 10^\circ\text{C}$.
- f. Bias conditions shall be $V_{CC} = 5.5$ V dc for the latch-up measurements.
- g. For SEP test limits, see table IB herein.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/</u> <u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	<u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1, 7, and deltas.

3/ Delta limits, as specified in table III, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE III. Burn-in and operating life test, delta parameters (+25°C).

Parameter <u>1/</u>	Symbol	Device type	Delta limits
Quiescent supply current	$I_{CCH}, I_{CCL}, I_{CCZ}$	01	± 100 nA <u>2/</u>
		03	± 300 nA
Supply current delta	ΔI_{CC}	03	± 0.4 mA
Input current low level	I_{IL}	03	± 20 nA
Input current high level	I_{IH}	03	± 20 nA
Output voltage low level ($V_{CC} = 5.5$ V, $I_{OL} = 24$ mA)	V_{OL}	03	± 0.04 V
Output voltage high level ($V_{CC} = 5.5$ V, $I_{OH} = -24$ mA)	V_{OH}	03	± 0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determined delta limits.

2/ This limit is guaranteed if not tested.

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4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

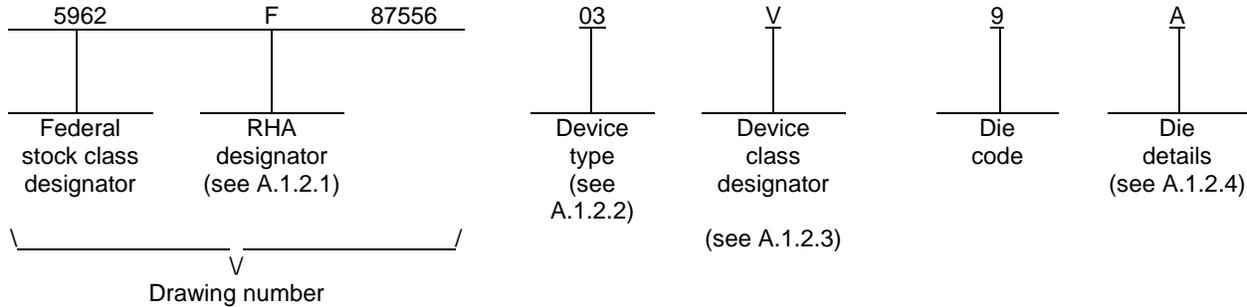
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APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-87556

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
03	54ACT373	Octal transparent latch with three-state outputs, TTL compatible inputs

A.1.2.3 Device class designator.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

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APPENDIX A

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A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

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A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

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A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

- a) Wafer lot acceptance for Class V product using the criteria defined in MIL-STD-883, method 5007.
- b) 100% wafer probe (see paragraph A.3.4 herein).
- c) 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883 method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

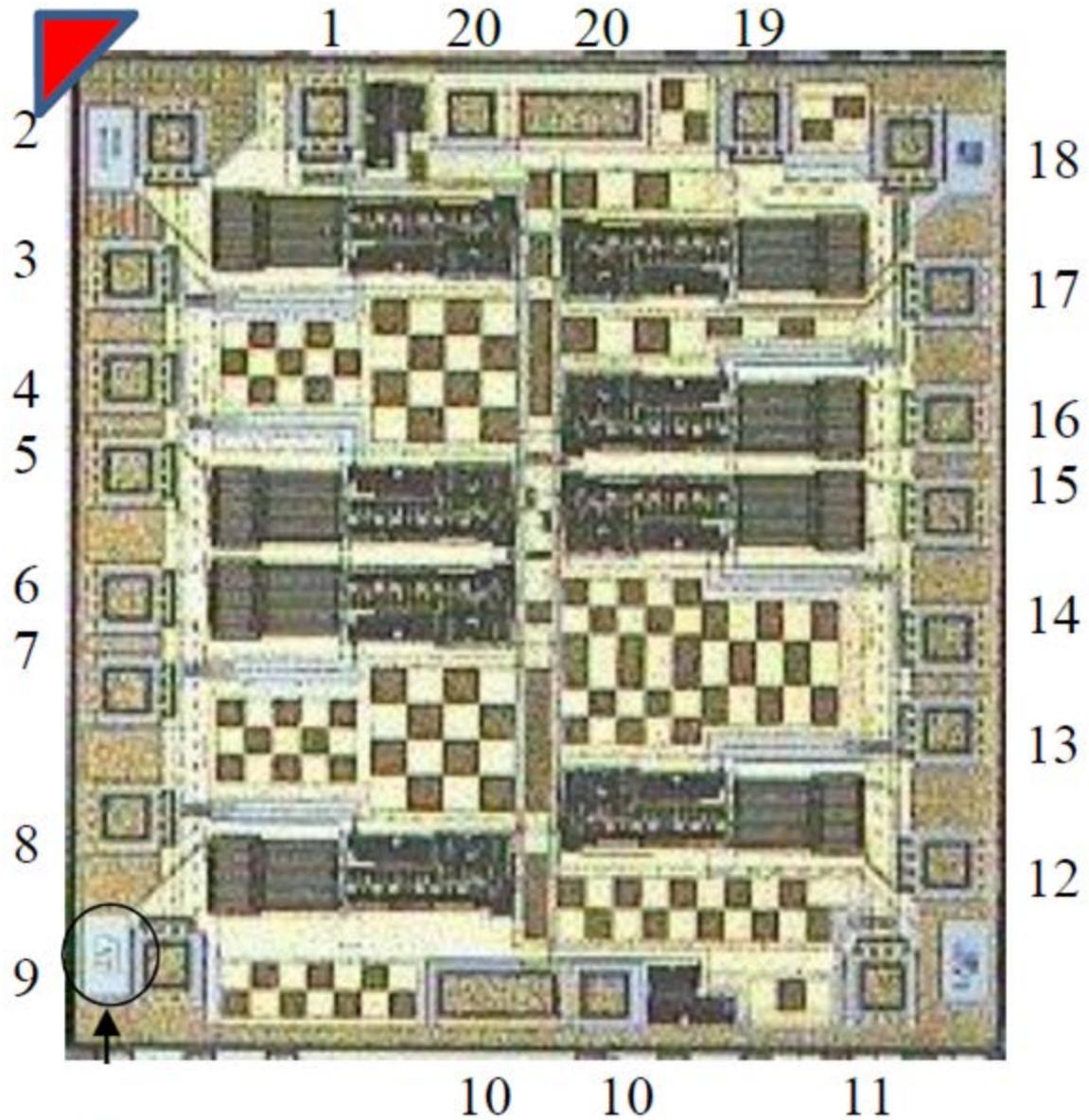
A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0547.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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Note: Pad numbers reflect terminal numbers when placed in Case Outline R and X (see paragraph 1.2.4 and figure 1)

FIGURE A-1. Die bonding pad locations and electrical functions.

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Bonding Pads Coordinates		
Pad number	X(μm)	Y(μm)
1	-525.0	1081.5
2	-898.1	1015.0
3	-999.9	683.1
4	-999.8	426.7
5	-999.8	200.3
6	-999.8	-113.2
7	-999.8	-339.6
8	-999.8	-653.1
9	-998.1	-1015.5
10	-95.0	-1081.5
10	169.2	-1081.5
11	843.0	-1057.4
12	999.8	-756.5
13	999.8	-426.7
14	999.8	-200.3
15	999.8	-113.2
16	999.8	339.6
17	999.8	653.1
18	898.1	1015.0
19	525.0	1081.5
20	95	1081.5
20	-169.2	1081.5

Die physical dimensions.

Die size: 2408 μm x 2250 μm
 Die thickness: 285 ± 25 μm
 Die pad size 1: 100X100 μm
 Die pad size 2: 100X280 μm

Interface materials.

Top to bottom metallization: Si (1%), Al (98.5%), Cu(0.5%) and Thickness: 0.85 μm
 Backside metallization: None

Glassivation.

Type: Nitride (7000Å) + Pvpox (5000Å)
 Substrate: Silicon

Assembly related information.

Substrate potential: Floating or tied to ground
 Special assembly instructions: Bond one of the pad 20 first.

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

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DATE: 16-04-12

Approved sources of supply for SMD 5962-87556 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8755601RA	0C7V7	54ACT373DMQB
	01295	SNJ54ACT373J
5962-8755601SA	0C7V7	54ACT373FMQB
	01295	SNJ54ACT373W
5962-87556012A	0C7V7	54ACT373LMQB
	01295	SNJ54ACT373FK
5962-8755601VRA	01295	SNV54ACT373J
5962-8755601VSA	01295	SNV54ACT373W
5962-8755602LA	<u>3/</u>	SNJ54ACT11373JT
5962-87556023A	<u>3/</u>	SNJ54ACT11373FK
5962-8755603XA	<u>3/</u>	54ACT373
5962-8755603XC	<u>3/</u>	54ACT373
5962-8755603VXA	<u>3/</u>	54ACT373
5962-8755603VXC	<u>3/</u>	54ACT373
5962F8755603XA	F8859	RHFACT373K02Q
5962F8755603XC	F8859	RHFACT373K01Q
5962F8755603VXA	F8859	RHFACT373K02V
5962F8755603VXC	F8859	RHFACT373K01V
5962F8755603VRC	F8859	RHFACT373D03V
5962F8755603RC	F8859	RHFACT373D03Q
5962F8755603VRA	F8859	RHFACT373D04V
5962F8755603RA	F8859	RHFACT373D04Q
5962F8755603V9A	F8859	ACT373DIE2V

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ No longer available from an approved source of supply.

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<u>Vendor CAGE number</u>	<u>Vendor name and address</u>
0C7V7	e2v, Inc. 765 Sycamore Drive Milpitas, CA 95035
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE

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