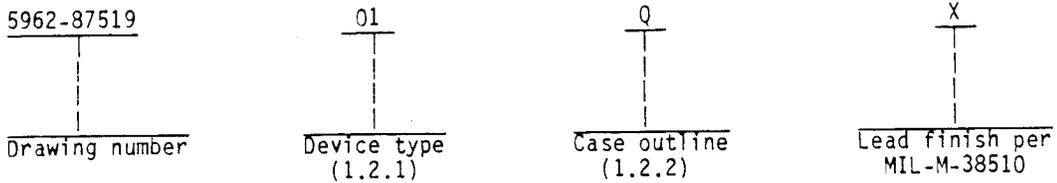


NOTICE OF REVISION (NOR) (See MIL-STD-480 for instructions) This revision described below has been authorized for the document listed.		DATE (YYMMDD) 91/09/20	Form Approved OMI: No. 0704-0188
Public reporting burden for this collection is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Washington, DC 20503.			
1. ORIGINATOR NAME AND ADDRESS Defense Electronics Supply Center Dayton, Ohio 45444-5277	2. CAGE CODE 67268	3. NOR NO. 5962-R011-91	
	4. CAGE CODE 67268	5. DOCUMENT NO. 5962-87519	
6. TITLE OF DOCUMENT MICROCIRCUITS, DIGITAL, NMOS, GENERAL, PURPOSE INTERFACE BUS CONTROLLER, MONOLITHIC SILICON	7. REVISION LETTER (Current) Initial (New) A		
	8. ECP NO.		
9. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES			
10. DESCRIPTION OF REVISION <u>1/</u> Sheet 1: Revisions ltr column; add "A" Revisions description column; add "Changes in accordance with NOR 5962-R011-91". Revisions date column; add "91-09-20". Sheet 4: Change Table 1, Input Current (I_I) FROM: $V_{CC} = 4.75$ V TO: $V_{CC} = 5.25$ V Sheet 5: Change Table 1, Delay of BI interrupt from DAV true (t_{d6}) FROM: BI interrupt unmasked, ATN = false, device in LASC TO: BI interrupt unmasked, ATN = false, device in LACS. Sheet 8: Change Table 1, Clock high pulse duration (t_{μ} (Theta H)) FROM: 1955 ns Min TO: 1955 ns Max Sheet 30: Change Pin Description No. 39 (TR) FROM: ...the get command is given by the MPU TO: ...the fget command is given by the MPU. Notes: <u>1/</u> These changes were previously approved 2 JUN 88 for incorporation into the next action of drawing 5962-87519.			
11. THIS SECTION FOR GOVERNMENT USE ONLY			
a. CHECK ONE <input checked="" type="checkbox"/> EXISTING DOCUMENT SUPPLEMENTED BY THIS NOR MAY BE USED IN MANUFACTURE. <input type="checkbox"/> REVISED DOCUMENT MUST BE RECEIVED BEFORE MANUFACTURER MAY INCORPORATE THIS CHANGE. <input type="checkbox"/> CUSTODIAN OF MASTER DOCUMENT SHALL MAKE ABOVE REVISION AND FURNISH REVISED DOCUMENT TO:			
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ECC	SIGNATURE AND TITLE <i>Monci Felkin</i> CHIEF MICROELECTRONICS BRANCH		DATE (YYMMDD) 91/09/20
12. ACTIVITY ACCOMPLISHING REVISION DESC-ECC	REVISION COMPLETED (Signature) <i>Thomas M. Idon</i>		DATE (YYMMDD) 91/09/20

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	9914A	General purpose interface bus (GPIB) controller

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

<u>Outline letter</u>	<u>Case outline</u>
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) - - - - -	-0.3 V dc to 20 V dc
Input voltage range - - - - -	-0.3 V dc to 20 V dc
Output voltage range - - - - -	-0.3 V dc to 20 V dc
Continuous power dissipation - - - - -	1.0 W
Storage temperature range - - - - -	-55°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}) - - - - -	See MIL-M-38510, appendix C
Lead temperature (soldering, 10 seconds) - - - - -	+300°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) - - - - -	4.75 V dc to 5.25 V dc
Supply voltage (V_{SS}) - - - - -	0 V dc
High level input voltage (V_{IH}) - - - - -	2.0 V dc minimum
Low level input voltage (V_{IL}) - - - - -	0.8 V dc maximum
High level output current (I_{OH}):	
All outputs except REN, IFC, INT - - - - -	-400 μ A maximum
Outputs REN and IFC only - - - - -	-100 μ A maximum
Low level output current (I_{OL}) - - - - -	2.0 mA maximum
Case operating temperature range (T_C) - - - - -	-55°C to +110°C

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A	5962-87519
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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 Register addresses. The register addresses shall be as shown on figure 3.

3.2.5 Internal registers. The internal registers shall be as shown on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions -55°C < T _C < +110°C 4.75 V ≤ V _{CC} ≤ 5.25 V	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage (all outputs except REN, IFC, and INT)	V _{OH}	V _{CC} = 4.75 V, V _{IL} = 0.8 V, V _{IH} = 2.0 V, I _{OH} = -400 μA	1,2,3	01	2.4		V
High level output voltage (REN and IFC only)	V _{OH}	V _{CC} = 4.75 V, V _{IL} = 0.8 V, V _{IH} = 2.0 V, I _{OH} = -100 μA	1,2,3	01	2.2		V
Low level output voltage	V _{OL}	V _{CC} = 4.75 V, V _{IL} = 0.8 V, V _{IH} = 2.0 V, I _{OL} = 2.0 mA	1,2,3	01		0.4	V
Input current	I _I	V _{CC} = 4.75 V, V _I = V _{SS} to V _{CC}	1,2,3	01	-10	10	μA
Off-state output current	I _{OZL}	V _{CC} = 5.25 V, V _O = 0.4 V	1,2,3	01		-20	μA
Off-state output current	I _{OZH}	V _{CC} = 5.25 V, V _O = 2.4 V	1,2,3	01		20	μA
Supply current	I _{CC}	V _{CC} = 5.25 V	1,2,3	01		200	mA
Input capacitance	C _{in}	See 4.3.1c	4	01		15	pF
Functional tests		See figure 5 and 4.3.1d	7,8	01			
Access time from \overline{CE}	t _a (CE)	See figure 5	9,10,11	01		150	ns
Access time from DBIN low	t _a (DBIN)		9,10,11	01		150	ns
Address setup time to \overline{CE}	t _{su} (AD)		9,10,11	01	0		ns
DBIN low to data high impedance	t _d (DBINL-DZ)		9,10,11	01		100	ns
\overline{CE} high to data high impedance	t _d (CEH-DZ)		9,10,11	01		100	ns

See footnotes at end of table.

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		REVISION LEVEL	SHEET 4

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions -55°C < T _C < +110°C 4.75 V < V _{CC} < 5.25 V	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Access time from $\overline{\text{ACCGR}}$ low	t _a (GR)	See figure 5	9,10,11	01		150	ns
$\overline{\text{ACCGR}}$ high to data high impedance	t _d (AGRH-DZ)					100	ns
Delay of $\overline{\text{ACCGR}}$ high from $\overline{\text{ACCGR}}$ low	t _d (GRL-RQH)					100	ns

Test	Symbol	Conditions -55°C < T _C < +110°C 4.75 V < V _{CC} < 5.25 V	Group A subgroups	Dev. type	Limits		Unit
					Min	Max	
Delay of DAV true from end of write operation to data out register	t _{d1} <u>3/</u>	See figure 5	9,10,11	01	12t _C (∅)+	12t _C (∅)+310	ns
					8t _C (∅)+	8t _C (∅)+310	
					4t _C (∅)+	4t _C (∅)+310	ns
Delay of valid GPIB data lines from end of write cycle	t _{d2} <u>3/</u>		9,10,11	01		140	ns
Delay of B0 interrupt from DAC true	t _{d3} <u>3/</u>	B0 interrupt unmasked	9,10,11	01		300	ns
Delay of $\overline{\text{ACCGR}}$ DAC true	t _{d4} <u>3/</u>		9,10,11	01		300	ns
Delay of DAV false from DAC true	t _{d5} <u>3/</u>		9,10,11	01		160	ns
Delay of B1 interrupt from DAV true	t _{d6} <u>4/</u>	B1 interrupt unmasked, ATN = false, device in LASC See figure 5	9,10,11	01	2t _C (∅)+	2t _C (∅)+415	ns
Delay of $\overline{\text{ACCGR}}$ from DAV true	t _{d7} <u>4/</u>	ATN = false, device in LASC See figure 5	9,10,11	01	2t _C (∅)+	2t _C (∅)+290	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions -55°C < T _C < +110°C 4.75 V ≤ V _{CC} ≤ 5.25 V	Group A subgroups	Dev. type	Limits		Unit
					Min	Max	
Delay of NDAC false from DAV true	t _{d8} 4/	ATN = false, device in LACS See figure 5	9,10,11	01	3t _C (∅) ⁺	3t _C (∅) ⁺⁺ 445	ns
Delay of NRFD false from end of read operation of data-in register	t _{d9} 4/	See figure 5	9,10,11	01		220	ns
Delay of interface message interrupt from DAV true	t _{d10} 4/	ATN = false, device not in CACS, all interface message interrupts (except UNC) See figure 5	9,10,11	01	2t _C (∅) ⁺	2t _C (∅) ⁺⁺ 415	ns
		UNC interrupt only	9,10,11	01	5t _C (∅) ⁺	5t _C (∅) ⁺⁺ 415	ns
Delay of NDAC false from DAV true	t _{d11} 4/	ATN = true, device not in CACS, no DAC holdoff See figure 5	9,10,11	01	7t _C (∅) ⁺	7t _C (∅) ⁺⁺ 415	ns
Delay of NDAC false from end of write operation	t _{d12} 4/	See figure 5	9,10,11	01		230	ns
Delay of NRFD false from DAV false	t _{d13} 4/	ATN = true, device not in CACS See figure 5	9,10,11	01		180	ns
Delay of NDAC true from ATN true	t _{d14} 5/	Device is not in CACS See figure 5	9,10,11	01		195	ns
			9,10,11	01		125	ns
			9,10,11	01		140	ns
			9,10,11	01		125	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions -55°C < T _C < +110°C 4.75 V ≤ V _{CC} ≤ 5.25 V	Group A subgroups	Dev. type	Limits		Unit
					Min	Max	
Delay of NRFD true from ATN false	t _{d18} 5/	Device is in LADS/LACS See figure 5	9,10,11	01		140	ns
Response time to IFC	t _{d19} 5/	See figure 5	9,10,11	01	16t _C (∅)	30t _C (∅)	ns
Delay of ATN true from end of tca auxiliary command	t _{d20} 6/		9,10,11	01	8t _C (∅)	10t _C (∅)+220	ns
Delay of BO interrupt from end of tca auxiliary command	t _{d21} 6/		9,10,11	01	18t _C (∅)	22t _C (∅)+415	ns
Delay of ATN true from end of tcs auxiliary command	t _{d22} 6/	BO unmasked, device is in ANRS. See figure 5	9,10,11	01	8t _C (∅)	10t _C (∅)+220	ns
Delay of BO interrupt from end of tcs auxiliary command	t _{d23} 6/	BO unmasked, device is in ANRS. See figure 5	9,10,11	01	18t _C (∅)	22t _C (∅)+415	ns
Delay of EOI true from rpp auxiliary command set	t _{d24} 6/	See figure 5	9,10,11	01		230	ns
Delay of EOI false from rpp auxiliary command set	t _{d25} 6/		9,10,11	01		230	ns
Delay of BO interrupt from rpp auxiliary command cleared	t _{d26} 6/	BO unmasked. See figure 5	9,10,11	01	8t _C (∅)	10t _C (∅)+415	ns
Delay of ATN false from gts auxiliary command	t _{d27} 6/	Device is not in SDYS or STRS. See figure 5	9,10,11	01		210	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions -55°C < T _C < +110°C 4.75 V ≤ V _{CC} ≤ 5.25 V	Group A subgroups	Dev. type	Limits		Unit
					Min	Max	
Clock cycle time	t _C (∅)	See figure 5	9,10,11	01	0.2	2.0	μs
Clock high pulse duration	t _w (∅H)		9,10,11	01	1955		ns
Clock low pulse duration	t _w (∅L)		9,10,11	01	45		ns
Address setup time	t _{su} (AD)		9,10,11	01	0		ns
DBIN setup time 7/	t _{su} (DBIN)		9,10,11	01	0		ns
CE setup time	t _{su} (CE)		9,10,11	01	100		ns
WE setup time 7/	t _{su} (WE)		9,10,11	01	0		ns
Data setup time	t _{su} (DA)		9,10,11	01	80		ns
Data hold time	t _h (DA)		9,10,11	01	15		ns
Address hold time	t _h (AD)		9,10,11	01	0		ns
DBIN hold time 7/	t _h (DBIN)		9,10,11	01	0		ns
CE hold time	t _h (CE)		9,10,11	01	80		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions -55°C ≤ T _C ≤ +110°C 4.75 V ≤ V _{CC} ≤ 5.25 V	Group A subgroups	Dev. type	Limits		Unit					
					Min	Max						
\overline{ACCGR} setup time	t _{su} (GR)	See figure 5	9,10,11	01	100		ns					
\overline{ACCGR} hold time	t _h (GR)							9,10,11	01	80		ns
\overline{WE} low pulse duration	t _w (WE)											

- 1/ Timing measurements are referenced to or from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.
- 2/ A very short bus settling time (t₁) occurs on the second and subsequent data byte when ATN is false if the "vstd1" feature is set. A slightly longer bus settling time takes place if "std1" is set unless there is a very short bus settling time. In all other instances, a normal bus settling time occurs.
- 3/ Source handshake timing characteristics. The timing of the source handshake is the same whether ATN is true or false; i.e., whether the device is in TACS, CACS, or SPAS.
- 4/ Acceptor handshake timing characteristics.
- 5/ ATN, EOI, and IFC timing characteristics.
- 6/ Controller timing characteristics.
- 7/ Guaranteed to the limits specified herein, if not tested.

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Device type 01

Case Q

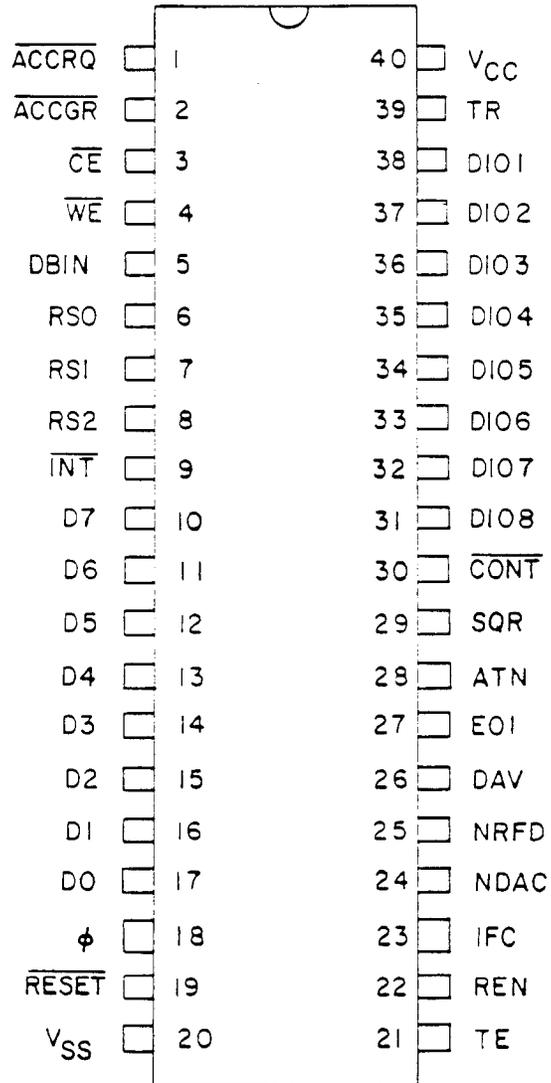


FIGURE 1. Terminal connections.

**STANDARDIZED
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DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

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Case X

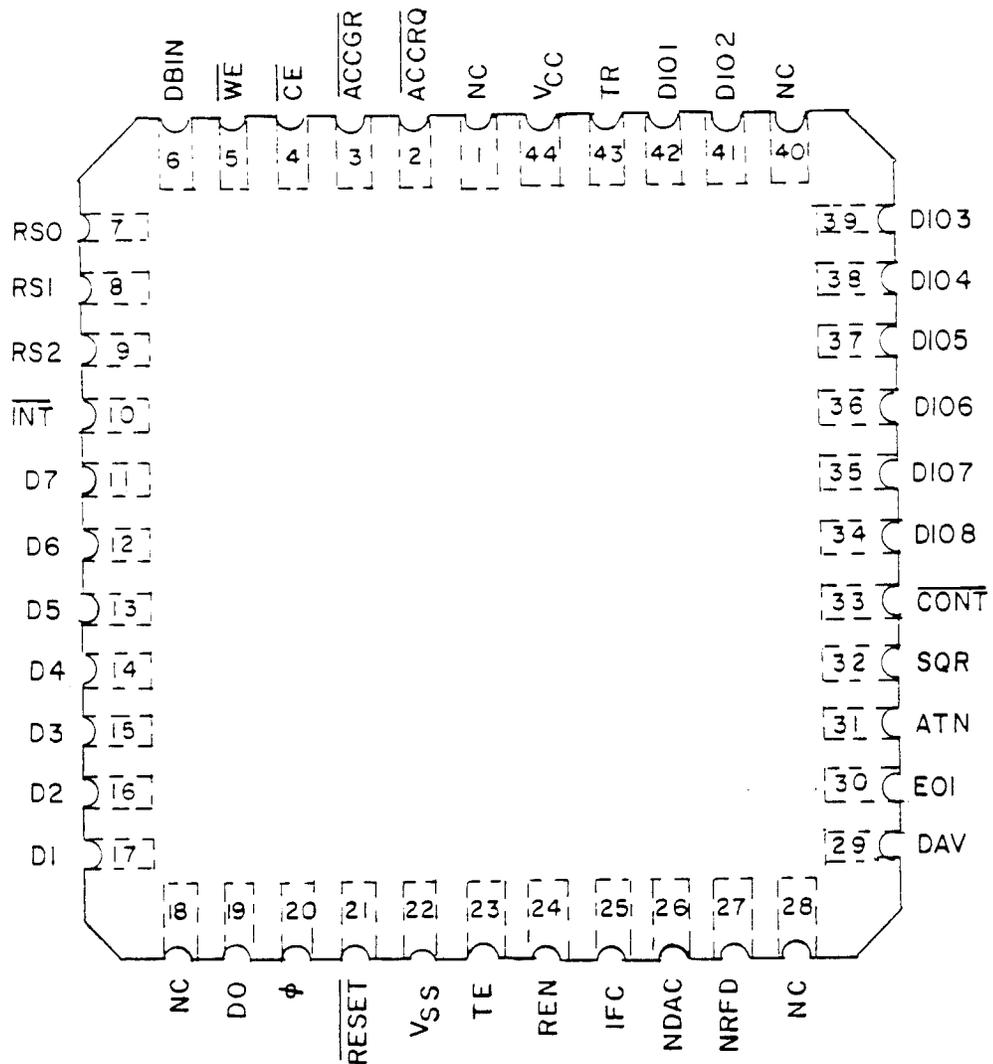


FIGURE 1. Terminal connections - Continued.

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Device type 01

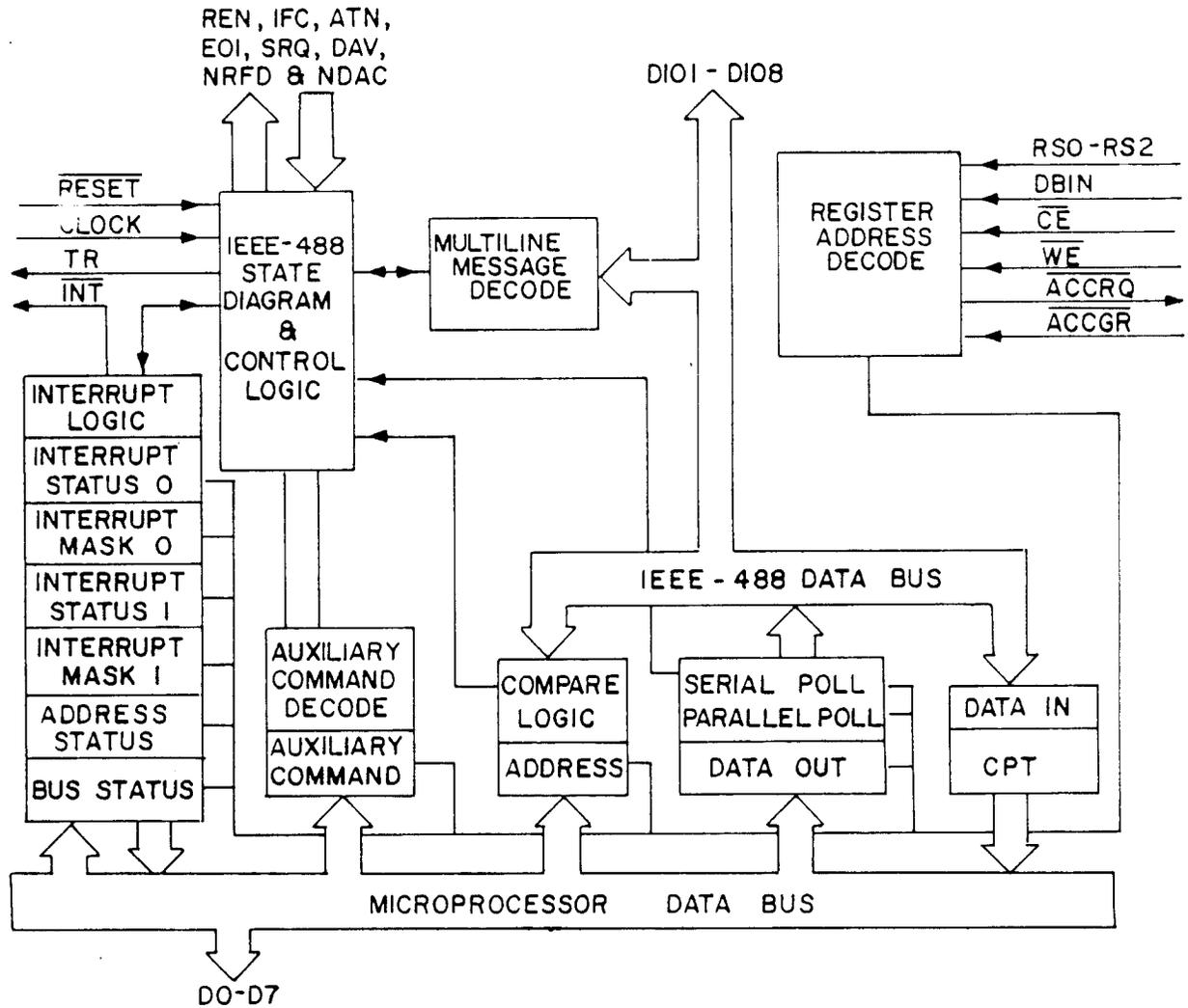


FIGURE 2. Functional block diagram.

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Device type 01

Address			Read registers	Write registers
RS2	RS1	RS0		
0	0	0	Interrupt status 0	Interrupt mask 0
0	0	1	Interrupt status 1	Interrupt mask 1
0	1	0	Address status	See note 1
0	1	1	Bus status	Auxiliary command
1	0	0	See note 2	Address
1	0	1	See note 2	Serial poll
1	1	0	Command pass thru	Parallel poll
1	1	1	Data in	Data out

NOTES:

1. This address is not decoded by the device. A write to this location will have no effect on the device, as if a write had not occurred.
2. The device host interface data lines will remain in the high-impedance state when these register locations are addressed. An address switch register may therefore be included in the address space of the device at these locations.

FIGURE 3. Register addresses.

Device type 01

Data-in register										
Address			Bit assignment							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	1	1	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

GP1B

Data-out register										
Address			Bit assignment							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	1	1	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

GP1B

FIGURE 4. Internal registers.

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Device type 01

Auxiliary-command register										
Address			Bit assignment							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
0	1	1	cs	xx	xx	f4	f3	f2	f1	f0

cs = Clear or set
xx = Don't care

f4-f0 = Auxiliary command select

Interrupt mask/status register 0											
Address			Bit assignment								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
0	0	0	xx	xx	B1	B0	END	SPAS	RLC	MAC	INT MASK 0
0	0	0	INT0	INT1	B1	B0	END	SPAS	RLC	MAC	INT STAT 0

INT1 = Interrupt status register 1
INT0 = Interrupt status register 0
BI = Byte in
BO = Byte out
XX = Don't care

END = Last byte in string received
SPAS = Device has been serial polled
RLC = Remote local change
MAC = My address change

Interrupt mask/status register 1											
Address			Bit assignment								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
0	0	1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC	INT MASK 1
0	0	1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC	INT STAT 1

GET = Group execute trigger
ERR = Error
UNC = Unrecognized command
APT = Address pass through

DCAS = Device clear active state
SRQ = Service request
MA = My address
IFC = Interface clear

FIGURE 4. Internal registers - Continued.

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Device type 01

Address status register										
Address			Bit assignment							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
0	1	0	REM	LLO	ATN	LPAS	TPAS	LADS	TADS	ulpa

REM = Remote state
LLO = Local lockout

ATN = Attention

LPAS = Listener primary addressed state

TPAS = Talker primary addressed state

LADS = Addressed to listen

TADS = Addressed to talk

ulpa = LSB last address

Address register										
Address			Bit assignment							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	0	0	edpa	dal	dat	A5	A4	A3	A2	A1

edpa = Enable dual-primary addressing mode

dal = Disable listener function

dat = Disable talker function

A5-A1 = Primary address

Bus status register										
Address			Bit assignment							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
0	1	1	ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN

FIGURE 4. Internal registers - Continued.

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Device type 01

Serial poll register										
Address			Bit assignment							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	0	1	S8	rsv1	S6	S5	S4	S3	S2	S1
			DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

GPIB
 S8, S6-S1 = Device status
 rsv1 = Request service bit 1

Command pass through register										
Address			Bit assignment							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	1	0	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

GPIB

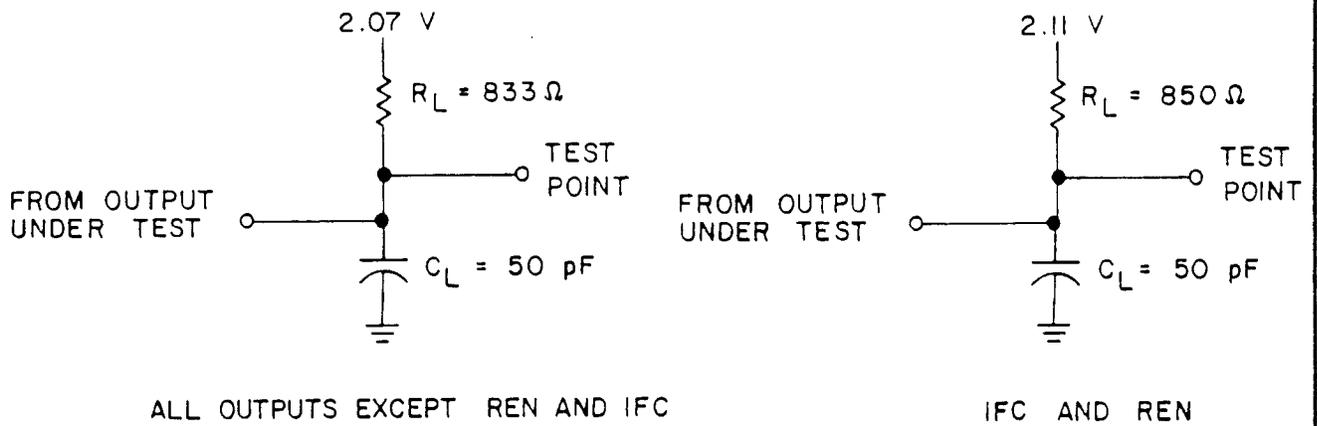
Parallel poll register										
Address			Bit assignment							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	1	0	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1
			DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

GPIB

FIGURE 4. Internal registers - Continued.

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Device type 01



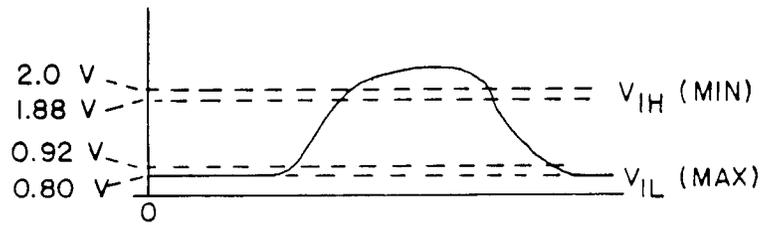
NOTE: Timing measurements are referenced to or from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 5. Switching test circuits and waveforms.

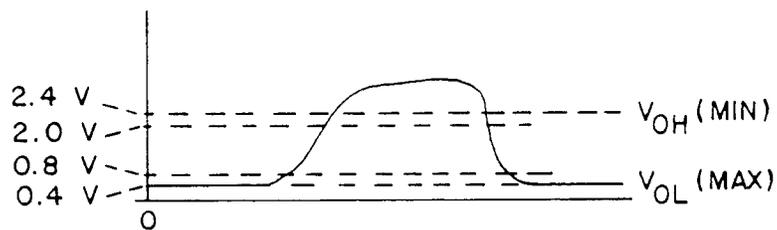
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Device type 01

Voltage reference levels



INPUT



OUTPUTS

High impedance measurement

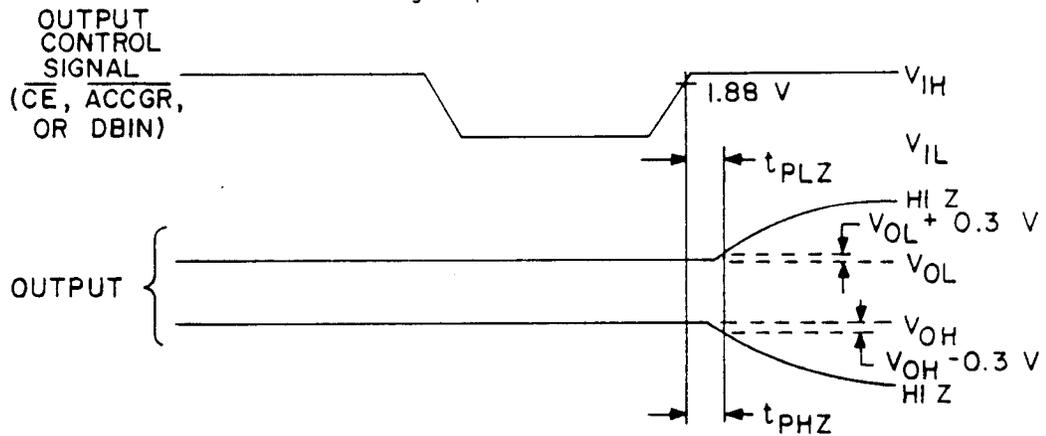
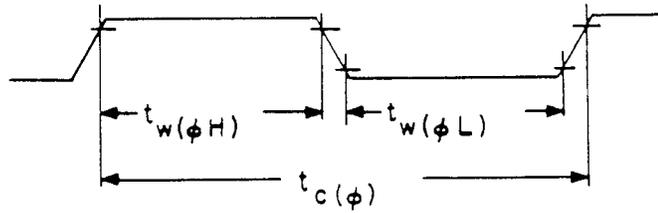


FIGURE 5. Switching test circuits and waveforms - Continued.

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Device type 01

CLOCK CYCLE TIMING



READ CYCLE TIMING

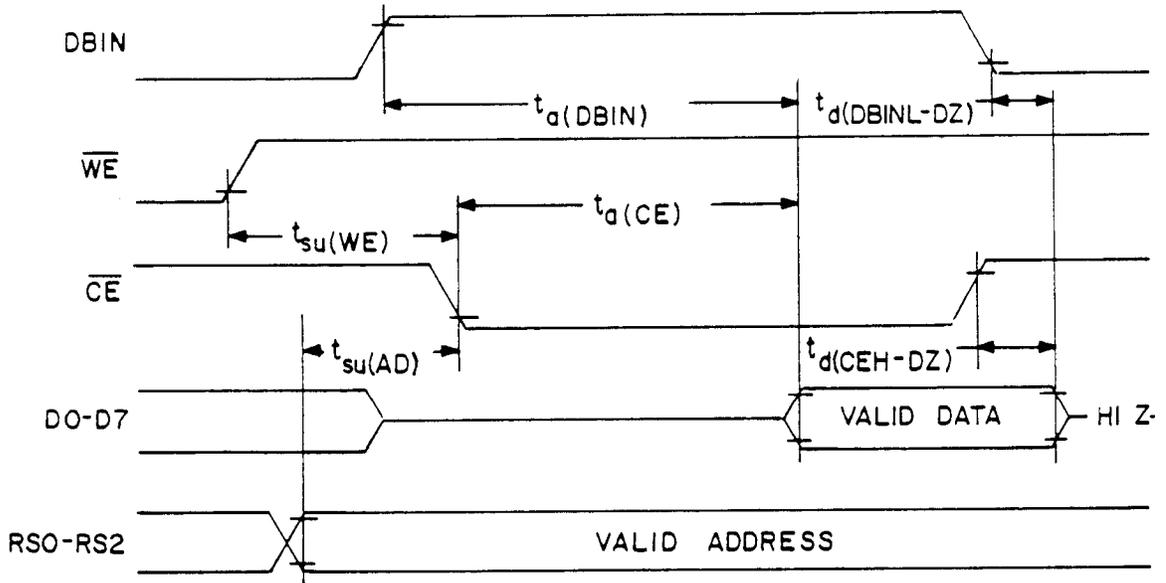
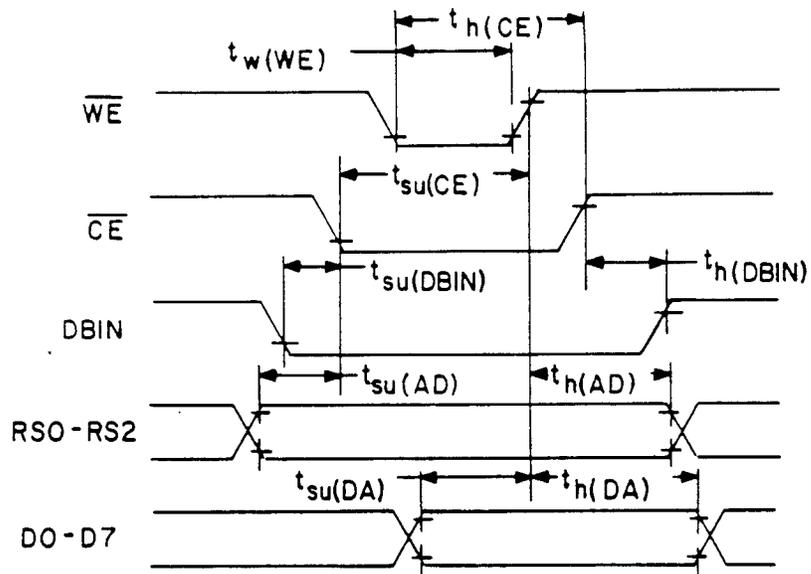


FIGURE 5. Switching test circuits and waveforms - Continued.

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Device type 01

WRITE CYCLE TIMING



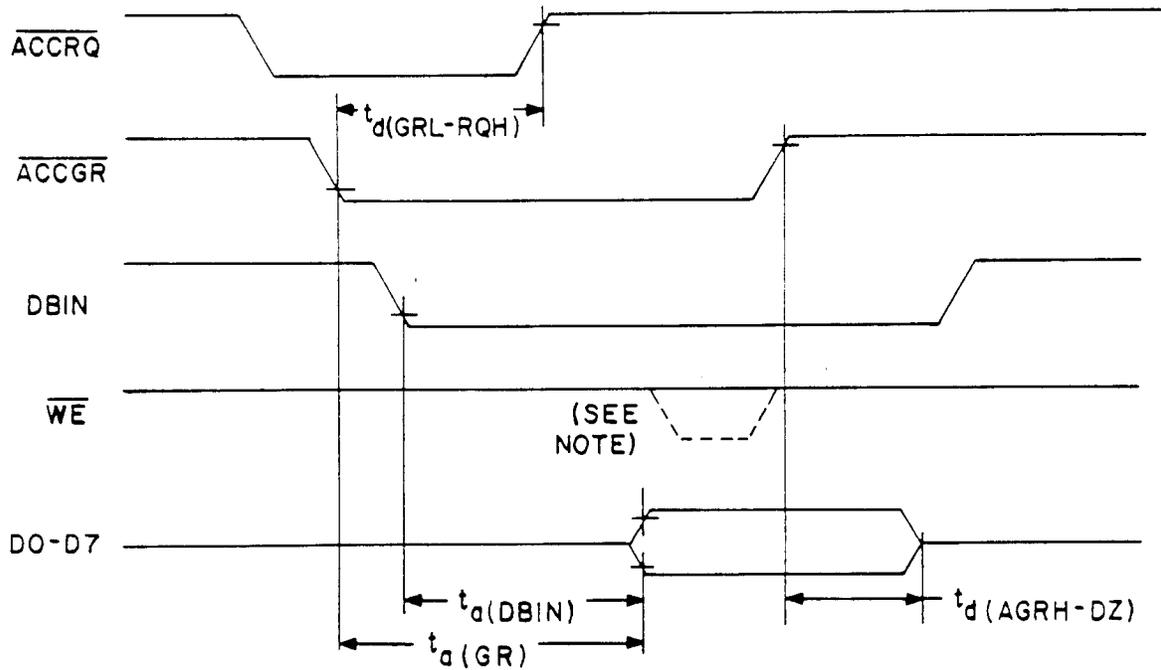
NOTE: $t_h(AD)$ and $t_h(DA)$ are shown measured from the rising edge of \overline{WE} . This is the correct reference point in this figure, since the measurements should be from the rising edge of \overline{WE} or \overline{CE} - whichever comes first.

FIGURE 5. Switching test circuits and waveforms - Continued.

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Device type 01

DMA READ OPERATION



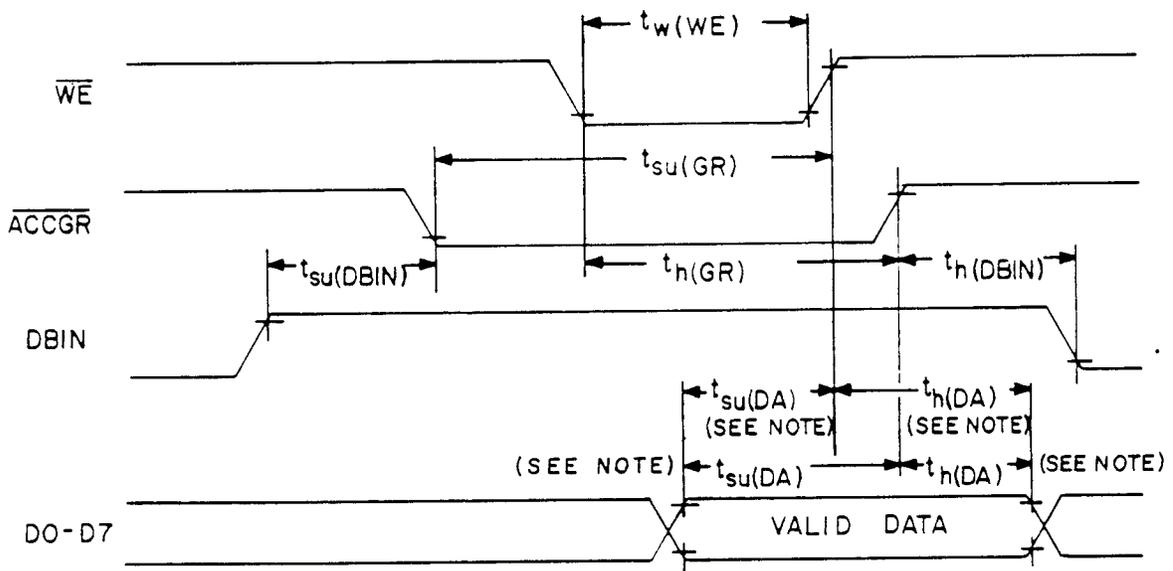
NOTE: A write-enable pulse may occur in a DMA read operation. A write-enable pulse may therefore be provided for system memory and need not be suppressed at the device.

FIGURE 5. Switching test circuits and waveforms - Continued.

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Device type 01

DMA WRITE OPERATION

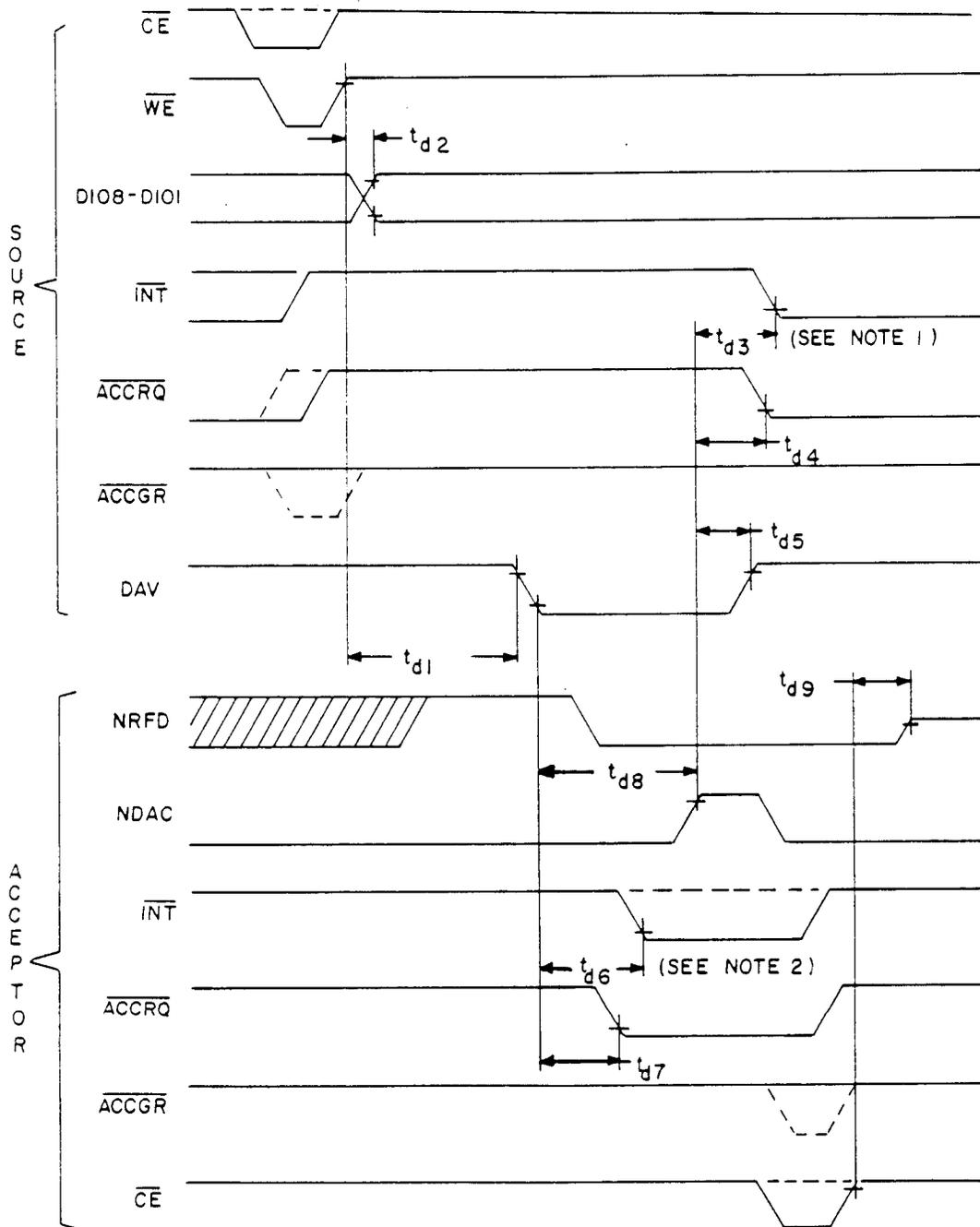


NOTE: $t_{su}(DA)$ and $t_h(DA)$ are only applicable to the first signal to become inactive, whether it is \overline{WE} or \overline{ACCGR} .

FIGURE 5. Switching test circuits and waveforms - Continued.

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SOURCE AND ACCEPTOR HANDSHAKE TIMING



NOTES:

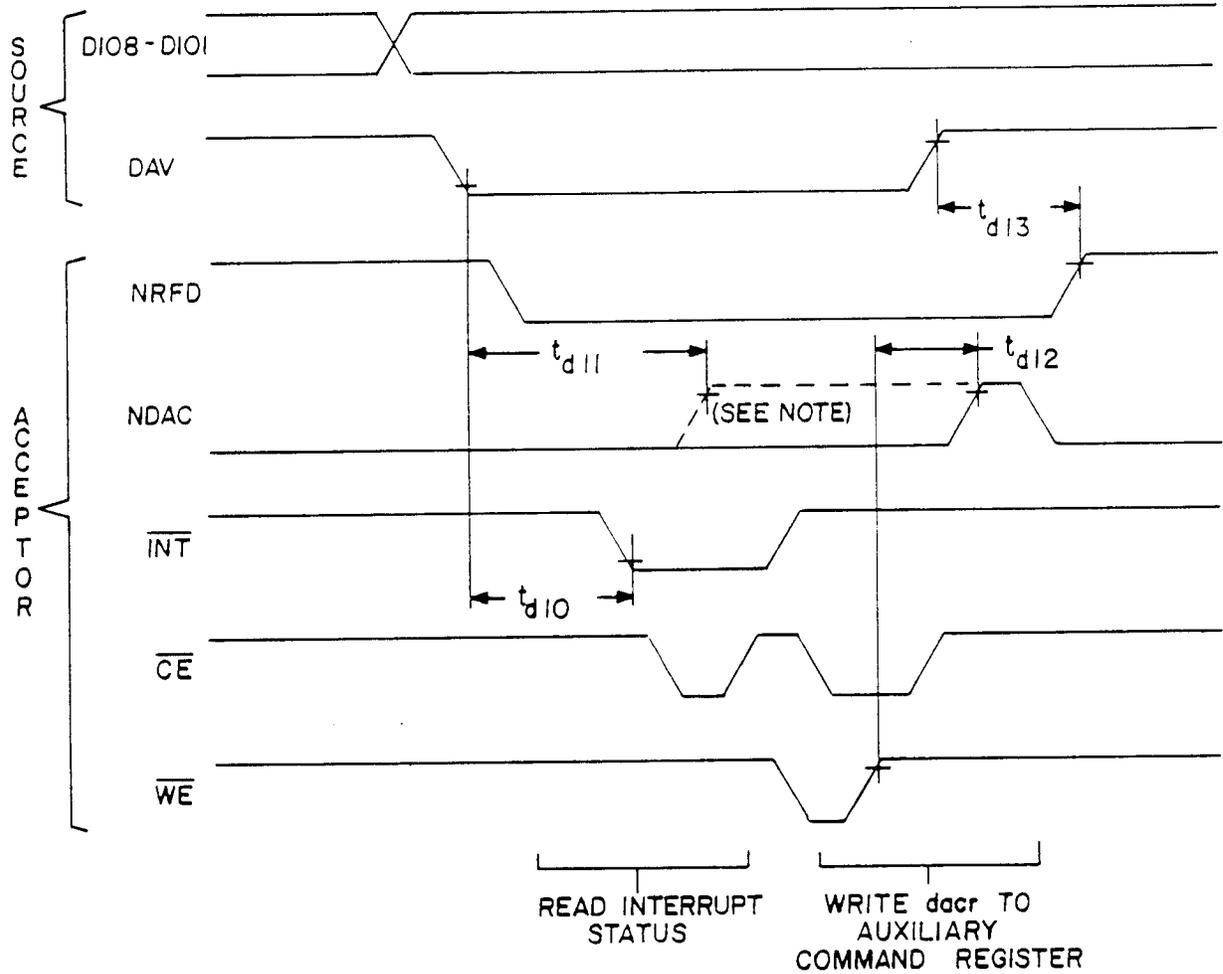
1. The interrupt line is taken low by a B0 interrupt.
2. The interrupt line is taken low by a B1 interrupt.

FIGURE 5. Switching test circuits and waveforms - Continued.

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Device type 01

ACCEPTOR HANDSHAKE TIMING "ATN" TRUE



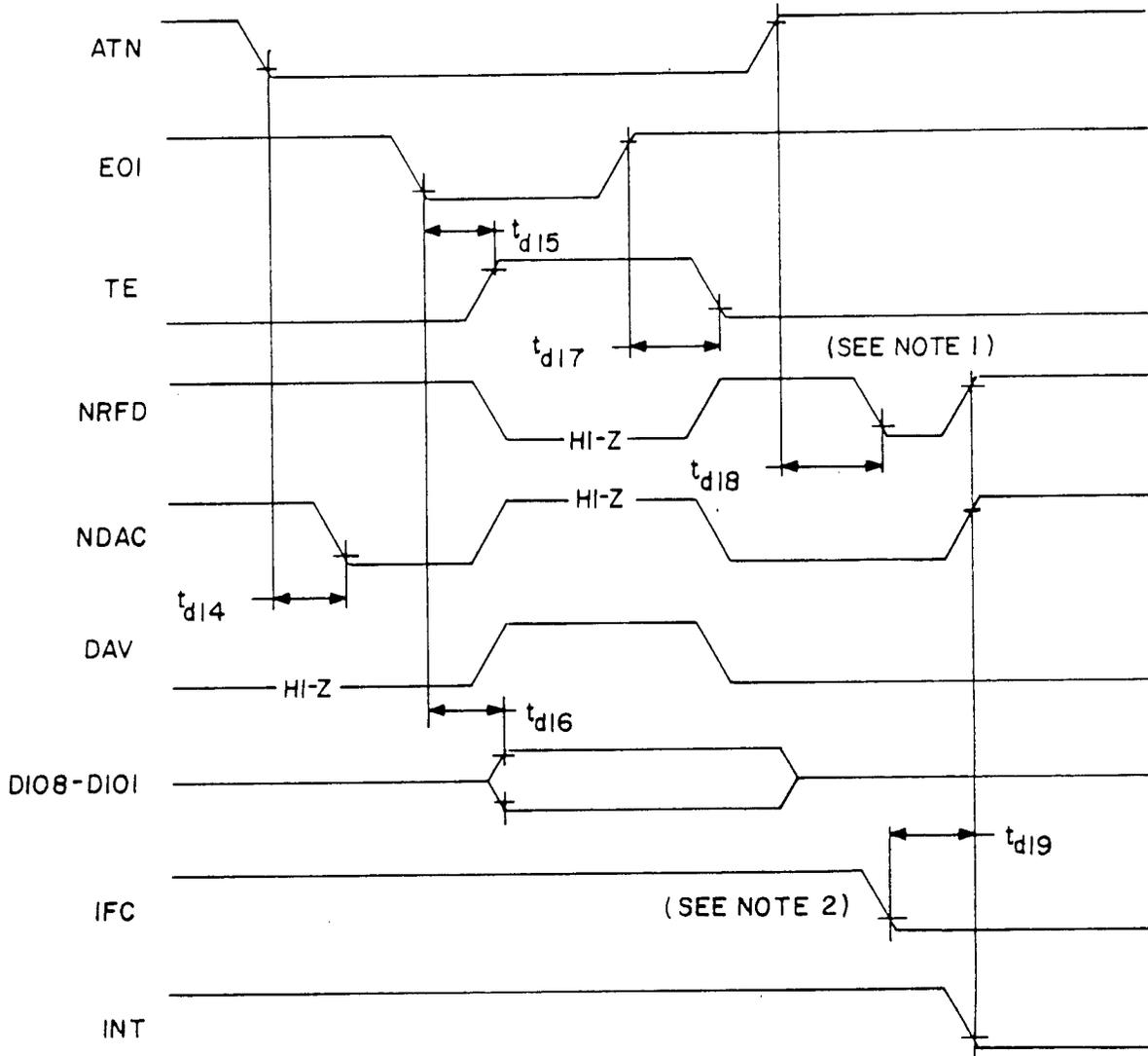
NOTE: The broken line shows the waveform if there is no DAC holdoff. The solid lines assume there is a DAC holdoff.

FIGURE 5. Switching test circuits and waveforms - Continued.

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Device type 01

RESPONSE TO "ATN" AND "EOI"



NOTES:

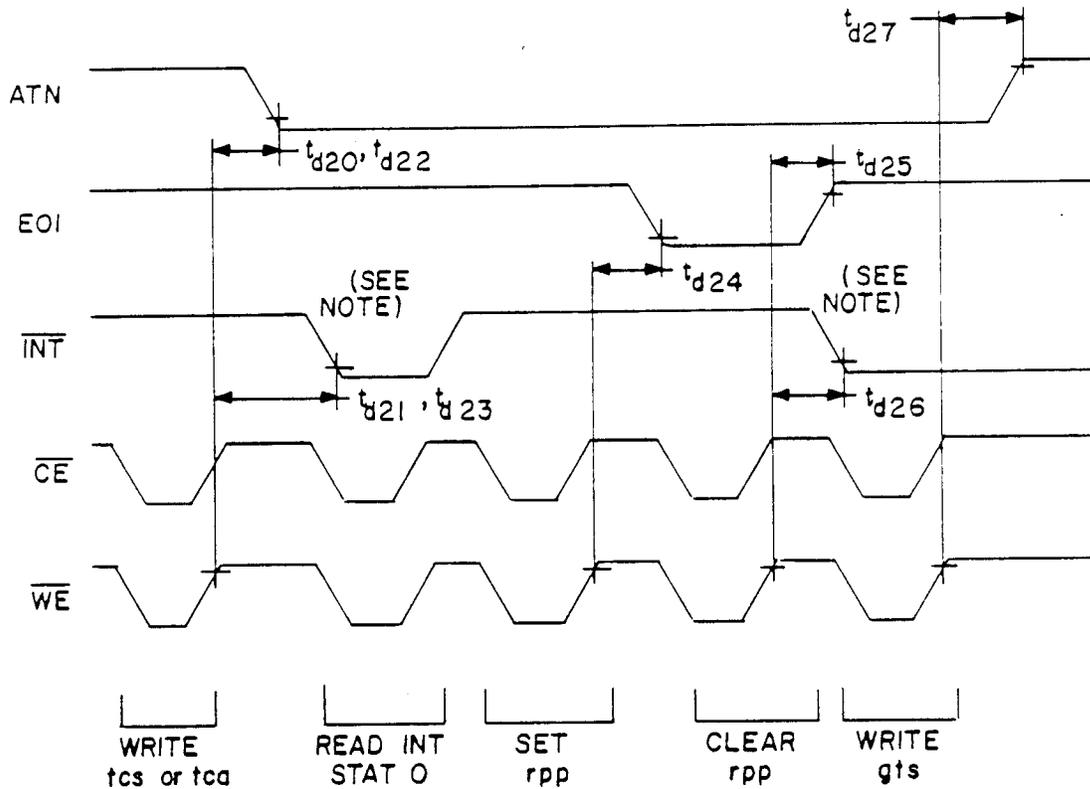
- 1. This assumes that an RFD holdoff occurs.
- 2. IFC causes the device to be unaddressed and an IFC interrupt occurs.

FIGURE 5. Switching test circuits and waveforms - Continued.

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Device type 01

CONTROLLER TIMING



NOTE: A BO interrupt occurs as the device enters CACS.

FIGURE 5. Switching test circuits and waveforms - Continued.

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3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 tests shall verify the functionality of the device. It forms a part of the vendor's test tape and shall be maintained and available from the approved sources of supply.

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TABLE II. Electrical test requirements. 1/ 2/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10

1/ (*) indicates PDA applies to subgroup 1.

2/ Any or all subgroups may be combined when using high-speed testers.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) $T_A = +125^\circ\text{C}$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Pin descriptions.

Pin <u>1/</u>		I/O (type)	Description
No.	Name		
1	ACCGRQ	0 <u>2/</u>	Access request. This pin becomes active (low) to request a direct memory access.
2	ACCGR	I	Access granted. When received from the direct-memory-access control logic, this enables the byte onto the data bus. ACCGR must be high when not participating in DMA transfer.
3	CE	I	Chip enable. CE allows access for read and write registers. If CE is high, D0-D7 are in high impedance unless ACCGR is low.
4	WE	I	Write enable. When active (low) indicates to the device that data is being written to one of its registers.
5	DBIN	I	Data bus in. An active (high) state indicates to the device that a read is about to be carried out by the MPU.
6	RS0	I	Register select lines. Determine which register is addressed by the MPU during a read or write operation.
7	RS1	I	
8	RS2	I	
9	INT	0 <u>3/</u>	Interrupt. Sent to the MPU to cause a branch to a service routine.
10-17	D0-D7	I/O <u>2/</u>	Data transfer bit lines on the MPU side of the device. D0 is the most-significant bit.
18	∅	I	Clock input. 500 kHz to 5 MHz. Need not be synchronous to system clock.
19	RESET <u>4/</u>	I	Initializes the device at power on.
20	V _{SS}		Ground reference voltage.
21	TE	0 <u>2/</u>	Talk enable. Controls the direction of the transfer of the line transceivers. Logically, it is: $\overline{[CACS + TACS + EIO.ATN.(CIDS + CADS)/SWRST]}$.

See footnotes at end of pin descriptions.

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Pin <u>1/</u>		I/O (type)	Description
No.	Name		
22	REN	I/O <u>5/</u>	Remote enable. Sent by system controller to select control, either from the front panel or from the IEEE bus.
23	IFC	I/O <u>5/</u>	Interface clear. Sent by the system controller to set the interface system into a known quiescent state. The system controller becomes the controller in charge.
24	NDAC	I/O <u>2/</u>	Not data accepted. Handshake line. Acceptor sets this false (high) when it has latched the data from the I/O lines.
25	NRFD	I/O <u>2/</u>	Not ready for data. Handshake line. Sent by acceptor to indicate readiness for the next byte.
26	DAV	I/O <u>2/</u>	Data valid. Handshake line controlled by source to show acceptors when valid data is present to the bus.
27	EOI	I/O <u>2/</u>	End or identify. If ATN is false (high), this indicates the end of a message block. If ATN is true (low), the controller is requesting a parallel poll.
28	ATN	I/O <u>2/</u>	Attention. Sent by controller in charge. When true (low) interface commands are being sent over the DIO lines. When false (high), these lines carry data.
29	SRQ	I/O <u>2/</u>	Service request. Set true (low) by a device to indicate a need for service.
30	CONT	0 <u>2/</u>	Indicates (low) if a device is controller in charge. It is used to control direction of SRQ and ATN in pass control systems. Logically, it is: (CIDS + CADS).
31-38	DIO1-DIO8	I/O <u>2/</u>	DIO8 through DIO1 are the data input/output lines on the GPIB side. These pins connect to the IEEE-488 bus via non-inverting transceivers.
39	TR	0 <u>2/</u>	Trigger. Activated when the GET command is received over the interface or the get command is given by the MPU.
40	VCC		Supply voltage (5 V nominal).

See footnotes on next page.

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- 1/ Pin numbers given are for case outline Q.
- 2/ Push-pull output.
- 3/ Open-drain output with no internal pullup.
- 4/ The hardware RESET pin has the following effect on the device:
 - a. Serial and parallel poll registers cleared.
 - b. All clear/set auxiliary commands cleared except "swrst".
 - c. "swrst" auxiliary command set. This holds the device in known states.
- 5/ Open-drain output with internal pullup.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8751901QX	01295	SMJ9914AJJS	
5962-8751901XX	01295	SMJ9914AFDS	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments, Inc.
P. O. Box 6448
Midland, TX 79711

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