

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes according to NOR 5962-R125-92. tvn	92-02-05	Mionica L. Poelking
B	Update to reflect latest changes in format and requirements. Editorial changes throughout. -les	01-11-29	Raymond Monnin
C	Update drawing to current requirements. Editorial changes throughout. - gap	09-03-18	Robert M. Heber
D	Update to current MIL-PRF-38535 requirements. - rdc	15-11-09	Charles F. Saffle
E	Update drawing to latest MIL-PRF-38535 requirements. - jt	20-09-01	James R. Eschmeyer



THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

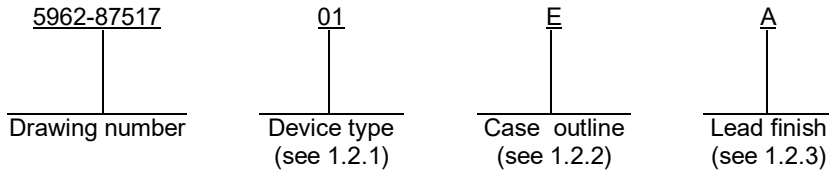
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REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E				
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12							

PMIC N/A	PREPARED BY David W. Queenan	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime</p>		
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY Robert P. Evans			
	APPROVED BY Michael A. Frye			
	DRAWING APPROVAL DATE 88-01-26			
AMSC N/A	REVISION LEVEL E	SIZE A	CAGE CODE 67268	5962-87517
		SHEET 1 OF 12		

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54LS590	8-bit binary counter with three-state output registers

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat package
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V to +7.0 V
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P _D) ^{1/}	357 mW
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T _J)	+175°C
Thermal resistance, junction-to-case (θ _{JC})	See MIL-STD-1835
Input voltage range	-1.5 V at -18 mA to +7.0 V
Off-state output voltage, maximum	5.5 V

^{1/} Must withstand the added P_D, due to short-circuit test, e.g., I_{os}.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-87517
		REVISION LEVEL E	SHEET 2

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V to 5.5 V
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Maximum high level output current:	
\overline{RCO}	-1 mA
Q	-1 mA
Maximum low level output current:	
\overline{RCO}	8 mA
Q	12 mA
Counter clock frequency (f_{CCK})	0 MHz to 20 MHz
Register clock frequency (f_{RCK})	0 MHz to 25 MHz
Minimum counter clock pulse width (t_{WCCK})	25 ns
Minimum counter clear pulse width (t_{WCCLR})	20 ns
Minimum register clock pulse width (t_{WRCK})	20 ns
Minimum setup time (t_{su}) :	
\overline{CCKEN}	20 ns
\overline{CCLR}	20 ns
CCK before RCK \uparrow ^{2/}	40 ns
Minimum hold time (t_h)	0 ns
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

^{2/} This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-87517
		REVISION LEVEL E	SHEET 3

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit and waveforms. The test circuit and waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-87517
		REVISION LEVEL E	SHEET 4

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -1 mA, V _{IN} = 0.7 V or 2.0 V		1, 2, 3	01	2.4		V
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, V _{IN} = 0.7 V or 2.0 V	I _{OL} = 8 mA RCO output	1, 2, 3	01		0.4	V
			I _{OL} = 12 mA Q output	1, 2, 3	01		0.4	V
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA		1, 2, 3	01		-1.5	V
High level input current	I _{IH1}	V _{CC} = 5.5 V, V _{IN} = 7.0 V		1, 2, 3	01		0.1	mA
	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 2.7 V		1, 2, 3	01		20	μA
Low level input current	I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.4 V	CCK input	1, 2, 3	01		-0.8	mA
			All other inputs	1, 2, 3	01		-0.2	mA
Short-circuit output current	I _{OS}	V _{CC} = 5.5 V, V _{OUT} = 0.0 V <u>1/</u>	RCO output	1, 2, 3	01	-20	-100	mA
			Q output	1, 2, 3	01	-30	-130	mA
Off-state output current, high level voltage applied	I _{OZH}	V _{CC} = 5.5 V, V _{OUT} = 2.7 V, V _{IN} = 0.7 V or 2.0 V		1, 2, 3	01		20	μA
Off-state output current, low level voltage applied	I _{OZL}	V _{CC} = 5.5 V, V _{OUT} = 0.4 V, V _{IN} = 0.7 V or 2.0 V		1, 2, 3	01		-20	μA
Supply current	I _{CCH}	V _{CC} = 5.5 V, All possible inputs grounded, all outputs open		1, 2, 3	01		55	mA
	I _{CCL}			1, 2, 3	01		65	mA
	I _{CCZ}			1, 2, 3	01		65	mA
Functional test		See 4.3.1c		7	01			

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-87517

REVISION LEVEL
E

SHEET
5

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Maximum count frequency	f _{MAX}	V _{CC} = 5.0 V, R _L = 666 Ω, C _L = 45 pF	9	01	20		MHz	
			10, 11	01	12		MHz	
Propagation delay time, CCK to \overline{RCO}	t _{PLH1}	V _{CC} = 5.0 V R _L = 1 kΩ C _L = 30 pF See figure 4	9	01		22	ns	
			10, 11	01		31	ns	
	t _{PHL1}		9	01		30	ns	
			10, 11	01		43	ns	
Propagation delay time, CCLR to \overline{RCO}	t _{PLH2}	V _{CC} = 5.0 V R _L = 667 Ω C _L = 45 pF See figure 4	9	01		45	ns	
			10, 11	01		64	ns	
Propagation delay time, RCK to Q	t _{PLH3}		V _{CC} = 5.0 V R _L = 667 Ω C _L = 45 pF See figure 4	9	01		18	ns
				10, 11	01		26	ns
	t _{PHL3}	9		01		33	ns	
		10, 11		01		47	ns	
Propagation delay time, \overline{G} to Q	t _{PZH}	V _{CC} = 5.0 V R _L = 667 Ω C _L = 45 pF See figure 4	9	01		38	ns	
			10, 11	01		60	ns	
	t _{PZL}		9	01		45	ns	
			10, 11	01		64	ns	
Propagation delay time, \overline{G} to Q	t _{PHZ}	V _{CC} = 5.0 V R _L = 667 Ω C _L = 5 pF See figure 4	9	01		30	ns	
			10, 11	01		43	ns	
	t _{PLZ}		9	01		38	ns	
			10, 11	01		60	ns	

1/ Not more than one output should be shorted at a time and the duration of the short-circuit condition should not exceed one second.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-87517
		REVISION LEVEL E	SHEET 6

Case outlines	E and F	2
Terminal number	Terminal symbol	
1	Q _B	NC
2	Q _C	Q _B
3	Q _D	Q _C
4	Q _E	Q _D
5	Q _F	Q _E
6	Q _G	NC
7	Q _H	Q _F
8	GND	Q _G
9	$\overline{\text{RCO}}$	Q _H
10	$\overline{\text{CCLR}}$	GND
11	CCK	NC
12	$\overline{\text{CCKEN}}$	$\overline{\text{RCO}}$
13	RCK	$\overline{\text{CCLR}}$
14	$\overline{\text{G}}$	CCK
15	Q _A	$\overline{\text{CCKEN}}$
16	V _{CC}	NC
17		RCK
18		$\overline{\text{G}}$
19		Q _A
20		V _{CC}

NC = No connection

FIGURE 1. Terminal connections.

Inputs					Device state
$\overline{\text{G}}$	$\overline{\text{CCLR}}$	$\overline{\text{CCKEN}}$	CCK	RCK	
H	X	X	X	X	Disabled
L	L	X	X	↑	Clear
L	H	H	X	X	No change
L	H	L	↑	X	Internal count
L	H	L	↑	↑	External count

H = High level voltage
L = Low level voltage
X = irrelevant
↑ = Low to high clock transition.

FIGURE 2. Truth table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-87517
		REVISION LEVEL E	SHEET 7

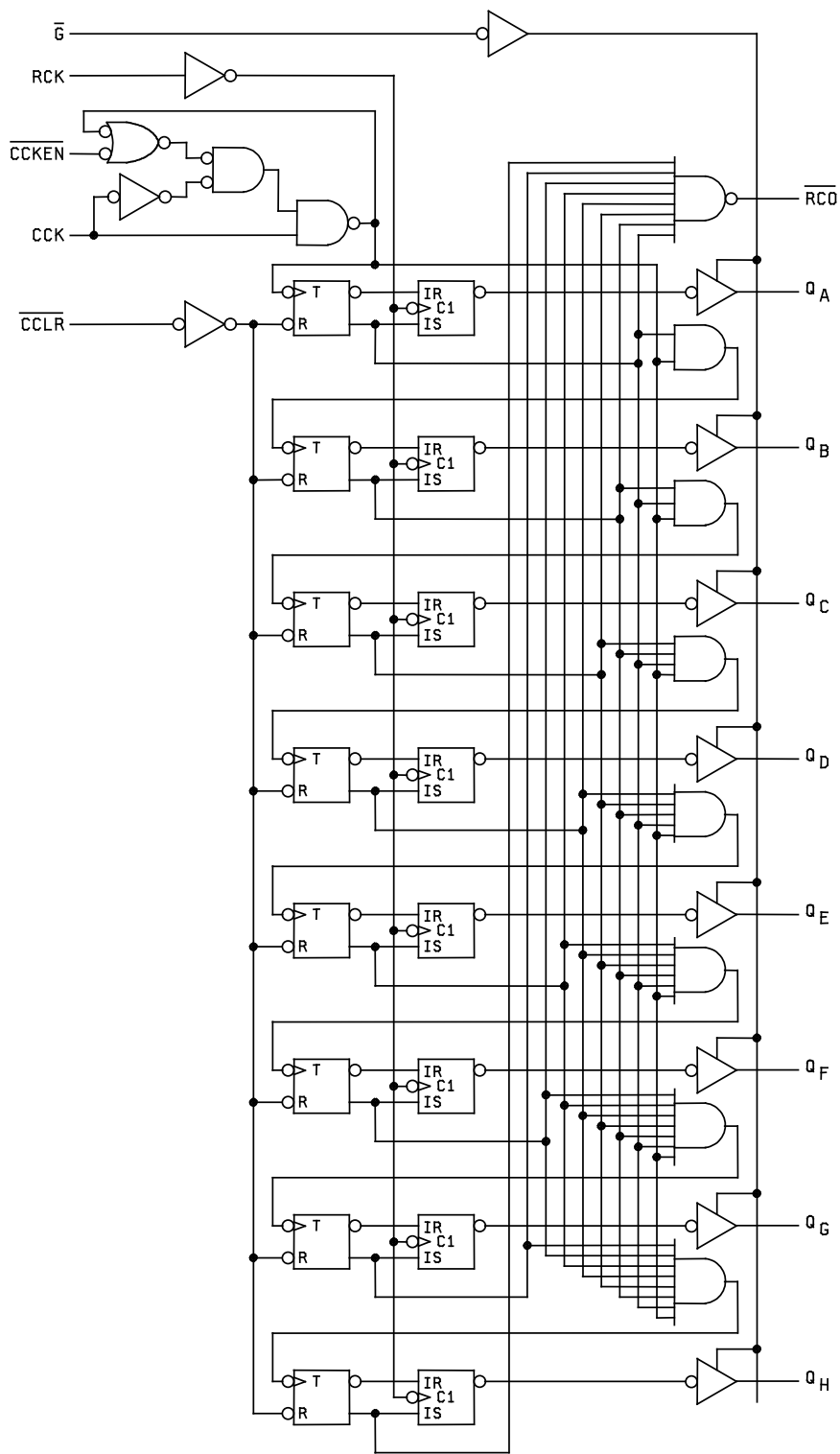


FIGURE 3. Logic diagram.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-87517

REVISION LEVEL
E

SHEET
8

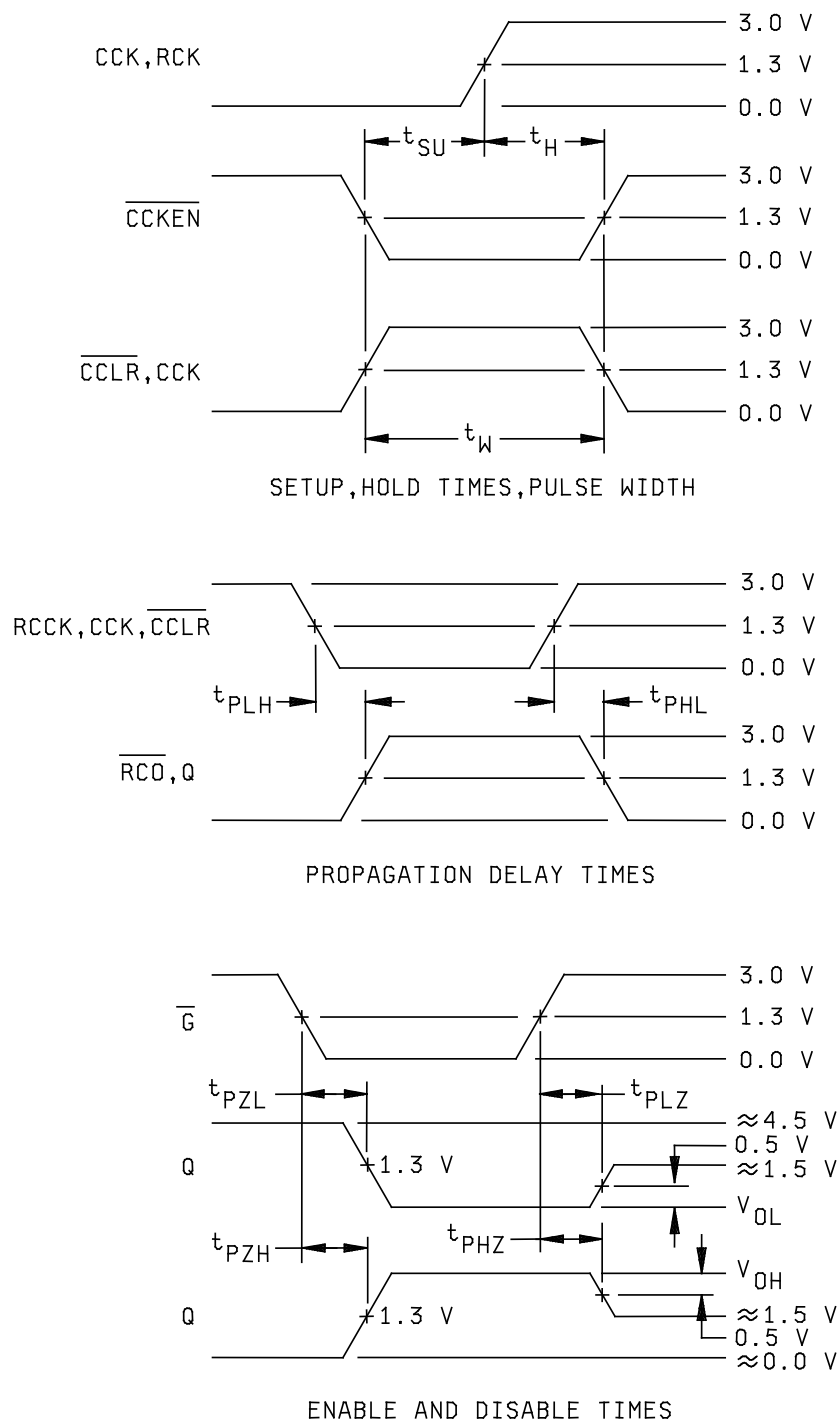
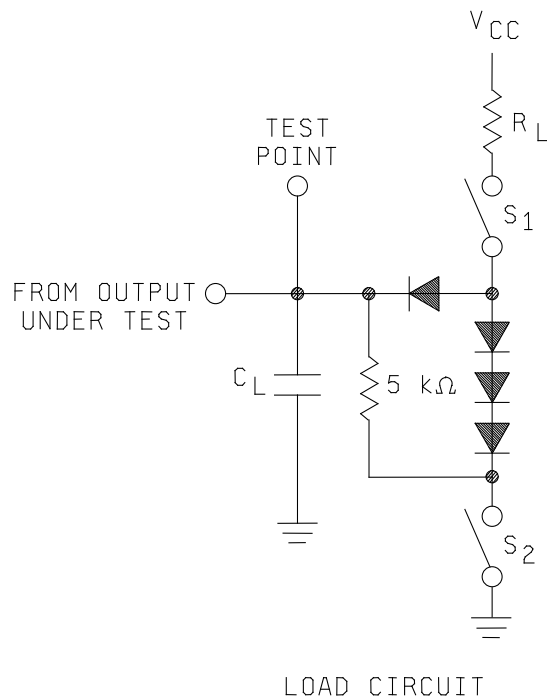


FIGURE 4. Test circuit and switching waveforms.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-87517
		REVISION LEVEL E	SHEET 9



NOTES:

1. The pulse generator shall have the following characteristics: $PRR \leq 1 \text{ MHz}$; $t_R \leq 15 \text{ ns}$; $t_F \leq 6 \text{ ns}$.
2. C_L includes scope probe, wiring, and stray capacitance without the package in the test fixture.
3. All diodes are 1N3064, 1N916, or equivalent.
4. Switches S_1 and S_2 shall be set for enable and disable time tests as follows:
 t_{PZL} : S_1 closed, S_2 open
 t_{PZH} : S_1 open, S_2 closed
 t_{PLZ} and t_{PHZ} : S_1 and S_2 closed

FIGURE 4. Test circuit and switching waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-87517
		REVISION LEVEL E	SHEET 10

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 shall include verification of the truth table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-87517
		REVISION LEVEL E	SHEET 11

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-87517
		REVISION LEVEL E	SHEET 12

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-09-01

Approved sources of supply for SMD 5962-87517 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8751701EA	01295	SNJ54LS590J
5962-8751701FA	<u>3/</u>	SNJ54LS590W
5962-87517012A	01295	SNJ54LS590FK

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source.

Vendor CAGE
number

01295

Vendor name
and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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