REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make changes to paragraphs 1.3, 4.3.1c, table I, and figure 3. Make editorial changes throughout.	89-01-30	M. A. Frye
B	Add one vendor, CAGE 07933. Make changes to table I and editorial changes throughout. Remove vendor CAGE 34371. Device 013X is not available from an approved source of supply.	90-05-30	M. A. Frye
C	Changes in accordance with N.O.R. 5962-R013-91.	91-09-27	M. A. Frye
D	Drawing updated to reflect current requirements. - ro	02-07-08	R. Monnin
E	Redrawn. Update paragraphs to MIL-PRF-38535 requirements. - drw	14-10-09	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS				REV			E	E	E	E	E	E	E	E	E	E	E			
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A	PREPARED BY Donald R. Osborne	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Ray Monnin	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, LINEAR, BUS INTERFACE DRIVER CIRCUIT, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 88-05-05	
AMSC N/A	REVISION LEVEL E	SIZE A / CAGE CODE **67268** / **5962-86879**
		SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86879	01	E	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-3182, HI-8382	Bus interface line driver circuit

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V+ minus V- (differential voltage) ..... 40 V dc
V_1 ..... 7 V dc
V_{REF} ..... 6 V dc
Logic input voltage range ..... (GND - 0.3 V) to (V_1 + 0.3 V)
Maximum power dissipation (P_D):
Case E ..... 1.725 W 1/
Case 3 ..... 1.12 W 1/
Junction temperature (T_J) ..... +175°C
Lead temperature (soldering, 10 seconds) ..... +275°C
Storage temperature range ..... -65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):
Case E ..... 86.5°C/W
Case 3 ..... 133.7°C/W

1/ Derate above +25°C, 11.5 mW/°C for case E, and 7.5 mW/°C for case 3.

1.4 Recommended operating conditions. 2/

Supply voltage:

V+ ..... 15 V dc ±10%

V- ..... -15 V dc ±10%

V_1 ..... 5 V dc ±5%

V_{REF} ..... 5 V dc ±5%

Ambient operating temperature range (T_A) ..... -55°C to +125°C

Maximum load:

Data rate at 12.5 KBPS: $R_L = 800\Omega$, $C_L = 30$ nF; $R_L = 400\Omega$, $C_L = 6.9$ nF.

Data rate at 100 KBPS: $R_L = 800\Omega$, $C_L = 4$ nF.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2/ All voltages referenced to GND.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current V+ (operating)	I_{CCOP} (V+)	No load (0-100 k bits/s)	1, 2, 3	01		16	mA
Supply current V- (operating)	I_{CCOP} (V-)	No load (0-100 k bits/s)	1, 2, 3	01		-16	mA
Supply current V_1 (operating)	I_{CCOP} (V_1)	No load (0-100 k bits/s)	1, 2, 3	01		975	µA
Supply current V_{REF} (operating)	I_{CCOP} (V_{REF})	No load (0-100 k bits/s)	1, 2, 3	01		-1.0	mA
Supply current V- (during short circuit test)	I_{SC} (V-)	Short to ground 1/	1, 2, 3	01		-150	mA
Supply current V+ (during short circuit test)	I_{SC} (V+)	Short to ground 1/	1, 2, 3	01		150	mA
Output short circuit current (output high)	I_{OSHC}	Short to ground, V_{min} = 0 V 2/	1, 2, 3	01	-80		mA
Output short circuit current (output low)	I_{OSLC}	Short to ground, V_{min} = 0 V 2/	1, 2, 3	01	+80		mA
Input current (input high)	I_{IH}		1, 2, 3	01		10	µA
Input current (input low)	I_{IL}		1, 2, 3	01		-20	µA
Output voltage high (output to ground)	V_{OH}	No load (0-100 k bits/s)	1, 2, 3	01	$+V_{REF}$ - .25	$+V_{REF}$ + .25	V
Output voltage low (output to ground)	V_{OL}	No load (0-100 k bits/s)	1, 2, 3	01	$-V_{REF}$ - .25	$-V_{REF}$ + .25	V
Output voltage null	V_{NULL}	No load (0-100 k bits/s)	1, 2, 3	01	-250	+250	mV
Input capacitance	C_{IN}	See 4.3.1c, T_A = +25°C	4	01		30	pF
Functional tests		V_{IH} = 2.0 V, V_{IL} = 0.5 V, see 4.3.1d 3/	7, 8	01			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Rise time (A_{OUT}, B_{OUT})	t_r	See figure 4, C_L = 75 pF 3/	9, 10, 11	01	0.9	2.4	µs
Fall time (A_{OUT}, B_{OUT})	t_f	See figure 4, C_L = 75 pF 3/	9, 10, 11	01	0.9	2.4	µs
Propagation delay input to output	t_{PLH}	See figure 4, C_L = 75 pF 3/	9, 10, 11	01		3.3	µs
Propagation delay input to output	t_{PHL}	See figure 4, C_L = 75 pF 3/	9, 10, 11	01		3.3	µs

1/ Not tested, but characterized at initial device design and after major process or design change which affects this parameter.

2/ Interchangeability of force and sense is acceptable.

3/ V+ = 15 V, V- = 15 V, $V_1 = V_{REF}$ = 5.0 V.

Device type	01	
Case outlines	E	3
Terminal number	Terminal symbol	
1	V_{REF}	V_{REF}
2	GND	NC
3	SYNC	GND
4	DATA (A)	SYNC
5	C_A	NC
6	A_{OUT}	DATA (A)
7	-V	NC
8	GND	NC
9	+V	C_A
10	NC	NC
11	B_{OUT}	NC
12	C_B	NC
13	DATA (B)	A_{OUT}
14	CLOCK	-V
15	NC	GND
16	V_1	+V
17	- - -	B_{OUT}
18	- - -	NC
19	- - -	NC
20	- - -	NC
21	- - -	NC
22	- - -	C_B
23	- - -	DATA (B)
24	- - -	NC
25	- - -	CLOCK
26	- - -	NC
27	- - -	NC
28	- - -	V_1

NC = No connection

FIGURE 1. Terminal connections.

SYNC	CLOCK	DATA (A)	DATA (B)	A_{OUT}	B_{OUT}	COMMENTS
X	L	X	X	0 V	0 V	NULL
L	X	X	X	0 V	0 V	NULL
H	H	L	L	0 V	0 V	NULL
H	H	L	H	$-V_{REF}$	$+V_{REF}$	LOW
H	H	H	L	$+V_{REF}$	$-V_{REF}$	HIGH
H	H	H	H	0 V	0 V	NULL

FIGURE 2. Truth table.

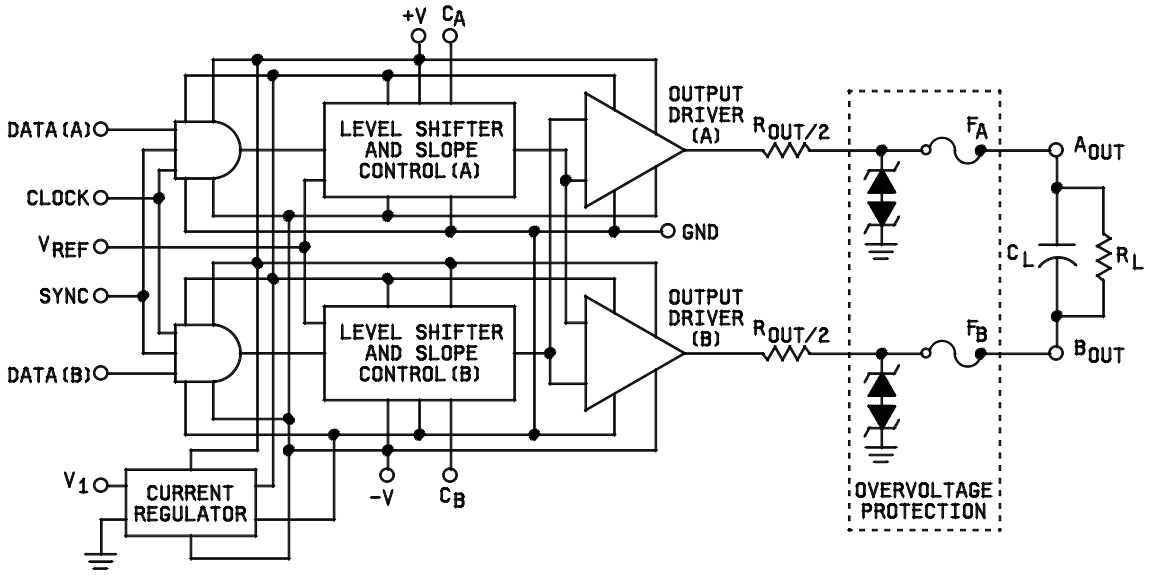
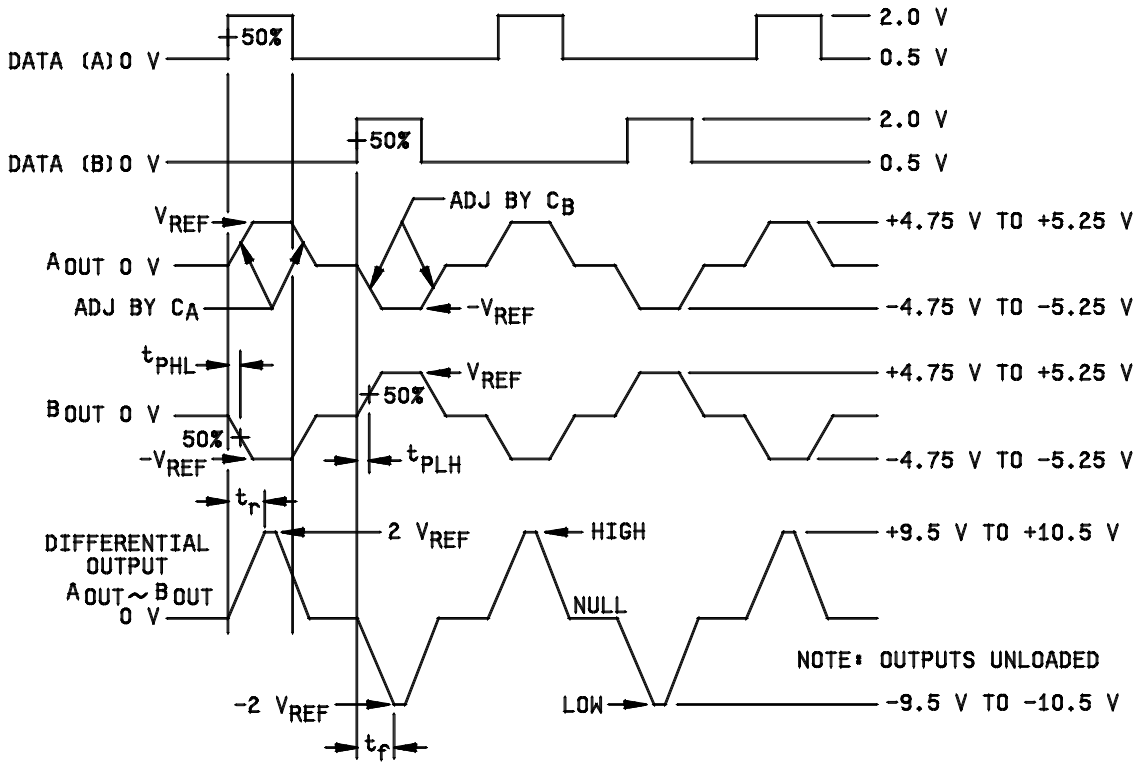


FIGURE 3. Logic diagram.



NOTE:

t_r measured 50 percent to 90 percent times two.

t_f measured 50 percent to 90 percent times two.

V_{IH} = 2.0 V, V_{OL} = -4.75 V to -5.25 V

V_{IL} = 0.5 V, V_{OH} = 4.75 V to 5.25 V

FIGURE 4. Switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is 15 devices, all input and output terminals tested, and no failures.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-10-09

Approved sources of supply for SMD 5962-86879 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8687901EA	34371	HS1-3182/883
	44270	HI-8382CM-03
	3/	HI-8382CM-02
	3/	RM3182S/883B
5962-86879013A	3/	HI-8382SM-02
	3/	HS4-3182/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035-6803
44270	Holt Integrated Circuits, Inc. 23351 Madero Mission Viejo, CA 92691-2730

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.