

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change ripple carry truth table. Code ident. no. changed to 67268.	87-07-01	M. A. Frye
B	Split V _{IL} into temperatures. Change propagation delays. Add footnotes to table I. Add figures 4 and 5. Change footnote 1/ of 1.3. Change in table II. Editorial changes throughout.	88-05-12	M. A. Frye
C	Changes in accordance with NOR 5962-R239-92.	92-07-10	Monica L. Poelking
D	Changes in accordance with NOR 5962-R135-96.	96-06-05	Monica L. Poelking
E	Redraw with changes. Update to current requirements. Editorial changes throughout. - gap	05-12-06	Raymond Monnin
F	Update drawing as part of 5 year review. - jt	11-02-02	C. SAFFLE

CURRENT CAGE CODE 67268

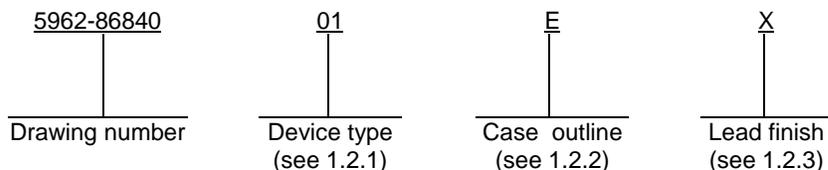
The original first page of this drawing has been replaced.

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REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13						
PMIC N/A	PREPARED BY David W. Queenen				<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil</p>															
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY David H. Johnson																			
	APPROVED BY Michael A. Frye				<p align="center">MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED LOW-POWER SCHOTTKY TTL, COUNTER, MONOLITHIC SILICON</p>															
	DRAWING APPROVAL DATE 86-11-10																			
	REVISION LEVEL F				SIZE A	CAGE CODE 14933	5962-86840													
SHEET 1 OF 13																				

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ALS191A	Synchronous 4-bit up/down binary counter

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat package
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc minimum to 7.0 V dc maximum
Input voltage range	-1.5 V dc at -18 mA to 7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P _D) ^{1/}	121 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ _{JC})	See MIL-STD-1835
Junction temperature (T _J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V _{CC})	4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V _{IH})	2.0 V dc
Maximum low level input voltage (V _{IL}):	
V _{IL} = +125°C	0.7 V dc
V _{IL} = +25°C	0.8 V dc
V _{IL} = -55°C	0.8 V dc
Case operating temperature range (T _C)	-55°C to +125°C
Pulse width:	
CLK high or low	20 ns minimum
LOAD low	25 ns minimum

^{1/} Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short circuit test; e.g., I_o.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Timing sequence. The timing sequence shall be as specified on figure 4.

3.2.6 Switching circuit and waveforms. The switching circuit and waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime 's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -0.4 mA V _{IH} = 2.0 V <u>2/</u>	V _{IL} = 0.7 V	2	2.5		V
			V _{IL} = 0.8 V	1, 3			
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 4.0 mA V _{IH} = 2.0 V <u>2/</u>	V _{IL} = 0.7 V	2		0.4	V
			V _{IL} = 0.8 V	1, 3			
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V I _{IN} = -18 mA		1, 2, 3		-1.5	V
Low level input current at <u>CTEN</u> , CLK	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.4 V, Unused inputs ≥ 4.5 V		1, 2, 3		-0.2	mA
Low level input current at all other inputs	I _{IL2}	V _{CC} = 5.5 V, V _{IN} = 0.4 V, Unused inputs ≥ 4.5 V		1, 2, 3		-0.2	mA
High level input current	I _{IH1}	V _{CC} = 5.5 V, V _{IN} = 2.7 V, All other inputs = 0.0 V		1, 2, 3		20	μA
	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 7.0 V All other inputs = 0.0 V		1, 2, 3		0.1	mA
Output current	I _O	V _{CC} = 5.5 V V _{OUT} = 2.25 V <u>3/</u>		1, 2, 3	-20	-112	mA
Supply current	I _{CC}	V _{CC} = 5.5 V, All inputs ≤ 0.4 V		1, 2, 3		22	mA
Functional tests		See 4.3.1c <u>4/</u>		7, 8			

See footnotes at end of table.

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Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Maximum clock frequency	f _{MAX}	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω 5/ See figures 4 and 5	9, 10, 11	20		MHz
Propagation delay time, LOAD to any Q	t _{PLH1}		9, 10, 11	7	34	ns
	t _{PHL1}		9, 10, 11	8	31	ns
Propagation delay time, A, B, C, D to any Q	t _{PLH2}		9, 10, 11	3	21	ns
	t _{PHL2}		9, 10, 11	4	22	ns
Propagation delay time, CLK to RCO	t _{PLH3}		9, 10, 11	5	24	ns
	t _{PHL3}		9, 10, 11	5	24	ns
Propagation delay time, CLK to any Q	t _{PLH4}		9, 10, 11	3	20	ns
	t _{PHL4}		9, 10, 11	3	21	ns
Propagation delay time, CLK to MAX/MIN	t _{PLH5}		9, 10, 11	8	34	ns
	t _{PHL5}		9, 10, 11	8	34	ns
Propagation delay time, D/Ū to RCO	t _{PLH6}		9, 10, 11	8	42	ns
	t _{PHL6}		9, 10, 11	10	33	ns
Propagation delay time, D/Ū to MAX/MIN	t _{PLH7}		9, 10, 11	8	30	ns
	t _{PHL7}		9, 10, 11	8	30	ns
Propagation delay time, CTEN to RCO	t _{PLH8}		9, 10, 11	4	18	ns
	t _{PHL8}	9, 10, 11	4	21	ns	

- 1/ Unused inputs that do not directly control the pin under test must be put ≥ 2.5 V or ≤ 0.4 V. The inputs shall not exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.
- 2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or V_{IH} minimum input.
- 3/ The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit output current, I_{OS}. Not more than one output will be tested at a time and the duration of the test condition shall not exceed 1 second.
- 4/ Functional tests shall be conducted at input test conditions of GND ≤ V_{IL} ≤ V_{OL} and V_{OH} ≤ V_{IH} ≤ V_{CC}.
- 5/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V.

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Case outlines	E and F	2
Terminal number	Terminal symbol	
1	B	NC
2	Q _B	B
3	Q _A	Q _B
4	\overline{CTEN}	Q _A
5	D/ \overline{U}	\overline{CTEN}
6	Q _C	NC
7	Q _D	D/ \overline{U}
8	GND	Q _C
9	D	Q _D
10	C	GND
11	\overline{LOAD}	NC
12	MAX/MIN	D
13	\overline{RCO}	C
14	CLK	\overline{LOAD}
15	A	MAX/MIN
16	V _{CC}	NC
17	---	\overline{RCO}
18	---	CLK
19	---	A
20	---	V _{CC}

FIGURE 1. Terminal connections.

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Mode select

Inputs				Mode
$\overline{\text{LOAD}}$	$\overline{\text{CTEN}}$	D/ $\overline{\text{U}}$	CLK	
H	L	L	$\underline{\hspace{0.5cm}}\overline{\hspace{0.5cm}}$	Count up
H	L	H	$\underline{\hspace{0.5cm}}\overline{\hspace{0.5cm}}$	Count down
L	X	X	X	Preset (asyn)
H	H	X	X	No change (hold)

Ripple carry

Inputs		Outputs		Count status
$\overline{\text{CTEN}}$	CLK	MAX/MIN	$\overline{\text{RCO}}$	
L	$\overline{\hspace{0.5cm}}\underline{\hspace{0.5cm}}$	$\underline{\hspace{0.5cm}}\overline{\hspace{0.5cm}}$	$\overline{\hspace{0.5cm}}\underline{\hspace{0.5cm}}$	Either 15 while counting up or 0 while counting down.
H	X	X	H	All conditions (hold)
X	X	L	H	All conditions other than 15 while counting up or 0 when counting down.

L = Low voltage level
H = High voltage level
X = Don't care
 $\underline{\hspace{0.5cm}}\overline{\hspace{0.5cm}}$ = Low-to-high clock transition
 $\underline{\hspace{0.5cm}}\overline{\hspace{0.5cm}}\underline{\hspace{0.5cm}}$ = One high level pulse
 $\overline{\hspace{0.5cm}}\underline{\hspace{0.5cm}}\overline{\hspace{0.5cm}}$ = One low level pulse

FIGURE 2. Truth tables.

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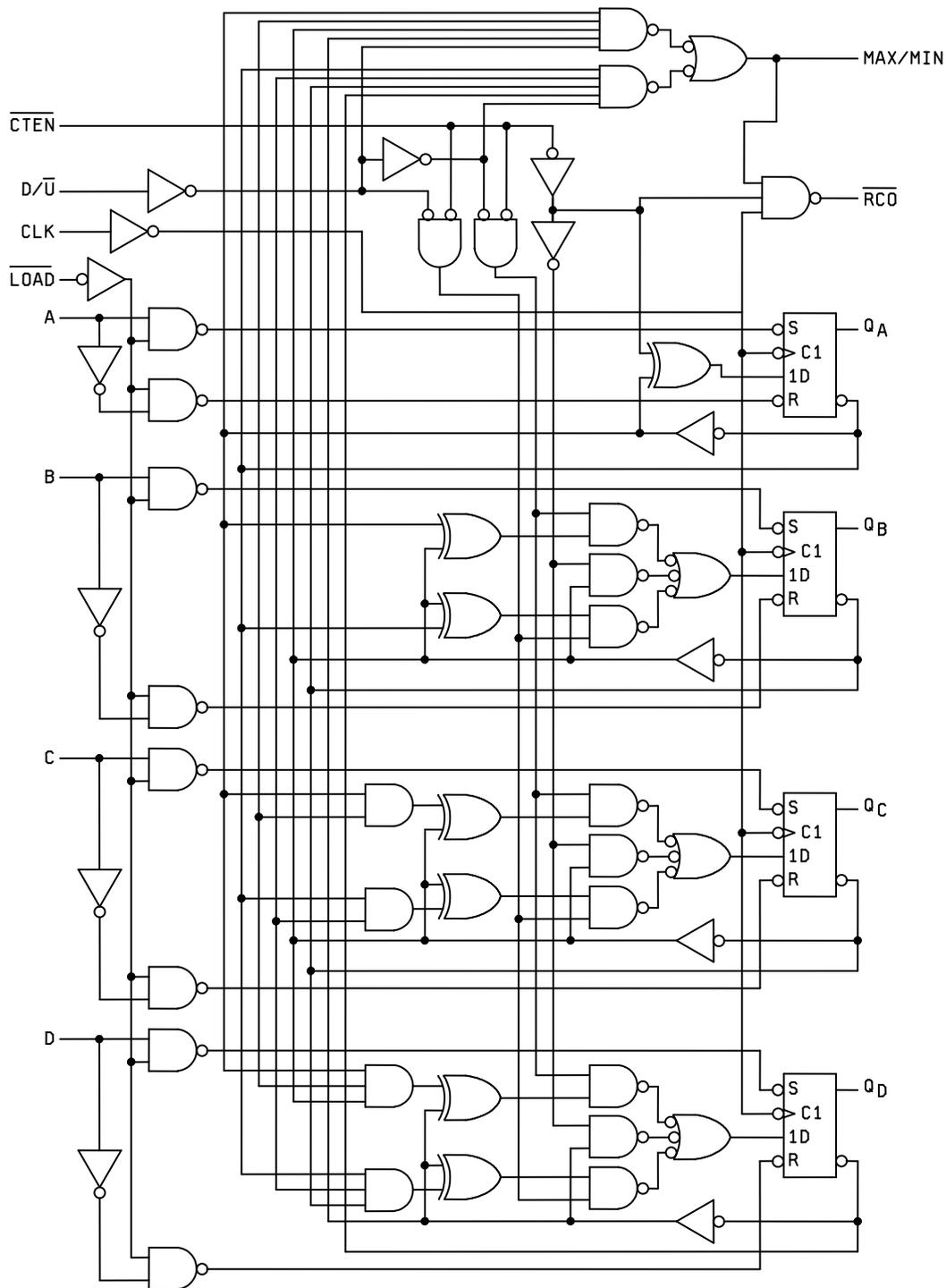


FIGURE 3. Logic diagram.

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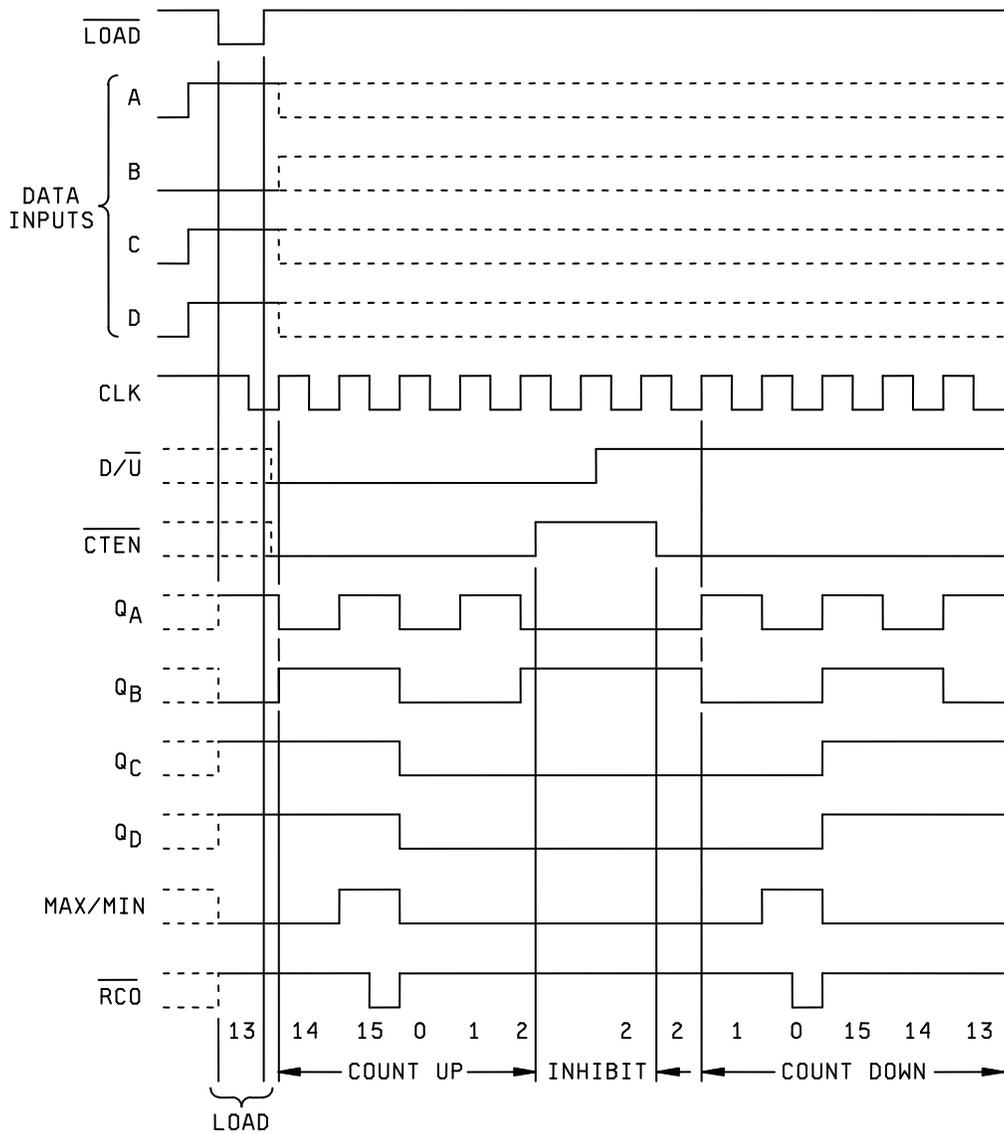


FIGURE 4. Timing sequence.

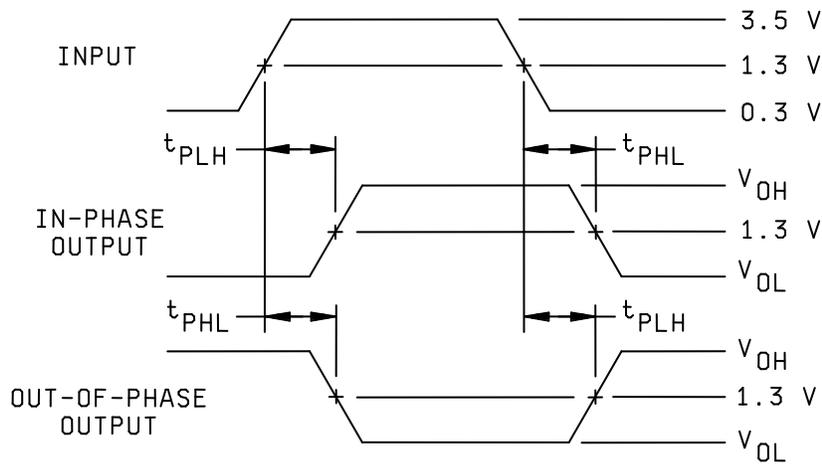
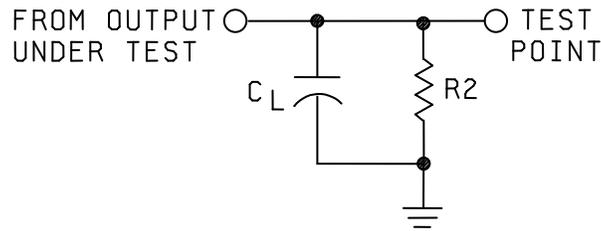
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NOTES:

1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics: $PRR \leq 10\text{MHz}$, duty cycle = 50%, $t_r = t_f = 3 \text{ ns} \pm 1 \text{ ns}$.
3. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Switching circuit and waveforms.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 shall include verification of the truth table.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0547.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-02-02

Approved sources of supply for SMD 5962-86840 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.dsccl.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8684001EA	01295	SNJ54ALS191AJ
5962-8684001FA	01295	SNJ54ALS191AW
5962-86840012A	01295	SNJ54ALS191AFK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

Vendor name
and address

01295

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
PO Box 660199
Dallas, TX 75243

POC U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

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