| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add vendor 27014 for device types 01EX and 012X. Recommended operating conditions, change pulse width ($t_W$) at $V_{CC}$ = 6.0 V and also changed maximum frequency ($f_{MAX}$) at $V_{CC}$ = 2.0 V. | 87-03-04 | N. A. Hauck |
| B | Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. – LTG | 03-05-15 | Thomas M. Hess |
| C | Add class V criteria. Add test circuit to figure 4. Add table III, delta limits. Editorial changes throughout. – jak | 03-08-22 | Thomas M. Hess |
| D | Update boilerplate to MIL-PRF-38535 requirements. - LTG | 08-09-03 | Thomas M. Hess |
| E | Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG | 15-02-26 | Thomas M. Hess |
| F | Update boilerplate to MIL-PRF-38535 requirements. - DRH | 21-10-05 | Muhammad A. Akbar |

**CURRENT CAGE CODE 67268**

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | F | | | | | | | | | | | | | | | | | | | |
| SHEET | 15 | | | | | | | | | | | | | | | | | | | |

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV STATUS | REV | F | F | F | F | F | F | F | F | F | F | F | F | F | F | F |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |

PMIC N/A

PREPARED BY
Greg A. Pitz

CHECKED BY
D. A. DiCenzo

APPROVED BY
Robert P. Evans

DRAWING APPROVAL DATE
86-09-19

REVISION LEVEL
F

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**https://www.dla.mil/LandandMaritime**

MICROCIRCUIT, DIGITAL, HIGH SPEED CMOS, 8-BIT SHIFT REGISTER, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **14933** | **5962-86816** |

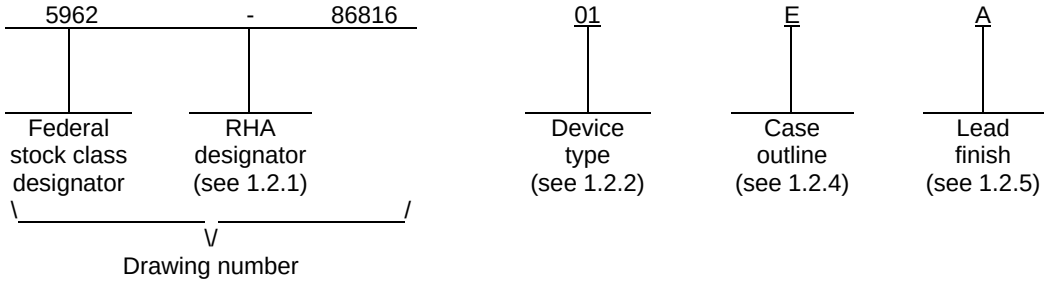
SHEET 1 OF 15

1. SCOPE

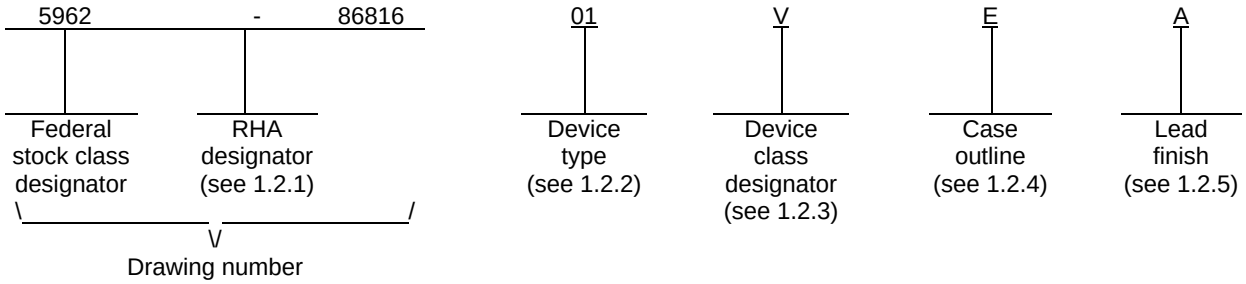
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device class M and Q:




For device class V:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54HC595 | Shift register, 8-bit with output latches |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| E | GDIP1-T16 or CDIP2-T16 | 16 | Dual-in-line |
| F | GDFP2-F16 or CDFP3-F16 | 16 | Flat pack |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range ($V_{CC}$) ..... -0.5 V dc to +7.0 V dc
DC input voltage range ($V_{IN}$) ..... -0.5 V dc to $V_{CC}$ + 0.5 V dc
DC output voltage range ($V_{OUT}$) ..... -0.5 V dc to $V_{CC}$ + 0.5 V dc
Clamp diode current ..... ±20 mA
DC output current (per pin) (SQH) ..... ±25 mA
DC output current (per pin) (QA –QH) ..... ±35 mA
$V_{CC}$ or GND current (per pin) ..... ±70 mA
Storage temperature range ($T_{STG}$) ..... -65°C to +150°C
Maximum power dissipation ($P_D$) ..... 500 mW 3/
Lead temperature (soldering 10 seconds) ..... 260°C
Thermal resistance, junction-to-case ($\theta_{JC}$) ..... See MIL-STD-1835
Junction temperature ($T_J$) ..... 175°C

1.4 Recommended operating conditions. 2/

Supply voltage range ($V_{CC}$) ..... +2.0 V dc to +6.0 V dc
Case operating temperature range ($T_C$) ..... -55°C to +125°C
Input rise or fall time ($t_r$, $t_f$ ):
$V_{CC}$ = 2.0 V ..... 0 to 1000 ns
$V_{CC}$ = 4.5 V ..... 0 to 500 ns
$V_{CC}$ = 6.0 V ..... 0 to 400 ns

Minimum setup time, serial data to shift clock ($t_S$):
$T_C$ = +25°C:
$V_{CC}$ = 2.0 V ..... 100 ns
$V_{CC}$ = 4.5 V ..... 20 ns
$V_{CC}$ = 6.0 V ..... 17 ns
$T_C$ = -55°C to +125°C:
$V_{CC}$ = 2.0 V ..... 150 ns
$V_{CC}$ = 4.5 V ..... 30 ns
$V_{CC}$ = 6.0 V ..... 26 ns

Minimum reset or latch clock or shift clock pulse width ($t_W$):
$T_C$ = +25°C:
$V_{CC}$ = 2.0 V ..... 80 ns
$V_{CC}$ = 4.5 V ..... 16 ns
$V_{CC}$ = 6.0 V ..... 22 ns
$T_C$ = -55°C to +125°C:
$V_{CC}$ = 2.0 V ..... 120 ns
$V_{CC}$ = 4.5 V ..... 24 ns
$V_{CC}$ = 6.0 V ..... 20 ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to ground.
3/ For $T_C$ = +100°C to +125°C, derate linearly at 12 Mw/°C.

1.4 Recommended operating conditions - Continued. 2/

Minimum hold time, shift clock to serial data ($t_H$):
$T_C$ = +25°C:
$V_{CC}$ = 2.0 V ..... 25 ns
$V_{CC}$ = 4.5 V ..... 5 ns
$V_{CC}$ = 6.0 V ..... 5 ns
$T_C$ = -55°C to +125°C:
$V_{CC}$ = 2.0 V ..... 40 ns
$V_{CC}$ = 4.5 V ..... 8 ns
$V_{CC}$ = 6.0 V ..... 7 ns

Maximum clock frequency ($f_{MAX}$):
$T_C$ = +25°C:
$V_{CC}$ = 2.0 V ..... 5 MHz
$V_{CC}$ = 4.5 V ..... 27 MHz
$V_{CC}$ = 6.0 V ..... 32 MHz
$T_C$ = -55°C to +125°C:
$V_{CC}$ = 2.0 V ..... 3.6 MHz
$V_{CC}$ = 4.5 V ..... 18 MHz
$V_{CC}$ = 6.0 V ..... 21 MHz

Minimum setup time, shift clock to latch clock ($t_S$):
$T_C$ = +25°C:
$V_{CC}$ = 2.0 V ..... 100 ns
$V_{CC}$ = 4.5 V ..... 20 ns
$V_{CC}$ = 6.0 V ..... 17 ns
$T_C$ = -55°C to +125°C:
$V_{CC}$ = 2.0 V ..... 150 ns
$V_{CC}$ = 4.5 V ..... 30 ns
$V_{CC}$ = 6.0 V ..... 26 ns

Minimum recovery time, reset inactive to shift clock ($t_{REC}$):
$T_C$ = +25°C:
$V_{CC}$ = 2.0 V ..... 50 ns
$V_{CC}$ = 4.5 V ..... 10 ns
$V_{CC}$ = 6.0 V ..... 9 ns
$T_C$ = -55°C to +125°C:
$V_{CC}$ = 2.0 V ..... 75 ns
$V_{CC}$ = 4.5 V ..... 15 ns
$V_{CC}$ = 6.0 V ..... 13 ns

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD7 - Standard for Description of 54/74HCXXXXX and 54/74HCTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at https://www.jedec.org/.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 40 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

| Test | Symbol | Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified | | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| High level output voltage (SQH) | $V_{OH1}$ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH} = -20\ \mu A$ | $V_{CC} = 2.0$ V | All | 1, 2, 3 | 1.9 | | V |
| | | | $V_{CC} = 4.5$ V | | | 4.4 | | |
| | | | $V_{CC} = 6.0$ V | | | 5.9 | | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH} = -4.0$ mA | $V_{CC} = 4.5$ V | | | 3.7 | | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH} = -5.2$ mA | $V_{CC} = 6.0$ V | | | 5.2 | | |
| Low level output voltage (SQH) | $V_{OL1}$ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL} = +20\ \mu A$ | $V_{CC} = 2.0$ V | All | 1, 2, 3 | | 0.1 | V |
| | | | $V_{CC} = 4.5$ V | | | | 0.1 | |
| | | | $V_{CC} = 6.0$ V | | | | 0.1 | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL} = +4.0$ mA | $V_{CC} = 4.5$ V | | | | 0.4 | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL} = +5.2$ mA | $V_{CC} = 6.0$ V | | | | 0.4 | |
| High level output voltage (QA – QH) | $V_{OH2}$ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH} = -20\ \mu A$ | $V_{CC} = 2.0$ V | All | 1, 2, 3 | 1.9 | | V |
| | | | $V_{CC} = 4.5$ V | | | 4.4 | | |
| | | | $V_{CC} = 6.0$ V | | | 5.9 | | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH} = -6.0$ mA | $V_{CC} = 4.5$ V | | | 3.7 | | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH} = -7.8$ mA | $V_{CC} = 6.0$ V | | | 5.2 | | |
| Low level output voltage (QA – QH) | $V_{OL2}$ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL} = +20\ \mu A$ | $V_{CC} = 2.0$ V | All | 1, 2, 3 | | 0.1 | V |
| | | | $V_{CC} = 4.5$ V | | | | 0.1 | |
| | | | $V_{CC} = 6.0$ V | | | | 0.1 | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL} = +6.0$ mA | $V_{CC} = 4.5$ V | | | | 0.4 | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL} = +7.8$ mA | $V_{CC} = 6.0$ V | | | | 0.4 | |
| High level input voltage 2/ | $V_{IH}$ | | $V_{CC} = 2.0$ V | All | 1, 2, 3 | 1.5 | | V |
| | | | $V_{CC} = 4.5$ V | | | 3.15 | | |
| | | | $V_{CC} = 6.0$ V | | | 4.2 | | |
| Low level input voltage 2/ | $V_{IL}$ | | $V_{CC} = 2.0$ V | All | 1, 2, 3 | | 0.3 | V |
| | | | $V_{CC} = 4.5$ V | | | | 0.9 | |
| | | | $V_{CC} = 6.0$ V | | | | 1.2 | |
| Quiescent current | $I_{CC}$ | $V_{CC} = 6.0$ V, $V_{IN} = V_{CC}$ or GND | | All | 1, 2, 3 | | 160 | µA |
| Input leakage current | $I_{IN}$ | $V_{CC} = 6.0$ V, $V_{IN} = V_{CC}$ or GND | | All | 1, 2, 3 | | ±1.0 | µA |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified | | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Three-state output current | $I_{OZ}$ | $V_O = V_{CC}$ or GND, $V_{IN} = V_{IH}$ or $V_{IL}$ | | All | 1, 2, 3 | | ±10.0 | µA |
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0.0 V, $T_C$ = 25°C See 4.4.1c | | All | 4 | | 10.0 | pF |
| Output capacitance | $C_{OUT}$ | $V_O$ = 0.0 V, $T_C$ = 25°C See 4.4.1c | | All | 4 | | 20.0 | pF |
| Functional tests | | See 4.4.1b | | All | 7 | L | H | |
| Propagation delay time, shift clock to SQH 3/ | $t_{PHL1}$, $t_{PLH1}$ | $C_L$ = 50 pF ±10% See figure 4 | $V_{CC}$ = 2.0 V | All | 9 | | 210 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 42 | |
| | | | $V_{CC}$ = 6.0 V | | | | 36 | |
| | | | $V_{CC}$ = 2.0 V | All | 10, 11 | | 315 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 63 | |
| | | | $V_{CC}$ = 6.0 V | | | | 54 | |
| Propagation delay time, reset to SQH 3/ | $t_{PHL2}$ | $C_L$ = 50 pF ±10% See figure 4 | $V_{CC}$ = 2.0 V | All | 9 | | 175 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 35 | |
| | | | $V_{CC}$ = 6.0 V | | | | 30 | |
| | | | $V_{CC}$ = 2.0 V | All | 10, 11 | | 265 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 53 | |
| | | | $V_{CC}$ = 6.0 V | | | | 45 | |
| Propagation delay time, latch clock to Q 3/ | $t_{PHL3}$, $t_{PLH3}$ | $C_L$ = 50 pF ±10% See figure 4 | $V_{CC}$ = 2.0 V | All | 9 | | 175 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 35 | |
| | | | $V_{CC}$ = 6.0 V | | | | 30 | |
| | | | $V_{CC}$ = 2.0 V | All | 10, 11 | | 265 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 53 | |
| | | | $V_{CC}$ = 6.0 V | | | | 45 | |
| Propagation delay time, output enable to Q 3/ | $t_{PZL}$, $t_{PZH}$ | $C_L$ = 50 pF ±10% See figure 4 | $V_{CC}$ = 2.0 V | All | 9 | | 150 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 30 | |
| | | | $V_{CC}$ = 6.0 V | | | | 26 | |
| | | | $V_{CC}$ = 2.0 V | All | 10, 11 | | 225 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 45 | |
| | | | $V_{CC}$ = 6.0 V | | | | 38 | |
| Propagation delay time, output disable to Q 3/ | $t_{PLZ}$, $t_{PHZ}$ | $C_L$ = 50 pF ±10% See figure 4 | $V_{CC}$ = 2.0 V | All | 9 | | 200 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 40 | |
| | | | $V_{CC}$ = 6.0 V | | | | 34 | |
| | | | $V_{CC}$ = 2.0 V | All | 10, 11 | | 300 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 60 | |
| | | | $V_{CC}$ = 6.0 V | | | | 51 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Test conditions 1/ $-55°C \le T_C \le +125°$ unless otherwise specified | | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Transition time (SQH) 4/ | $t_{TLH1}$, $t_{THL1}$ | $C_L$ = 50 pF ±10% See figure 4 | $V_{CC}$ = 2.0 V | All | 9 | | 75 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 15 | |
| | | | $V_{CC}$ = 6.0 V | | | | 13 | |
| | | | $V_{CC}$ = 2.0 V | All | 10, 11 | | 110 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 22 | |
| | | | $V_{CC}$ = 6.0 V | | | | 19 | |
| Transition time (QA-QH) 4/ | $t_{TLH2}$, $t_{THL2}$ | $C_L$ = 50 pF ±10% See figure 4 | $V_{CC}$ = 2.0 V | All | 9 | | 60 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 12 | |
| | | | $V_{CC}$ = 6.0 V | | | | 10 | |
| | | | $V_{CC}$ = 2.0 V | All | 10, 11 | | 90 | ns |
| | | | $V_{CC}$ = 4.5 V | | | | 18 | |
| | | | $V_{CC}$ = 6.0 V | | | | 15 | |

1/ For a power supply of 5.0 V ±10%, the worst case output voltages ($V_{OH}$ and $V_{OL}$) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5 V and 4.5 V, respectively. (The $V_{IH}$ value at 5.5 V is 3.85 V). The worst case leakage currents ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0 V values should be used. Power dissipation capacitance ($C_{PD}$), typically 300 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}{}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

2/ Tests not required if applied as a forcing function for $V_{OH}$ and $V_{OL}$.

3/ AC testing at $V_{CC}$ = 2.0 V and $V_{CC}$ = 6.0 V shall be guaranteed, if not tested, to the specified parameters.

4/ Transition times, if not tested, shall be guaranteed to the specified parameters.

| Device type | 01 | |
|---|---|---|
| Case outlines | E and F | 2 |
| Terminal numbers | Terminal symbols | Terminal symbols |
| 1 | QB | NC |
| 2 | QC | QB |
| 3 | QD | QC |
| 4 | QE | QD |
| 5 | QF | QE |
| 6 | QG | NC |
| 7 | QH | QF |
| 8 | GND | QG |
| 9 | SQH | QH |
| 10 | RESET | GND |
| 11 | SHIFT CLOCK | NC |
| 12 | LATCH CLOCK | SQH |
| 13 | OUTPUT ENABLE | RESET |
| 14 | A | SHIFT CLOCK |
| 15 | QA | LATCH CLOCK |
| 16 | $V_{CC}$ | NC |
| 17 | --- | OUTPUT ENABLE |
| 18 | --- | A |
| 19 | --- | QA |
| 20 | --- | $V_{CC}$ |

NC = No internal connection

FIGURE 1. Terminal connections.

| Inputs | | | | | Resulting Function |
|---|---|---|---|---|---|
| Reset | A | Shift Clock | Latch Clock | Output Enable | |
| L | X | X | X | X | Shift register contents are cleared. |
| H | L | ↑ | X | X | A low logic level is shifted into shift register. |
| H | H | ↑ | X | X | A high logic level is shifted into shift register. |
| H | X | ↓ | X | X | Shift register remains unchanged. |
| H | X | L | ↑ | X | Shift register data stored in the 8-bit latch. |
| H | X | L | ↓ | X | Data latch remains unchanged. |
| H | X | L | L | L | Latch Outputs, QA – QH are enabled. |
| H | X | L | L | H | Outputs QA – QH are in the high impedance state. |

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Transition from low to high level
↓ = Transition from high to low level

FIGURE 2. Truth table.

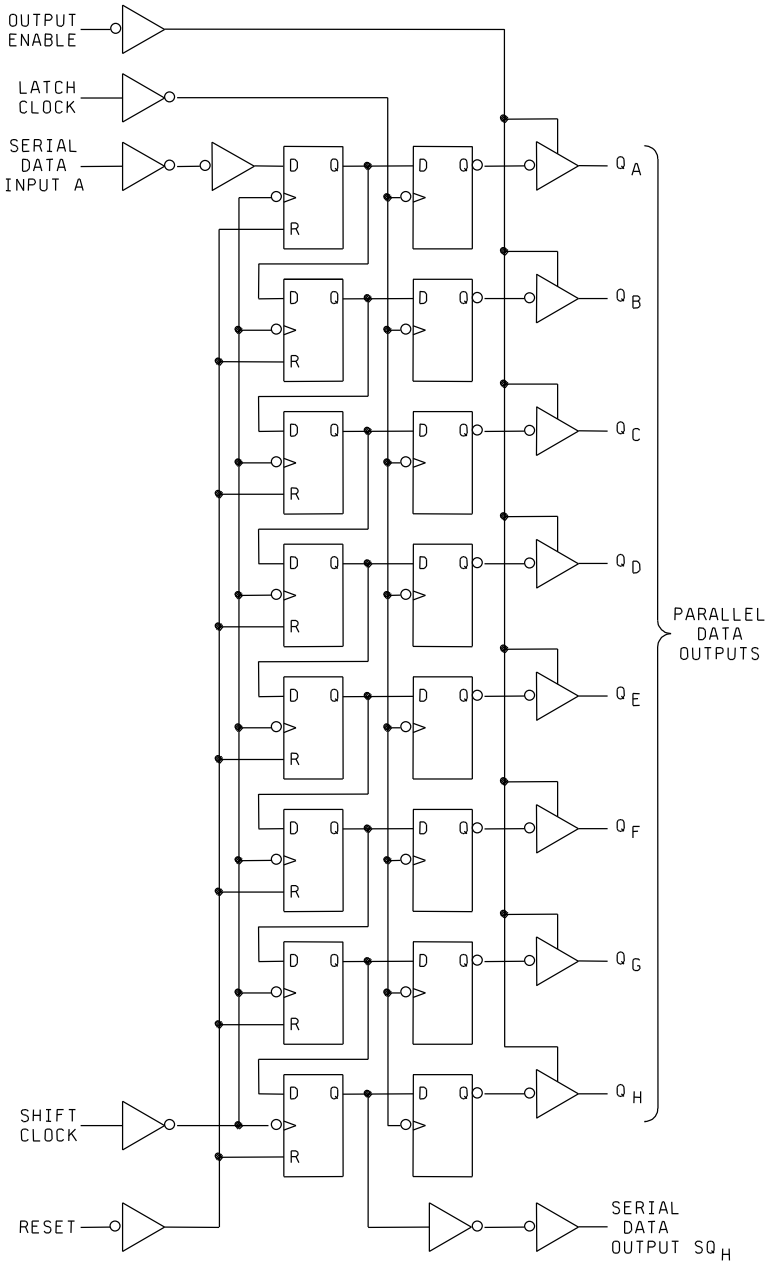
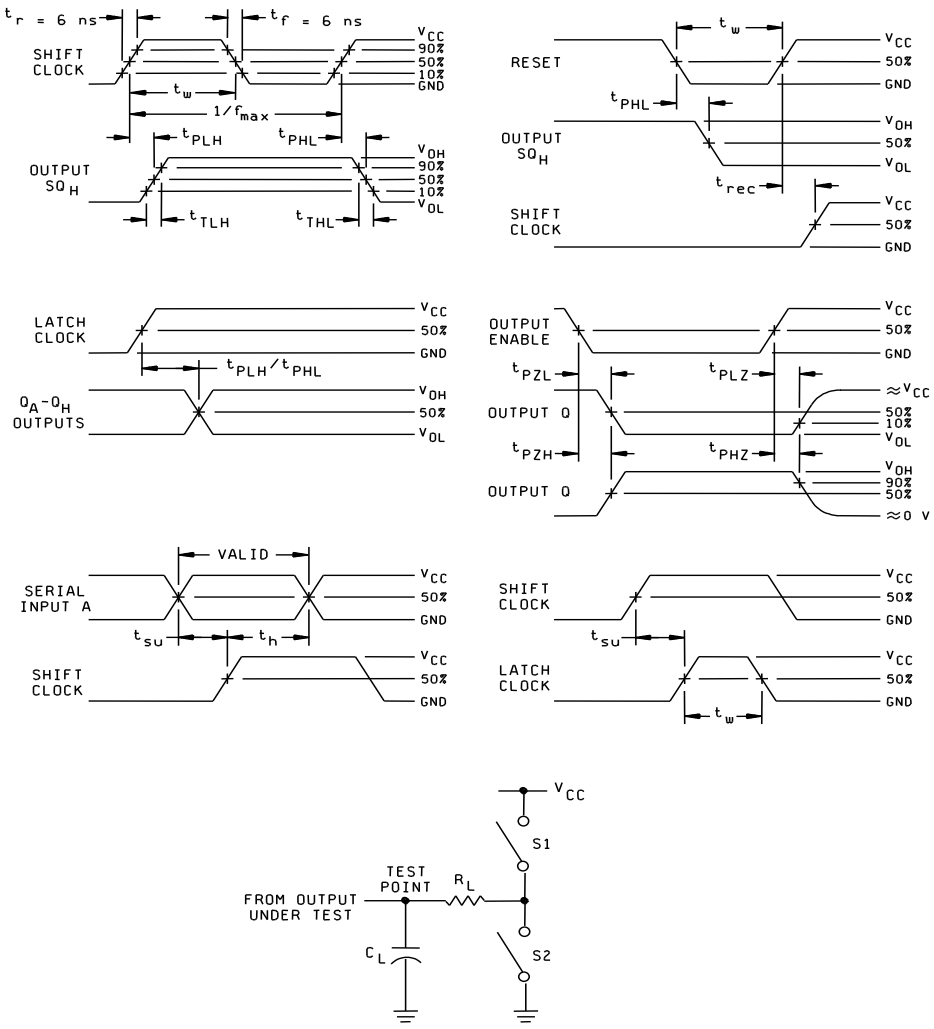



FIGURE 3. Logic diagram.




NOTES:

1. $t_{PLH}$ and $t_{PHL}$: S1 and S2 = open.
   $t_{TLH}$ and $t_{THL}$: S1 and S2 = open.
   $t_{PZH}$ and $t_{PHZ}$: S1 = open and S2 = closed.
   $t_{PZL}$ and $t_{PLZ}$: S1 = closed and S2 = open.
2. $R_L$ = 1 kΩ.
3. $C_L$ includes probe and test fixture capacitance.
4. The $t_{PZL}$ and $t_{PLZ}$ reference waveform is for the output under test with internal conditions such that the output is at $V_{OL}$ except when disabled by the output enable control. The $t_{PZH}$ and $t_{PHZ}$ reference waveform is for the output under test with internal conditions such that the output is at $V_{OH}$ except when disabled by the output enable control.
5. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50Ω, $t_r$ = 6.0 ns, $t_f$ = 6.0 ns.
6. The outputs are measured one at a time with one input transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroup 7 test shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. $C_{IN}$ and $C_{OUT}$ measurements shall be measured for the initial qualification and after process or design changes which may affect input capacitance. $C_{IN}$ and $C_{OUT}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. For $C_{IN}$ and $C_{OUT}$, test all applicable pins on five devices with zero failures.

TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | - - - | 1 |
| Final electrical parameters (see 4.2) | 1, 2, 9 1/ | 1/ 1, 2, 3, 7, 8, 9, 10, 11 | 2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (see 4.4) | 4/ 1, 2, 3, 4, 7, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 3/ 1, 2, 3, 7,8, 9, 10, 11 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7 and deltas.
3/ Delta limits, as specified in table III, shall be required where specified and the delta limits shall be completed with reference to the zero hour electrical parameters.
4/ Subgroups 10, and 11, if not tested, shall be guaranteed to the specified limits in table I.

TABLE III. Burn-in and operating life test delta parameters (+25°C).

| Parameter 1/ | Symbol | Delta limits |
|---|---|---|
| Quiescent supply current | $I_{CC}$ | ±120 nA |
| Input current low level | $I_{IL}$ | ±20 nA |
| Input current high level | $I_{IH}$ | ±20 nA |
| Output voltage low level ($I_{OL}$ = 6 mA, $V_{CC}$ = 4.5 V) | $V_{OL}$ | ±0.026 V |
| Output voltage high level ($I_{OH}$ = -6 mA, $V_{CC}$ = 4.5 V) | $V_{OH}$ | ±0.20V |

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.
b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-10-05

Approved sources of supply for SMD 5962-86816 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8681601EA | 01295 | SNJ54HC595J |
| 5962-86816012A | 01295 | SNJ54HC595FK |
| 5962-8681601VEA | 01295 | SNV54HC595J |
| 5962-8681601VFA | 01295 | SNV54HC595W |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments Incorporated<br>Semiconductor Group<br>8505 Forest Ln.<br>P.O. Box 660199<br>Dallas, TX 75243 |