

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02, generic 1847. Add two packages, F-5 and C-2. Make changes to paragraphs 1.2.1, 1.2.2, 6.4, table I, and figures 1 and 2. Change drawing CAGE code to 67268	89-03-22	M. A. FRYE
B	TABLE I. Short circuit current test. Under the conditions column, add the following sentence; "Both negative and positive currents are considered to decrease towards 0". Under the minimum limits column, delete "-1 mA dc" and substitute "-10 mA dc". Under the maximum limits column, delete "-10 mA" entirely. TABLE I. Shutdown terminal section. Threshold voltage test. Under the conditions column, add the following condition: "RL(CUR LIM/SS PIN) = 15 kΩ at 2 V or equivalent." Changes in accordance with NOR 5962-R080-94.	94-06-24	M. A. FRYE
C	Make changes to latching and nonlatching current test in table I. Update boilerplate. Add class V for vendor CAGE 01295. Redrawn. -rrp	00-12-01	R. MONNIN
D	Drawing updated to reflect current requirements. - ro	03-03-04	R. MONNIN
E	Add device type 03. -rrp	08-12-15	R. HEBER
F	Make change to the Sync input current (I _{SYNC}) test condition from "sync voltage = 5.25 V" to "sync voltage = 3.9 V". - ro	10-10-20	C. SAFFLE
G	Update document paragraphs to current MIL-PRF-38535 requirements. - ro	14-03-10	C. SAFFLE
H	Add paragraph 3.1.1 and Appendix A for microcircuit die. - ro	15-10-16	C. SAFFLE
J	Add radiation requirements to device type 03. - ro	17-01-27	C. SAFFLE
K	Drawing updated to reflect current MIL-PRF-38535 requirements. -rrp	23-04-26	J. ESCHMEYER



CURRENT CAGE CODE 67268

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV	K	K																				
SHEET	23	24																				
REV	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

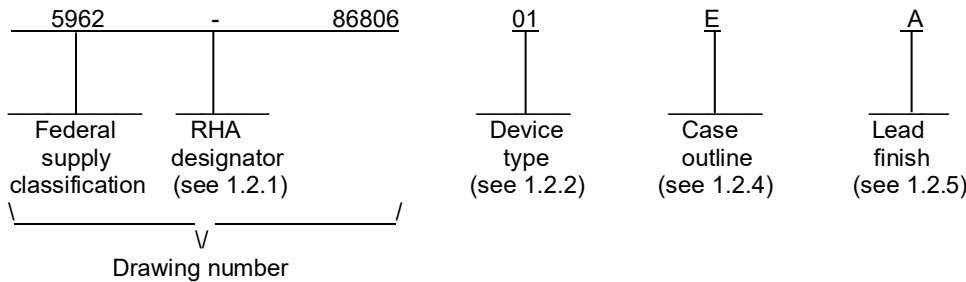
PMIC N/A		PREPARED BY DONALD R. OSBORNE		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime MICROCIRCUIT, LINEAR, CURRENT MODE PULSE WIDTH MODULATOR (PWM), MONOLITHIC SILICON		
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE		CHECKED BY D. A. DICENZO				
		APPROVED BY N. A. HAUCK				
		DRAWING APPROVAL DATE 87-03-10				
AMSC N/A		REVISION LEVEL K		SIZE A	CAGE CODE 14933	5962-86806
SHEET 1 OF 24						

1. SCOPE

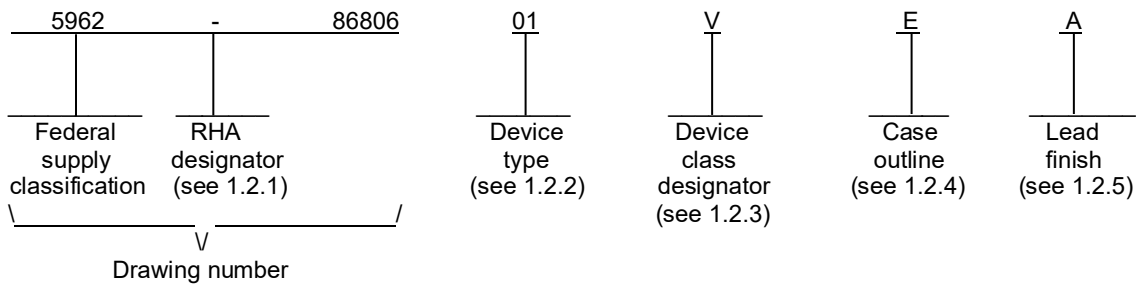
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	1846	Controller, pulse-width modulator
02	1847	Controller, pulse-width modulator
03	1846-SP	Controller, pulse-width modulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

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1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage (VIN)	+40 V dc
Collector supply voltage (VC)	+40 V dc
Output current, source or sink	500 mA dc
Analog inputs	-0.3 V to +VIN
Reference output current	-30 mA dc
Sync output current	-5 mA dc
Error amplifier output current	-5 mA dc
Soft start sink current	50 mA dc
Oscillator charging current	5 mA dc
Power dissipation at TA = +25°C	1000 mW 2/
Power dissipation at TC = +25°C	2000 mW 3/
Junction temperature (TJ)	+150°C
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θJC)	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θJA):	
Case E	100°C/W
Case F	115°C/W
Case 2	88°C/W

1.4 Recommended operating conditions.

Supply voltage range	+8 V dc to +40 V dc
Collector supply voltage range	+4.5 V dc to +40 V dc
Ambient operating temperature range (TA)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (low dose rate = 10 mrad(Si)/s):	
Device type 03	30 krad(Si) 4/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Derate at 10 mW/°C for TA above +50°C.

3/ Derate at 16 mW/°C for TC above +25°C.

4/ The manufacturer supplying device type 03 has performed low dose rate irradiation test. Device type 03 may exhibit enhanced low dose rate sensitivity. However, post irradiation electrical parametric limits remain within the pre-irradiation specifications limits at TID level 30 krad (Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, methods 1019, condition D for total dose of 30 krad (Si).

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reference section							
Output voltage	V _O	T _A = +25°C, I _O = 1 mA	1	01, 02	5.05	5.15	V dc
				03	5.04	5.16	
Line regulation	R _{LINE}	8 V ≤ V _{IN} ≤ 40 V	1,2,3	All	-20	20	mV dc
Load regulation	R _{LOAD}	-10 mA ≤ I _L ≤ -1 mA	1,2,3	All	-15	15	mV dc
Total output variation 3/	---	Line, load, and temperature	1,2,3	All	5.00	5.20	V dc
Short circuit output	I _{OS}	V _{REF} = 0 V, Both negative and positive currents are considered to decrease towards 0.	1,2,3	All	-10		mA dc
Oscillator section							
Initial accuracy	---	T _A = +25°C, R _T = 10 kΩ , C _T = 4700 pF	4	All	39	47	kHz
Frequency change with voltage	Δf _{OSC}	8 V ≤ V _{IN} ≤ 40 V	4,5,6	All	-2.0	2.0	%
Sync output voltage high level	V _{SOH}		1,2,3	All	3.9		V dc
Sync output voltage low level	V _{SOL}		1,2,3	01, 02		2.7	V dc
				03		2.5	
Sync input voltage high level	V _{SIH}	C _T = 0 V	1,2,3	All	3.9		V dc
Sync input voltage low level	V _{SIL}		1,2,3	All		2.5	V dc
Sync input current	I _{SYNC}	Sync voltage = 3.9 V, C _T = 0 V	1,2,3	All		1.5	mA dc

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/2/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Error amplifier section							
Input offset voltage	V _{IO}		1,2,3	All		5.0	mV dc
Input bias current	I _{IB}		1,2,3	All	-1.0		μA dc
Input offset current	I _{IO}		1,2,3	All	-250	250	nA dc
Common mode range	V _{CMR}	8 V ≤ V _{IN} ≤ 40 V	1,2,3	03	0	V _{IN} - 2	V
Open loop voltage gain	A _{VS}	V _O = 1.2 V to 3 V, V _{CM} = 2 V	4,5,6	All	80		dB
Unity gain bandwidth ^{3/}	GBW	T _A = +25°C	4	All	0.7		MHz
Common mode rejection ratio	CMRR	0 V ≤ V _{CM} ≤ 38 V, V _{IN} = 40 V	4,5,6	All	75		dB
Power supply rejection ratio	PSRR	8 V ≤ V _{IN} ≤ 40 V	4,5,6	All	80		dB
Output sink current (COMPENSATION pin)	I _{SINK}	-15 mV ≤ V _{ID} ≤ -5 V, V _{COMP} pin = 1.2 V	1,2,3	All	2.0		mA dc
Output source current (COMPENSATION pin)	I _{SOURCE}	15 mV ≤ V _{ID} ≤ 5 V, V _{COMP} pin = 2.5 V	1,2,3	All		-0.4	mA dc
High level output voltage	V _{OH}	R _L = (COMP) 15 kΩ	1,2,3	All	4.3		V dc
Low level output voltage	V _{OL}	R _L = (COMP) 15 kΩ	1,2,3	All		1.0	V dc

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Current sense amplifier section							
Amplifier gain <u>4/ 5/</u>	A _V	V(-CUR SENSE) pin = 0 V, V(CUR LIM/SS) pin open	4,5,6	01, 02	2.5	3.15	V dc
				03	2.5	3.1	
Maximum differential input signal (pos and neg current sense pin voltages)	V _{DIFF}	V(CUR LIM/SS) pin open, <u>4/</u> R _L = (COMP pin) = 15 kΩ	1,2,3	All	1.1		V dc
Input offset voltage	V _{IO}	V(CUR LIM/SS) pin = 0.5 V, COMP pin open <u>4/</u>	1,2,3	All	-25	25	mV dc
Common mode rejection ratio	CMRR	1 V ≤ V _{CM} ≤ 12 V	4,5,6	All	60		dB
Power supply rejection ratio	PSRR	8 V ≤ V _{IN} ≤ 40 V	4,5,6	All	60		dB
Input bias current	I _{IB}	V(CUR LIM/SS) pin = 0.5 V, <u>4/</u> COMP pin open	1,2,3	All	-10		μA dc
Input offset current	I _{IO}	V(CUR LIM/SS) pin = 0.5 V, <u>4/</u> COMP pin open	1,2,3	All	-1.0	1.0	μA dc
Input common mode range	V _{CMR}		1,2,3	03		V _{IN} - 3	V
Delay to outputs <u>3/</u>	---	T _A = +25°C	9	All		500	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Current limit adjust section							
Current limit offset	---	V(-CUR LIM/SS) pin = 0 V, <u>4/</u> V(+CUR LIM/SS) pin = 0 V, COMP pin open	1,2,3	01, 02	0.40	0.55	V dc
				03	0.45	0.55	
Input bias current	I _{IB}	V(+ERROR AMP) pin = V _{REF} , V(+ERROR AMP) pin = 0 V	1,2,3	All	-30		μA dc
Shutdown terminal section							
Threshold voltage	---	R _L (CUR LIM/SS) pin = 15 kΩ at 2 V or equivalent.	1,2,3	All	250	400	mV dc
Input voltage range	---		1,2,3	03	0	V _{IN}	V
Latching current	---	Current into CUR LIM/SS <u>6/</u>	1,2,3	All	3		mA
Nonlatching current	---	Current into CUR LIM/SS <u>7/</u>	1,2,3	All		0.8	mA
Delay to outputs <u>3/</u>	---	T _A = +25°C	9	All		600	ns
Output section							
Collector-emitter voltage	---		1,2,3	All	40		V dc
Collector leakage current	---	V _C = 40 V	1,2,3	01		200	μA dc
Output low level	V _{OL}	I _{SINK} = 20 mA	1,2,3	All		0.4	V dc
		I _{SINK} = 100 mA				2.1	
Output high level	V _{OH}	I _{SOURCE} = 20 mA	1,2,3	All		13	V dc
		I _{SOURCE} = 100 mA				12	
Rise time <u>3/</u>	t _R	C _L = 1,000 pF, T _A = +25°C	9	All		300	ns
Fall time <u>3/</u>	t _F	C _L = 1,000 pF, T _A = +25°C	9	All		300	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Under-voltage lockout section							
Start-up threshold	---		1,2,3	All		8.0	V dc
Total standby current section							
Supply current	ICC		1,2,3	All		21	mA dc
Cold start/PWM latch reset	LRESET	T _J = -55°C, R _T = 10 kΩ, C _T = 4700 pF, SYNC I _{OUT} = -1 mA	3	All	<u>8/</u>		kHz

1/ Standard test conditions (unless otherwise specified): +V_{IN} = 15 V dc, R_T = 10 kΩ, C_T = 4,700 pF.

2/ Device type 03 supplied to this drawing has been characterized through all levels M, D and P of irradiation. However, device type 03 is only tested at the "P" level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C. The manufacturer supplying device type 03 has performed low dose rate irradiation test. The radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition D for total dose of 30 krad(Si).

3/ If not tested, shall be guaranteed to specified limits.

4/ Parameter measured at trip point of latch with V+ERROR AMP = VREF; V-ERROR AMP = 0 V.

5/ Amplifier gain defined as:

$$G = (\Delta V_{COMP\ pin} / \Delta V_{+CURRENT\ SENSE\ pin}); \Delta V_{+CURRENT\ SENSE\ pin} = 0 \text{ to } 1.0 \text{ V}$$

6/ Current into CUR LIM/SS pin guaranteed to latch circuit in shutdown state.

7/ Current into CUR LIM/SS pin guaranteed not to latch circuit in shutdown state.

8/ To verify that the PWM latch is resetting properly, the output stage must resume switching after the completion of a PWM latch Set command. To minimize the effects of self heating, the test must be completed within the first 50 milliseconds of applied power. The minimum limit shall be equal to 0.49 x the oscillator frequency.

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3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 110 (see MIL-PRF-38535, appendix A).

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Device types	01, 02, and 03	01, 02, and 03	01, 02, and 03
Case outlines	E	F	2
Terminal number	Terminal symbol		
1	CUR. LIMIT/SOFTSTART	CUR. LIMIT/SOFTSTART	NC
2	VREF	VREF	CUR. LIMIT/SOFTSTART
3	(-) CUR. SENSE	(-) CUR. SENSE	VREF
4	(+) CUR. SENSE	(+) CUR. SENSE	(-) CUR. SENSE
5	(+) ERROR AMP	(+) ERROR AMP	(+) CUR. SENSE
6	(-) ERROR AMP	(-) ERROR AMP	NC
7	COMPENSATION	COMPENSATION	(+) ERROR AMP
8	CT	CT	(-) ERROR AMP
9	RT	RT	COMPENSATION
10	SYNC	SYNC	CT
11	OUTPUT A	OUTPUT A	NC
12	GROUND	GROUND	RT
13	Vc	Vc	SYNC
14	OUTPUT B	OUTPUT B	OUTPUT A
15	VIN	VIN	GROUND
16	SHUTDOWN	SHUTDOWN	NC
17	----	----	Vc
18	----	----	OUTPUT B
19	----	----	VIN
20	----	----	SHUTDOWN

NC = No connection

FIGURE 1. Terminal connections.

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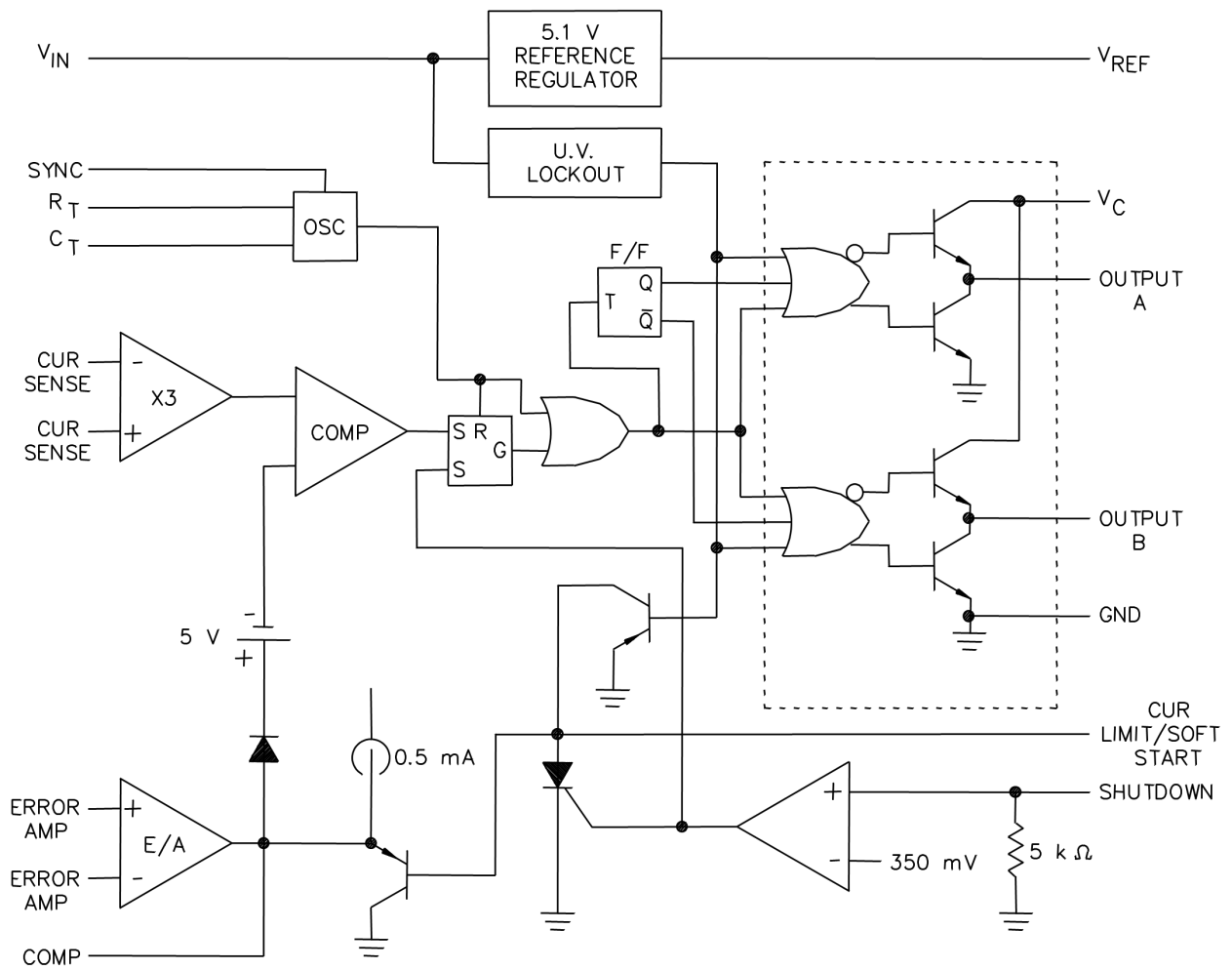


FIGURE 2. Block diagram.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7, 8, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1,4
Final electrical parameters (see 4.2)	1,2,3,4,9 <u>1/</u>	1,2,3,4,9 <u>1/</u>	1,2,3,4,9 <u>1/ 2/</u>
Group A test requirements (see 4.4)	1,2,3,4,5,6,9	1,2,3,4,5,6,9	1,2,3,4,5,6,9
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3,4 <u>2/</u>
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---	1,4,9

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous interim electrical parameters.

TABLE IIB. Burn-in and operating life test. 1/ 2/

Parameters	Symbol	Device type	Delta limits
Reference output voltage	V _O	03	±50 mV
Oscillator accuracy (R _T = 10 kΩ, C _T = 4.7 nF)	---	03	±4 kHz
Error amp input bias current	I _{IB}	03	±0.1 μA
Supply current	I _{CC}	03	±1 mA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

2/ Delta parameters measured at T_A = +25°C.

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition D for device type 03 and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

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6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

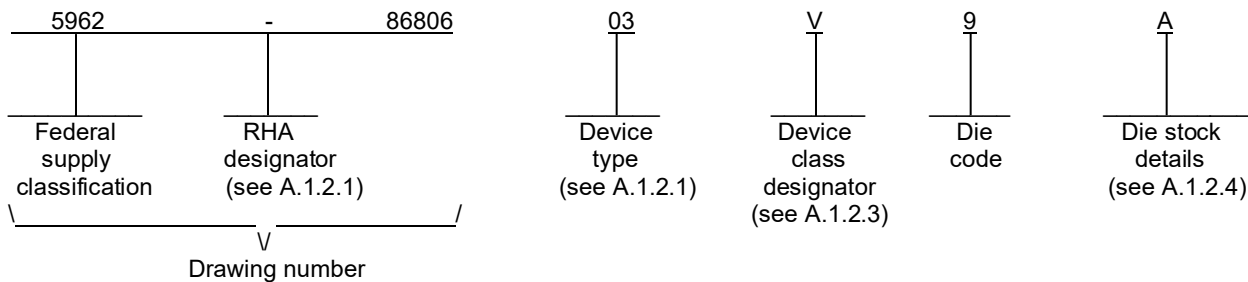
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APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-86806

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
03	1846-SP	Controller, pulse width modulator

A.1.2.3 Device class designator.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.1.5 Radiation features. See paragraph 1.5 herein for details.

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A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

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A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4, and 4.4.4.1 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

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A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0591.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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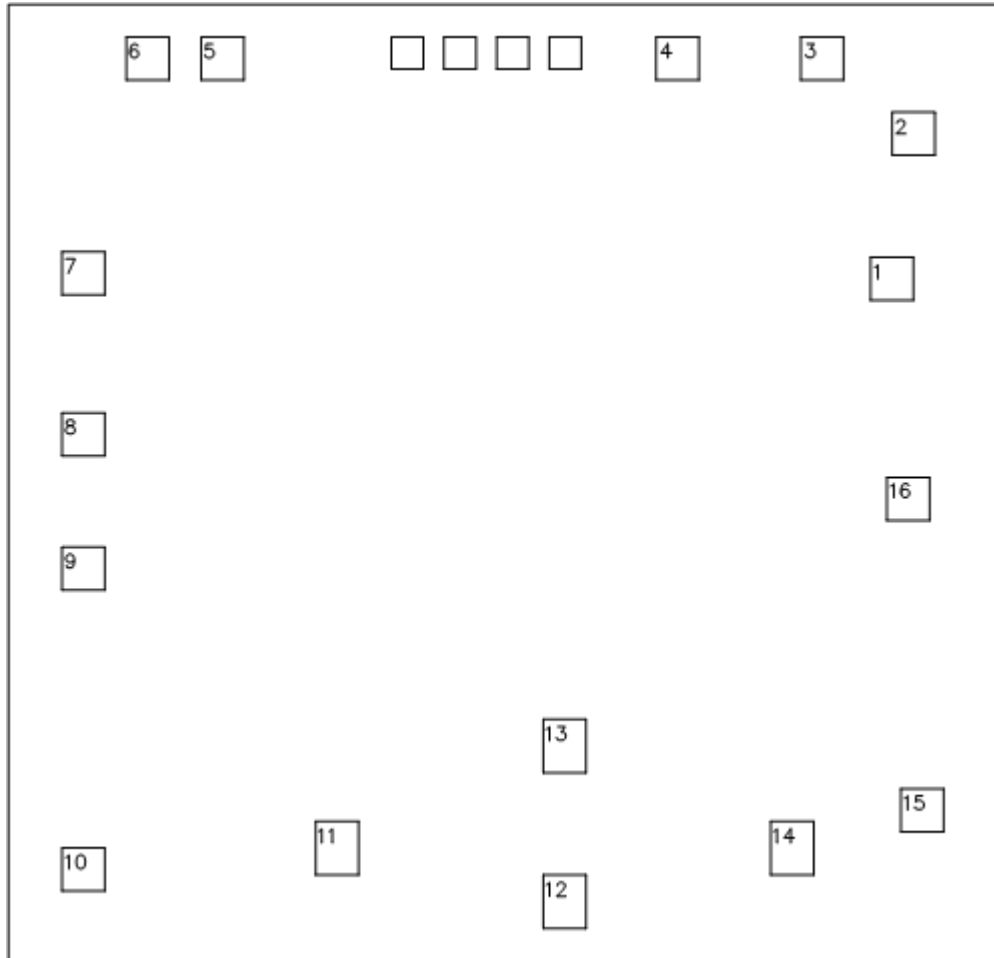


FIGURE A-1. Die bonding pad locations and electrical functions.

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Bond pad coordinates in microns

Terminal symbol	Pad number	X min	Y min	X max	Y max
CUR. LIMIT/ SOFTSTART	1	2174.24	1661.16	2280.92	1767.84
VREF	2	2235.2	2026.92	2341.88	2133.6
(-) CUR. SENSE	3	1996.44	2219.96	2103.12	2326.64
(+) CUR. SENSE	4	1635.76	2219.96	1742.44	2326.64
(+) ERROR AMP	5	467.36	2219.96	574.04	2326.64
(-) ERROR AMP	6	289.56	2219.96	396.24	2326.64
COMPENSATION	7	142.24	1671.32	248.92	1778
CT	8	157.48	1270	264.16	1376.68
RT	9	157.48	939.8	264.16	1046.48
SYNC	10	157.48	172.72	264.16	279.4
OUTPUT A	11	772.16	213.36	889	350.52
GROUND	12	1346.2	81.28	1463.04	208.28
Vc	13	1341.12	472.44	1468.12	645.16
OUTPUT B	14	1920.24	213.36	2037.08	350.52
VIN	15	2255.52	320.4	2362.2	426.72
SHUTDOWN	16	2214.88	1107.44	2321.56	1214.12

FIGURE A-1. Die bonding pad locations and electrical functions - Continued

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Die physical dimensions.

Die size: 2514.6 mils x 2413.0 mils

Die thickness: 15 mils

Interface materials.

Top metallization: AlCu2

Backside metallization: Not applicable

Glassivation.

Type: TEOS

Thickness: 7 kÅ

Substrate: Single crystal silicon

Assembly related information.

Substrate potential:

Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - Continued

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-04-26

Approved sources of supply for SMD 5962-86806 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8680601EA	01295	UC1846J-DESC
	34333	SG1846J-DESC
	<u>3</u> /	LT1846J/883B
5962-8680601FA	34333	SG1846F-DESC
5962-86806012A	01295	UC1846L-DESC
	<u>3</u> /	SG1846L/883B
5962-8680601VEA	01295	UC1846JQMLV
5962-8680601V2A	01295	UC1846LQMLV
5962-8680602EA	<u>3</u> /	UC1847J883B
	<u>3</u> /	SG1847J/883
	<u>3</u> /	LT1847J/883B
5962-8680602FA	<u>3</u> /	SG1847F/883B
5962-86806022A	<u>3</u> /	UC1847L/883B
	<u>3</u> /	SG1847L/883B

STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued

DATE: 23-04-26

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8680603VEA	01295	UC1846J-SP
5962-8680603VFA	01295	UC1846W-SP
5962-8680603V2A	01295	UC1846FK-SP
5962-8680603V9A	01295	UC1846KGD-SP
5962P8680603VEA	01295	UC1846J-RHA
5962P8680603VFA	01295	UC1846W-RHA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number

Vendor name and address

01295

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
PO Box 660199
Dallas, TX 75243

34333

Microsemi Analog Mixed Signal Group
11861 Western Avenue
Garden Grove, CA 92841-2119

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